To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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BB102C

Build in Biasing Circuit MOS FET IC
UHF RF Amplifier

RENESAS

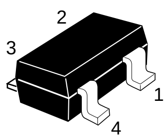
ADE-208-588 (Z)
1st. Edition
November 1997

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics;
  (NF = 2.1 dB typ. at f = 900 MHz)
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-4(SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Note 1 Marking is “BW–”.
- Note 2 BB302C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

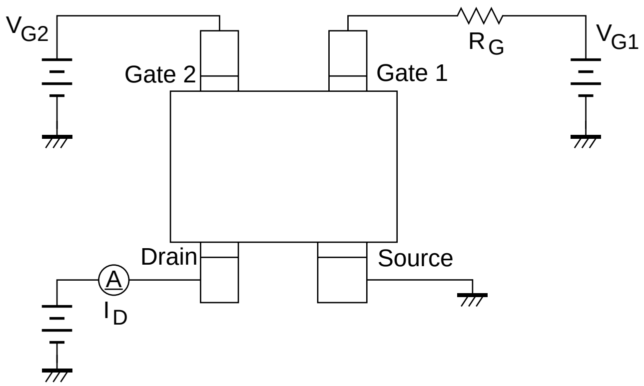
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	12	V
Gate1 to source voltage	V_{G1S}	+10 –0	V
Gate2 to source voltage	V_{G2S}	±10	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

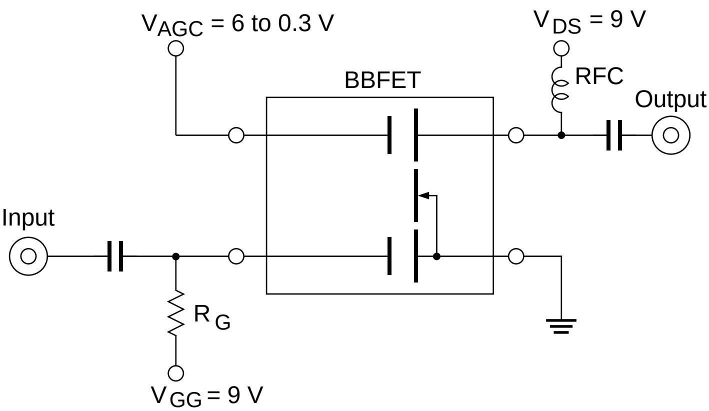
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	12	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+10	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±10	—	—	V	I_{G2} = ±10µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +9V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	±100	nA	V_{G2S} = ±9V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.1	—	0.8	V	V_{DS} = 9V, V_{G2S} = 6V, I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	—	1.1	V	V_{DS} = 9V, V_{G1S} = 9V, I_D = 100µA
Drain current	$I_{D(op)}$	10	15	20	mA	V_{DS} = 9V, V_{G1} = 9V, V_{G2S} = 6V R_G = 560kΩ
Forward transfer admittance	$\|y_{fs}\|$	16	21	—	mS	V_{DS} = 9V, V_{G1} = 9V, V_{G2S} =6V R_G = 560kΩ, f = 1kHz
Input capacitance	c_{iss}	1.2	1.6	2.2	pF	V_{DS} = 9V, V_{G1} = 9V
Output capacitance	c_{oss}	0.7	1.1	1.5	pF	V_{G2S} =6V, R_G = 560kΩ
Reverse transfer capacitance	c_{rss}	—	0.011	0.03	pF	f = 1MHz
Power gain	PG	16	20	—	dB	V_{DS} = 9V, V_{G1} = 9V, V_{G2S} =6V
Noise figure	NF	—	2.1	3.1	dB	R_G = 120kΩ, f = 900MHz

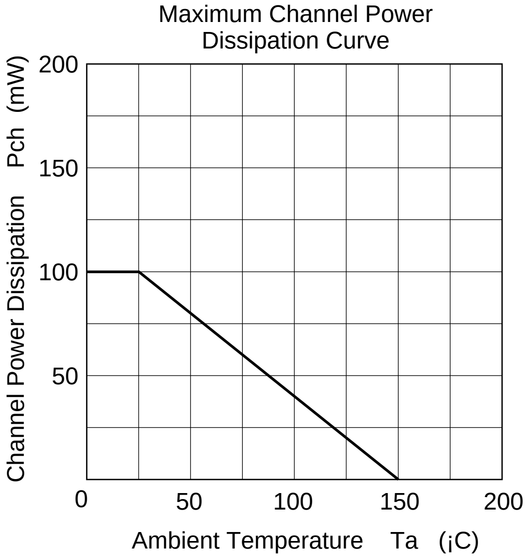
Main Characteristics

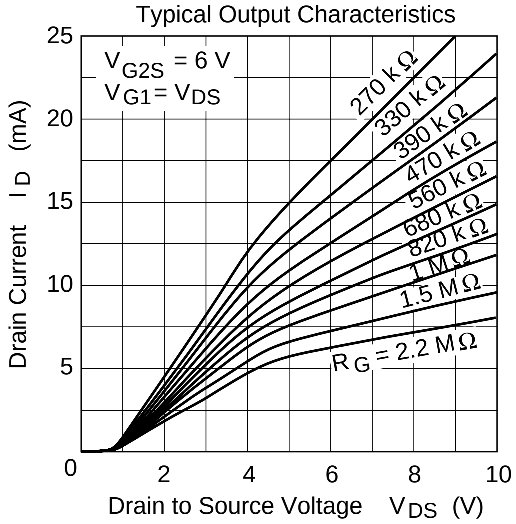
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

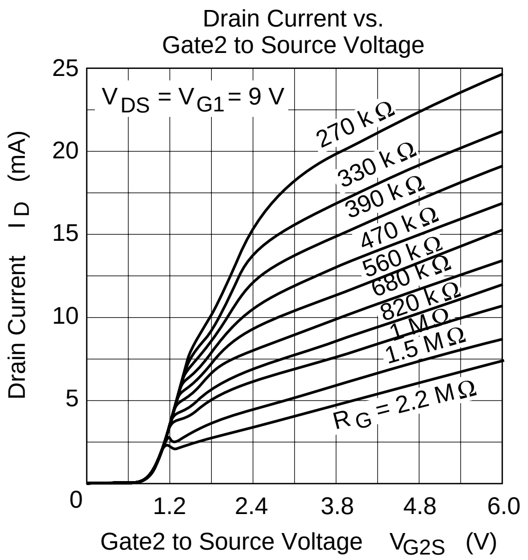


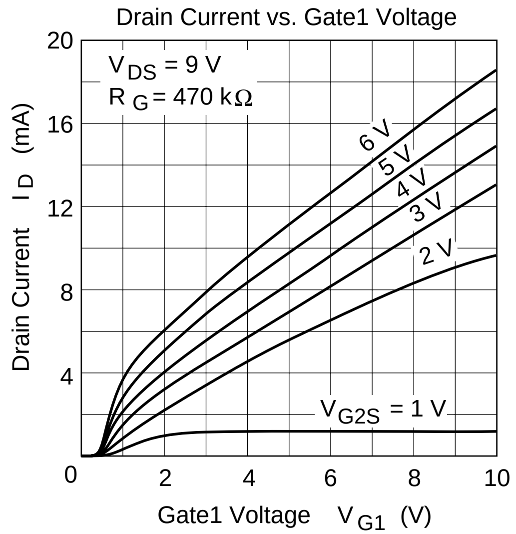
Application Circuit

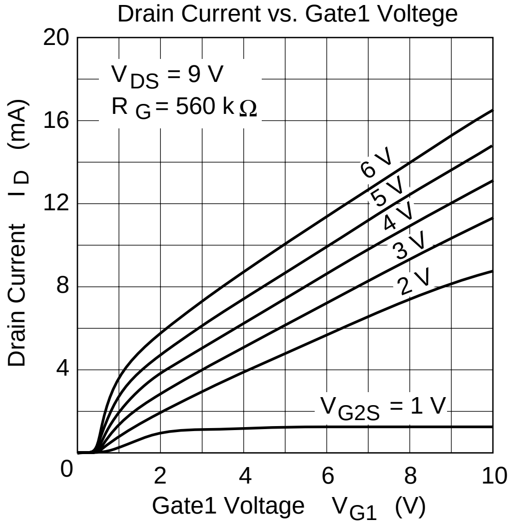


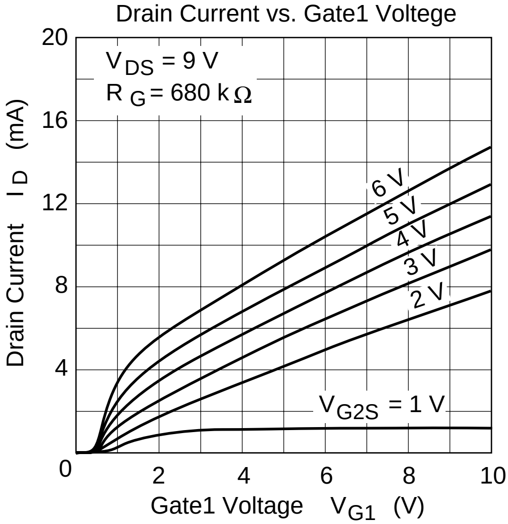

Maximum Channel Power
Dissipation Curve
Channel Power Dissipation Pch (mW)
200
150
100
50
0
50
100
150
200
Ambient Temperature Ta (¡C)

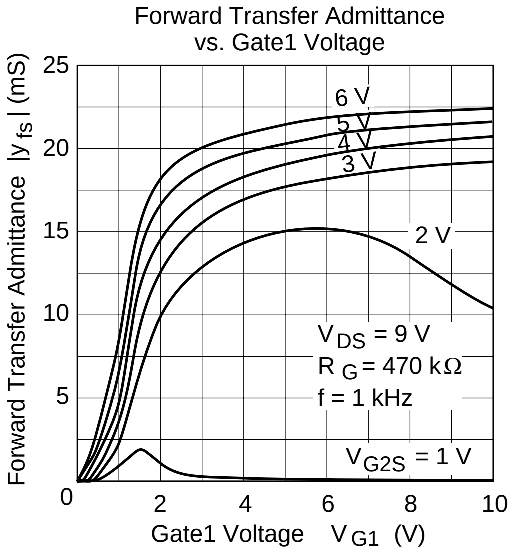

Typical Output Characteristics
V_{G2S} = 6 V
$V_{G1} = V_{DS}$
270 kΩ
330 kΩ
390 kΩ
470 kΩ
560 kΩ
680 kΩ
820 kΩ
1 MΩ
1.5 MΩ
R_G = 2.2 MΩ
Drain Current I_D (mA)
25
20
15
10
5
0
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)

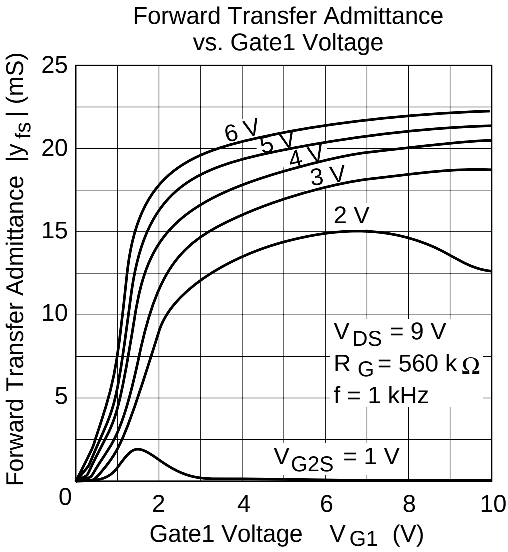

Drain Current vs.
Gate2 to Source Voltage
$V_{DS} = V_{G1}$ = 9 V
270 kΩ
330 kΩ
390 kΩ
470 kΩ
560 kΩ
680 kΩ
820 kΩ
1 MΩ
1.5 MΩ
R_G = 2.2 MΩ
Drain Current I_D (mA)
25
20
15
10
5
0
1.2
2.4
3.8
4.8
6.0
Gate2 to Source Voltage V_{G2S} (V)

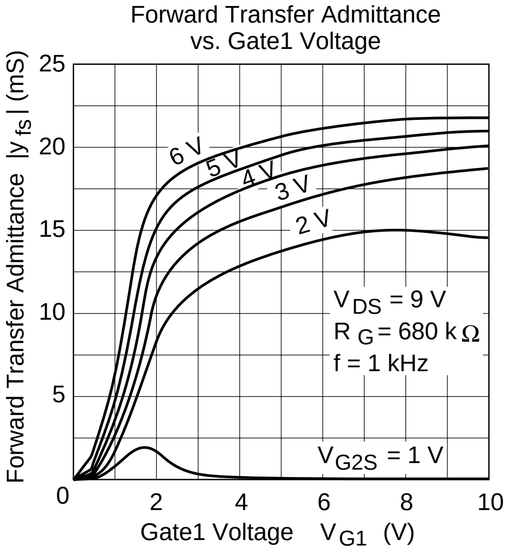

Drain Current vs. Gate1 Voltage
V_{DS} = 9 V
R_G = 470 kΩ
6 V
5 V
4 V
3 V
2 V
V_{G2S} = 1 V
Drain Current I_D (mA)
20
16
12
8
4
0
2
4
6
8
10
Gate1 Voltage V_{G1} (V)

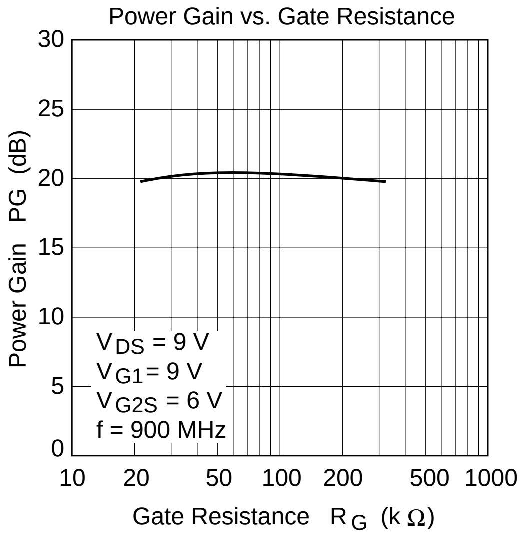

Drain Current vs. Gate1 Voltege
V DS = 9 V
R G = 560 kΩ
6 V
5 V
4 V
3 V
2 V
VG2S = 1 V
Drain Current I D (mA)
Gate1 Voltage VG1 (V)
0
2
4
6
8
10
4
8
12
16
20

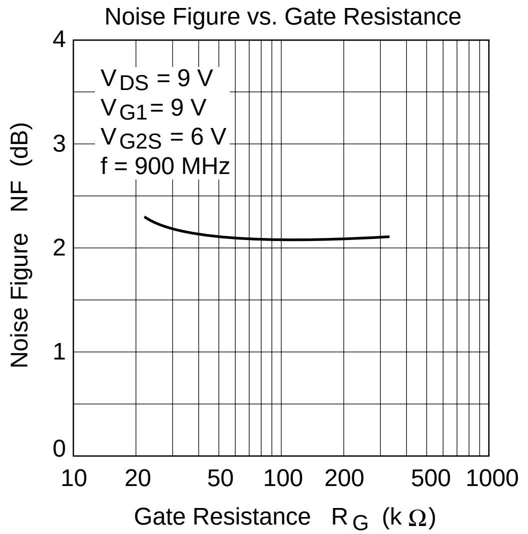

Drain Current vs. Gate1 Voltege
V DS = 9 V
R G = 680 kΩ
6 V
5 V
4 V
3 V
2 V
VG2S = 1 V
Drain Current I D (mA)
Gate1 Voltage VG1 (V)
0
2
4
6
8
10
4
8
12
16
20

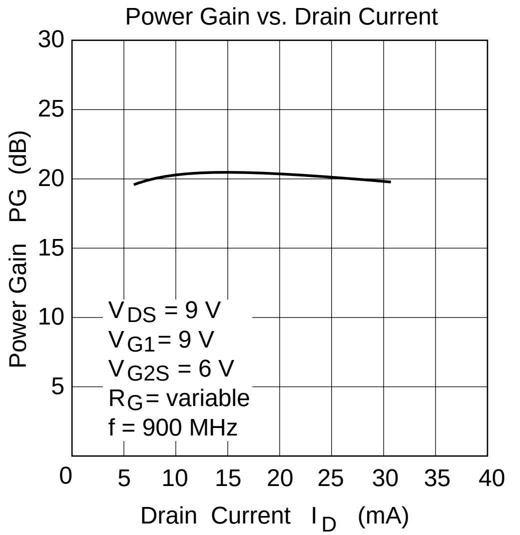

Forward Transfer Admittance
vs. Gate1 Voltage
6 V
5 V
4 V
3 V
2 V
V DS = 9 V
R G = 470 kΩ
f = 1 kHz
VG2S = 1 V
Forward Transfer Admittance |yfs| (mS)
Gate1 Voltage V G1 (V)
0
2
4
6
8
10
5
10
15
20
25

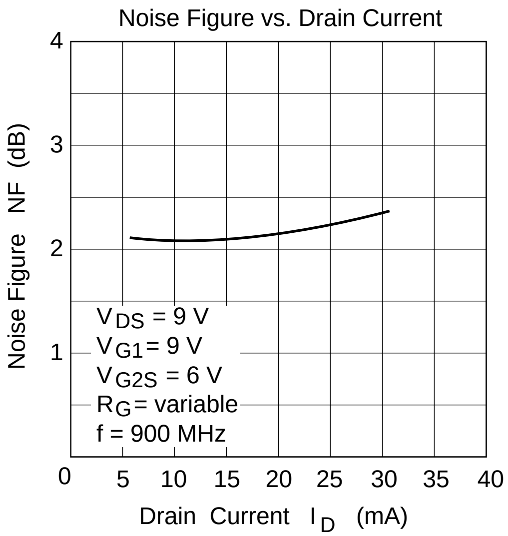

Forward Transfer Admittance
vs. Gate1 Voltage
6 V
5 V
4 V
3 V
2 V
V DS = 9 V
R G = 560 kΩ
f = 1 kHz
VG2S = 1 V
Forward Transfer Admittance |yfs| (mS)
Gate1 Voltage V G1 (V)
0
2
4
6
8
10
5
10
15
20
25

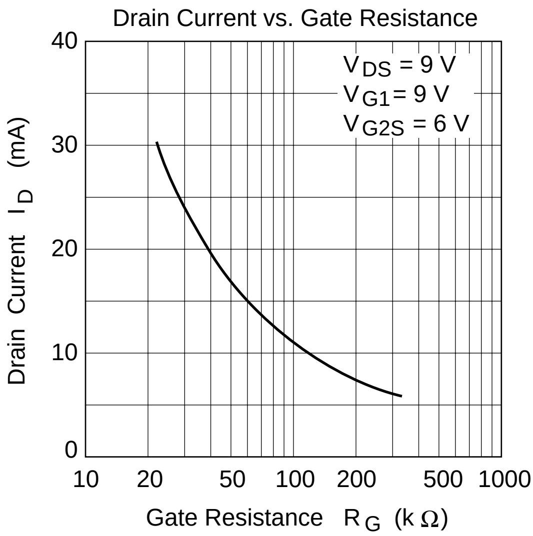

Forward Transfer Admittance
vs. Gate1 Voltage
Forward Transfer Admittance |y fs| (mS)
25
20
15
10
5
0
2
4
6
8
10
Gate1 Voltage V G1 (V)
6 V
5 V
4 V
3 V
2 V
V DS = 9 V
R G = 680 k Ω
f = 1 kHz
V G2S = 1 V

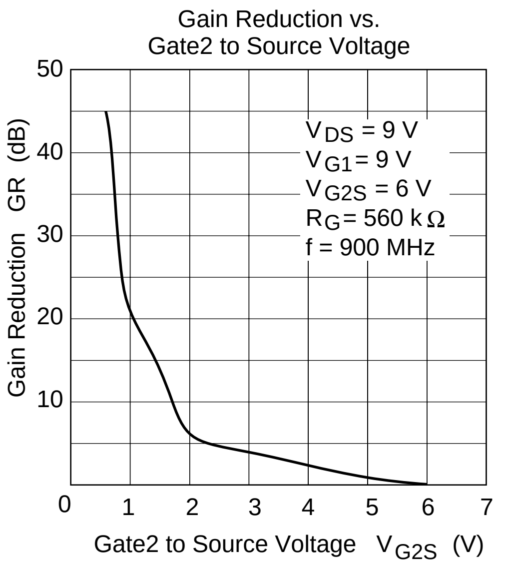

Power Gain vs. Gate Resistance
Power Gain PG (dB)
30
25
20
15
10
5
0
10
20
50
100
200
500
1000
Gate Resistance R G (k Ω)
V DS = 9 V
V G1 = 9 V
V G2S = 6 V
f = 900 MHz

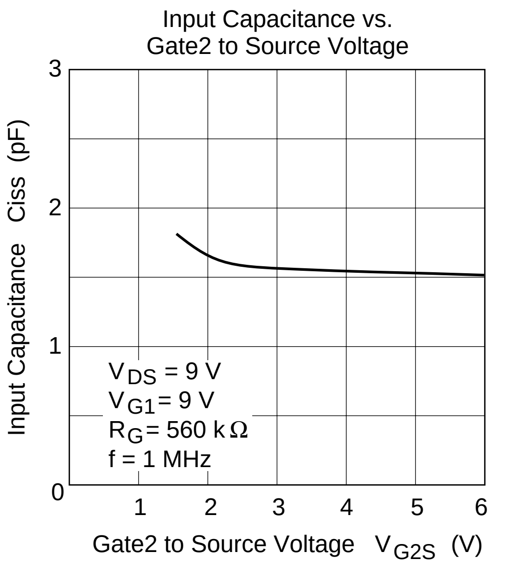

Noise Figure vs. Gate Resistance
Noise Figure NF (dB)
4
3
2
1
0
10
20
50
100
200
500
1000
Gate Resistance R G (k Ω)
V DS = 9 V
V G1 = 9 V
V G2S = 6 V
f = 900 MHz


Power Gain vs. Drain Current
Power Gain PG (dB)
30
25
20
15
10
5
0
5
10
15
20
25
30
35
40
Drain Current I D (mA)
V DS = 9 V
V G1 = 9 V
V G2S = 6 V
R G = variable
f = 900 MHz

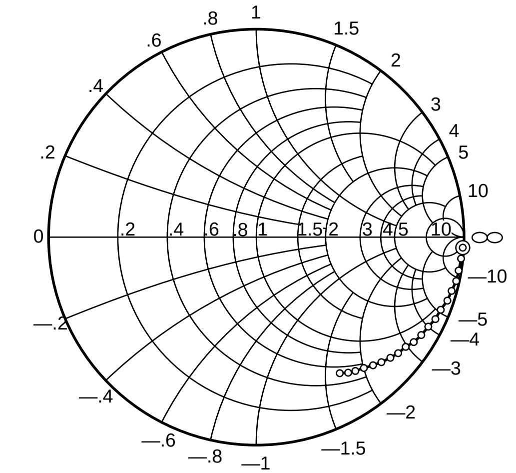

Noise Figure vs. Drain Current
Noise Figure NF (dB)
Drain Current I_D (mA)
V_{DS} = 9 V
V_{G1} = 9 V
V_{G2S} = 6 V
R_G = variable
f = 900 MHz
0 5 10 15 20 25 30 35 40
1 2 3 4


Drain Current vs. Gate Resistance
Drain Current I_D (mA)
Gate Resistance R_G (k Ω)
V_{DS} = 9 V
V_{G1} = 9 V
V_{G2S} = 6 V
10 20 50 100 200 500 1000
0 10 20 30 40


Gain Reduction vs.
Gate2 to Source Voltage
Gain Reduction GR (dB)
Gate2 to Source Voltage V_{G2S} (V)
V_{DS} = 9 V
V_{G1} = 9 V
V_{G2S} = 6 V
R_G = 560 k Ω
f = 900 MHz
0 1 2 3 4 5 6 7
10 20 30 40 50

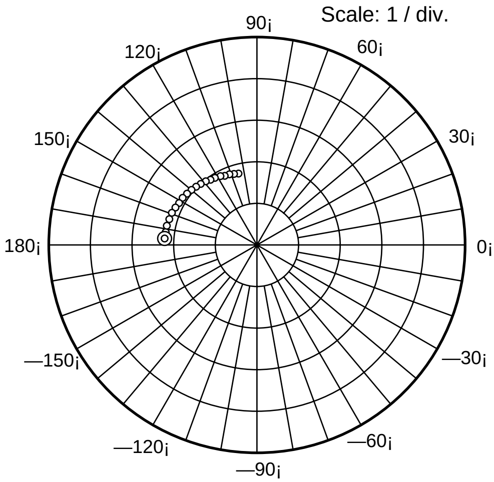

Input Capacitance vs.
Gate2 to Source Voltage
Input Capacitance Ciss (pF)
Gate2 to Source Voltage V_{G2S} (V)
V_{DS} = 9 V
V_{G1} = 9 V
R_G = 560 k Ω
f = 1 MHz
1 2 3 4 5 6
0 1 2 3

S11 Parameter vs. Frequency



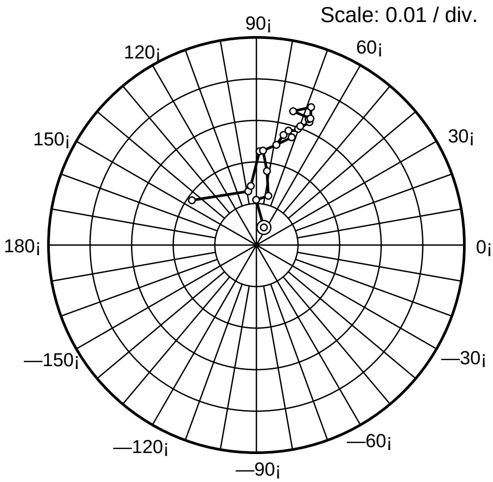
Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 560 kΩ
50 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency



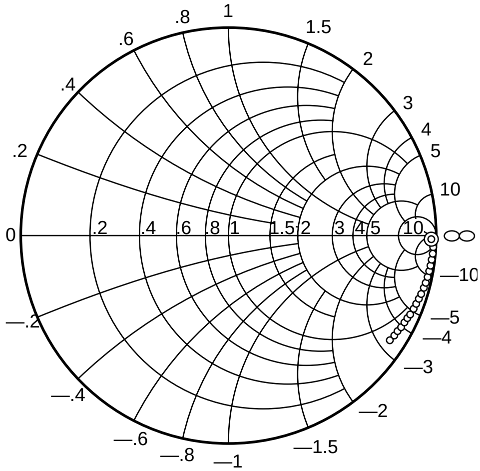
Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 560 kΩ
50 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency



Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 560 kΩ
50 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 560 kΩ
50 1000 MHz (50 MHz step)

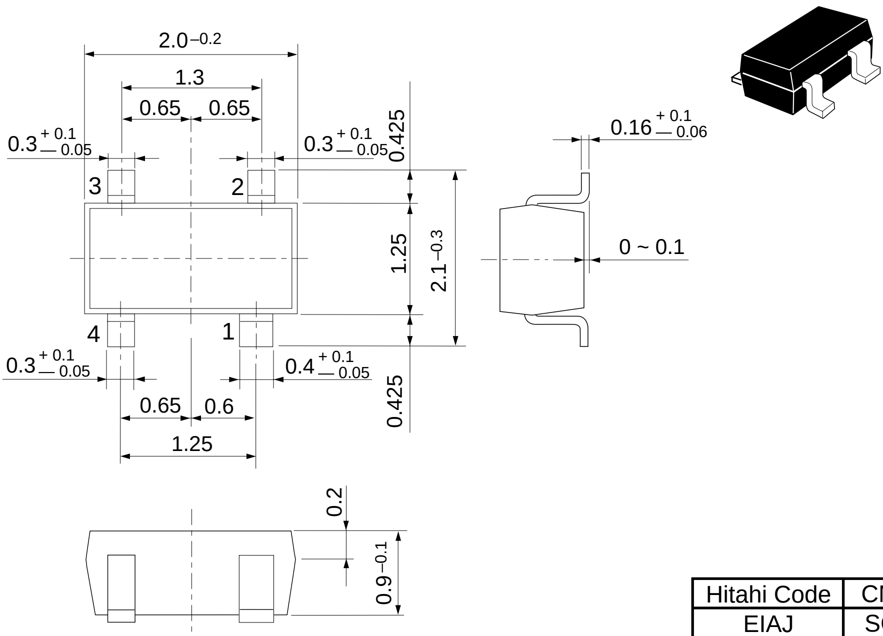
RENESAS

Sparameter (V_{DS} = V_{G1} = 9V, V_{G2S} = 6V, R_G = 560kΩ, Zo = 50Ω)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.995	–2.9	2.22	176.0	0.00046	66.9	0.977	–1.0
100	0.991	–6.0	2.21	172.0	0.00109	90.4	0.987	–3.2
150	0.987	–9.4	2.21	168.0	0.00122	76.5	0.987	–5.0
200	0.985	–12.4	2.19	163.6	0.00180	81.9	0.985	–6.7
250	0.975	–15.4	2.18	159.3	0.00228	86.0	0.983	–8.4
300	0.969	–18.4	2.15	155.3	0.00246	78.8	0.981	–10.0
350	0.954	–21.5	2.12	151.7	0.00273	76.2	0.979	–11.7
400	0.948	–24.6	2.11	147.6	0.00331	66.9	0.976	–13.4
450	0.933	–27.5	2.08	143.7	0.00334	74.7	0.973	–14.9
500	0.923	–30.7	2.05	139.9	0.00357	68.4	0.969	–16.8
550	0.912	–33.6	2.02	136.2	0.00328	67.5	0.965	–18.3
600	0.892	–36.3	1.99	123.9	0.00305	69.8	0.961	–19.9
650	0.882	–39.3	1.96	128.7	0.00322	66.7	0.958	–21.5
700	0.868	–42.0	1.92	125.4	0.00297	70.3	0.953	–23.4
750	0851	–45.0	1.90	122.0	0.00286	74.4	0.948	–24.7
800	0.834	–47.7	1.87	117.9	0.00273	71.9	0.944	–26.2
850	0.815	–50.6	1.83	114.9	0.00226	88.1	0.940	–27.9
900	0.801	–53.5	1.82	111.2	0.00143	95.5	0.934	–29.4
950	0.788	–55.9	1.79	107.8	0.00131	98.6	0.931	–31.0
1000	0.768	–58.5	1.77	104.4	0.00189	145.2	0.925	–32.9

Package Dimensions

Unit: mm



Hitahi Code	CMPAK-4
EIAJ	SC-82AB
JEDEC	

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Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX