5-channel BTL driver for CD players BA6795FP

The BA6795FP is a 5-channel BTL power driver for CD players and has an internal 5V regulator (attached PNP transistor required). The loading and spindle motor output pins are dual-use output pins and are switched between drivers using a control input. In addition, the internal level shifting circuit reduces the number of external components.

Applications

CD players, CD-ROM drives and other optical disc devices

Features

- 1) 5-channel BTL driver in a HSOP 28-pin package, ideal for application miniaturization.
- Internal level shifting circuit reduces the number of external components.
- 3) Gain is adjustable with an attached resistor.
- 4) Internal thermal shutdown circuit.
- 5) Internal 5V regulator. (attached PNP transistor required)

Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	18	V
Power dissipation	Pd	1.7* ¹	W
Operating temperature	Topr	-35~+85	°C
Storage temperature	Tstg	-55~+150	Ĉ

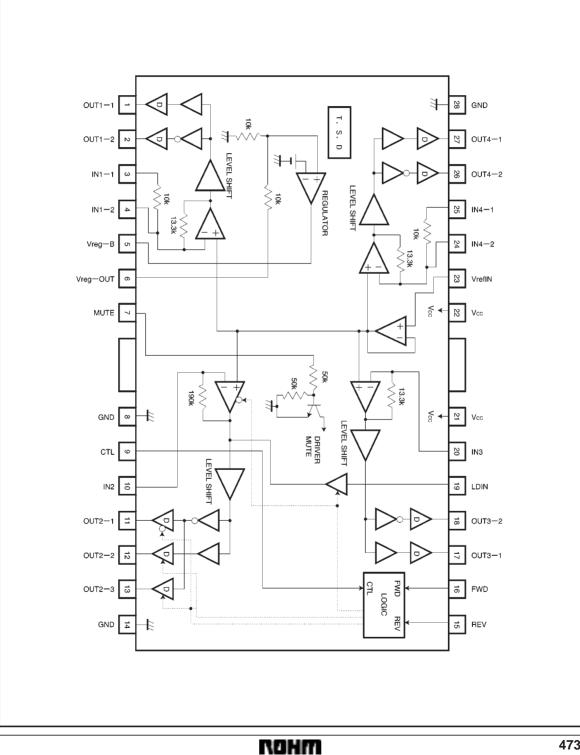
*1 When mounted on a 50 mm×50 mm×1.0 mm paper phenol board Reduced by 13.6 mW for each increase in Ta of 1°C over 25°C.

• Recommended operating conditions (Ta = 25° C)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power supply voltage	Maa	4.8	—	12.0	V
	Vcc	6.0	-	12.0	V*2

*2 Without regulator

Block diagram



Pin descriptions

Pin No.	Pin name	Function
1	OUT-1	Channel 1 negative output
2	OUT-2	Channel 1 positive output
3	IN 1-1	Channel 1 input
4	IN 1-2	Channel 1 gain adjustment input
5	Vreg—B	Attached transistor base connection
6	Vreg-OUT	Constant voltage output (attached transistor collector connection)
7	MUTE	Mute-on control
8	GND	Ground
9	CTL	Loading/spindle switching
10	IN 2	Channel 2 gain adjustment input
11	OUT-1	Channel 2 positive output
12	OUT-2	Channel 2 negative output/Loading positive output
13	OUT—3	Loading negative output
14	GND	Substrate ground
15	REV	Loading reverse input
16	FWD	Loading forward input
17	OUT3-1	Channel 3 negative output
18	OUT3-2	Channel 3 positive output
19	LDIN	Loading input
20	IN 3	Channel 3 gain adjustment input
21	Vcc	Vcc
22	Vcc	Vcc
23	VrefIN	Bias amplifier input
24	IN 4-2	Channel 4 gain adjustment input
25	IN 4-1	Channel 4 input
26	OUT4-2	Channel 4 positive output
27	OUT4-1	Channel 4 negative output
28	GND	Substrate ground

Note 1: Positive and negative output is relative to the polarity of the input pins.

Note 2: Loading positive output and loading negative output indicate the phase relative to the mode.



Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions			
Quiescent current dissipation	lcc	7.0	10.0	13.0	mA	No load			
Mute-off voltage	VMOFF	2.0	—	—	V				
Mute-on voltage	VMON	—	—	0.5	V				
Drivers (other than loading	drive) \rangle								
Output offset voltage 1	Voo1	-40	—	40	mV	Channels 1, 3 and 4, Driver			
Output offset voltage 2	V002	-60	—	60	V	Channel 2 driver (spindle)			
Maximum output voltage 1	Vон1	3.8	4.3	—	V	V _{IN} =8V			
Maximum output voltage 2	Vон2	—	-4.3	-3.8	V	V _{IN} =0.7V			
Closed loop voltage gain 1	Gvc1	5.5	8.0	10.5	dB	$V_{\rm IN} = \mu 0.5 V^{*1}$			
Closed loop voltage gain 2	Gvc2	7.5	11.0	14.5	dB	$V_{\rm IN} = \mu 0.5 V^{*2}$			
Ripple rejection	RR	_	60		dB	VIN=0.1Vrms, 100Hz			
Slew rate	SR	—	2.0	—	V/µs	100 Hz square wave, 3VP-P output			
$\langle Loading drivers angle$									
Output voltage F	Vof	2.7	3.2	3.7	V	Vcc=8V, RL=45Ω, VLD=3.0V			
Output voltage R	Vor	-2.5	-3.0	-3.5	V				
Output voltage range F	Vomf	1.9	2.2	_	V	$V_{CC}=8V, RL=45\Omega, VLD=4.5V^{*3}$			
Output voltage range R	Vomr	—	-2.2	-1.9	V				
Output load variation F1	ΔV_{F1}	—	250	500	mV	Vcc=8V, VLD=3.0V I=100→400mA*4			
Output load variation R1	ΔVR1	—	250	500	mV				
Output load variation F2	ΔV_{F2}	-	600	850	mV	Vcc=5V, VLD=4.5V			
Output load variation R2	ΔV_{R2}	—	600	850	mV	I=100→400mA* ⁵			
Supply voltage variation F	ΔV_{FL}	-500	_	500	mV				
Supply voltage variation R	ΔV_{RL}	-500	—	500	mV	Vcc=4.8V→12V, RL=∞			
Output offset voltage	Vool	-50	2.0	50	mV	When braking: Output voltage			
(Controllers CTL, FWD and	$REV\rangle$								
nput high level voltage 1	Vih1	2.0	—	_	V	FWD (pin 16), REV (pin 15)			
nput low level voltage 1	VIL1	_	_	0.5	V	Determined by input pin voltage			
nput high level voltage 2	VIH2	4.0		—	V	CTL (pin 9)			
nput low level voltage 2	VIL2	—	—	0.5	V	Determined by input pin voltage			
nput high level current	Ін	_	_	500	μA	VIN=5V			
nput low levelcurrent	hu	-		500	μA	V _{IN} =0V			
$\langle 5 V regulator angle$									
Output voltage	Vreg	4.75	5.00	5.25	V	I∟=100mA			
Output load variation	ΔV_{RL}	-50	0	50	mV	I∟=0~200mA			
Supply voltage variation	ΔVvcc	-50	0	25	mV	(Vcc=6~9V) IL=100mA			

ONot designed for radiation resistance.

*1 Attach a 10 k Ω resistor to the inputs (channel 1, channel 3 and channel 4).

*2 Attach a 100 k Ω resistor to the inputs (channel 2).

*3 Vomf and Vomr remain roughly the same even when loading input VLD (pin 19) is opened.

*4 $\Delta V_{f1}, \Delta V_{r1}$ indicate load variation at unclipped, 3.0 V output.

*5 ΔVr2, ΔVr2 indicate load variation when output is clipped to generate 4.5 V input at reduced voltage (5 V).



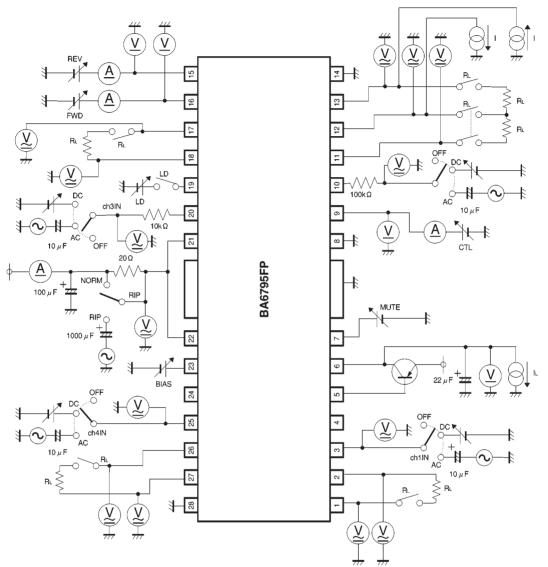


Fig.1



Measruement circuit switch table

$\begin{array}{ c c c c c c c c c c c c c c c c c c c$. .									
Mute-off voltageONONIIIDCDCDCDCDCDCDCV/C or GNDMute-on voltageONONIIIDCDCDCDCDCDCV/C or GND(Drivers (other than loading driver))Output offset voltageONONOFFNORMDCDCDCDCDCDCDCV/C or GNDMaximum output voltageIIIIIIIIDCDCDCDCDCV/C or 0.7VClosed loop voltage gain 1IIIIIIIIDCDCDCDCDCDCV/C or 0.7VClosed loop voltage gain 2IIIIIIIIDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDC	Parameter	RL	RL'	LD	RIP	CH1	CH2	СНЗ	CH4	Note
Mute-on voltageONON \downarrow \downarrow DCDCDCDCDCDCV: voc or GND(Drivers (other than loading driver)>Output offset voltageONONOFFNORMDCDCDCDCDCDC:bit voltageMaximum output voltage \downarrow <td>Quiescent current dissipation</td> <td>OFF</td> <td>OFF</td> <td>OFF</td> <td>NORM</td> <td>OFF</td> <td>OFF</td> <td>OFF</td> <td>OFF</td> <td></td>	Quiescent current dissipation	OFF	OFF	OFF	NORM	OFF	OFF	OFF	OFF	
	Mute-off voltage	ON	ON	Ļ	Ļ	DC	DC	DC	DC	DC: Vcc or GND
Output offset voltageONONOFFNORMDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCDCNORMDCDCDCDCDCDCNORVOTDCDCDCDCNORVDCDCDCNORVDCDCNORVDCDCNORVDCNORDCDCNORDCNORDCDCNORDCNORNORNORACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACAC <t< td=""><td>Mute-on voltage</td><td>ON</td><td>ON</td><td>Ļ</td><td>Ļ</td><td>DC</td><td>DC</td><td>DC</td><td>DC</td><td>DC: Vcc or GND</td></t<>	Mute-on voltage	ON	ON	Ļ	Ļ	DC	DC	DC	DC	DC: Vcc or GND
Maximum output voltageIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII <t< td=""><td>$\langle { m Drivers}$ (other than loading driver)$angle$</td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td></t<>	$\langle { m Drivers}$ (other than loading driver) $ angle$				1					
Closed loop voltage gain 1IIIIIIIIIIIIIDC: bias ±0.5 VClosed loop voltage gain 2IIIIIIIIIDC: bias ±0.5 VRipple rejectionIIIIRIPIIIIDC: bias ±0.5 VSiew rateIIIRIPIIIIDC: bias voltageSiew rateIIINORMACACACACAC: 100 Hz square wav(Loading drivers)Output voltage FONONNNORMOFFDCOFFOFFDC: bias voltageOutput voltage range FIIIIIIIDC: bias voltageOutput voltage range RIIIIIIDC: bias voltageOutput voltage range RIIIIIIDC: bias voltageLoad regulation FIOFFIIIIDC: bias voltageLoad regulation RIIIIIIDC: bias voltageController pins>Input high level voltage 1ONONOFFNCRMOFFDCOFFInput high level voltage 2IIIIIIIIIIInput high level voltage 2IIIIIIIIIInpu	Output offset voltage	ON	ON	OFF	NORM	DC	DC	DC	DC	DC: bias voltage
Closed loop voltage gain 2IIIIIIIIIRipple rejectionIIIIIIIIIDC: bias ±0.5 VRipple rejectionIIIIRIPIIIIDC: bias voltageSlew rateIIIINORMACACACACACIOD Hz square wav(Loading drivers)Output voltage FONONONNORMOFFDCOFFDFFDC: bias voltageOutput voltage RIIIIIIIDC: bias voltageOutput voltage range FIIIIIIDC: bias voltageOutput voltage range RIIIIIIDC: bias voltageOutput voltage range RIIIIIIDC: bias voltageLoad regulation FIOFFIIIIDC: bias voltageLoad regulation RIIIIIIDC: bias voltageLine regulationIIIIIIIDC: bias voltageOutput offset voltageIONONOFFNCRMOFFDCDFFInput high level voltage 1ONONOFFNCRMOFFDCOFFIInput high level voltage 2IIIIIIII </td <td>Maximum output voltage</td> <td>Ļ</td> <td>Ļ</td> <td>Ļ</td> <td>Ļ</td> <td>ţ</td> <td>Ļ</td> <td>Ļ</td> <td>Ļ</td> <td>DC: Vcc or 0.7V</td>	Maximum output voltage	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: Vcc or 0.7V
Ripple rejectionIIIRIPIIIIDC: bias voltageSlew rateIIIINORMACACACACACIDC: bias voltageSlew rateIIIINORMACACACACACIDC: bias voltageOutput voltage FONONONNORMOFFDCOFFOFFDC: bias voltageOutput voltage range FIIIIIIIIDC: bias voltageOutput voltage range RIIIIIIIIIIDC: bias voltageOutput voltage range RIIIIIIIIIIIDC: bias voltageLoad regulation FIOFFIIIIIIIIIDC: bias voltageLoad regulation RIIIIIIIIIIIIIDC: bias voltageOutput offset voltageIIONOFFIIIIIIIIIDC: bias voltageOutput offset voltageIIONOFFIIIIIIIIIIIDC: bias voltage(Controller pins)Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput high level voltage 2IIIIIIIIIIIIIIIIIIIIIIInput low level voltage 2IIIIIIIIIIIIIIIIIIII	Closed loop voltage gain 1	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	DC: bias <u>+</u> 0.5 V
Silew rateIIINORMACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACACAC <th< td=""><td>Closed loop voltage gain 2</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>DC: bias <u>+</u>0.5 V</td></th<>	Closed loop voltage gain 2	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	DC: bias <u>+</u> 0.5 V
〈Loading drivers〉ONONONONNORMOFFDCOFFOFFDC: bias voltageOutput voltage R↓↓↓↓↓↓↓↓↓↓DC: bias voltageOutput voltage range F↓↓↓↓↓↓↓↓↓DC: bias voltageOutput voltage range R↓↓↓↓↓↓↓↓DC: bias voltageOutput voltage range R↓↓↓↓↓↓↓DC: bias voltageLoad regulation F↓OFF↓↓↓↓↓DC: bias voltageLoad regulation R↓↓↓↓↓↓DC: bias voltageLine regulation R↓↓↓↓↓↓DC: bias voltageOutput offset voltage↓↓↓↓↓↓DC: bias voltageOutput offset voltage↓ONOFF↓↓↓↓DC: bias voltage(Controller pins〉ONOFFNORMOFFDCOFFOFFInput high level voltage 1↓↓↓↓↓↓↓↓Input high level voltage 2↓↓↓↓↓↓↓↓Input low level voltage 2↓↓↓↓↓↓↓↓↓Input low level currentOFFOFFOFF↓↓↓↓↓↓↓ </td <td>Ripple rejection</td> <td>Ļ</td> <td>Ļ</td> <td>Ļ</td> <td>RIP</td> <td>ţ</td> <td>Ļ</td> <td>Ļ</td> <td>Ļ</td> <td>DC: bias voltage</td>	Ripple rejection	Ļ	Ļ	Ļ	RIP	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Output voltage FONONONONNORMOFFDCOFFOFFDC: bias voltageOutput voltage R↓↓↓↓↓↓↓↓↓↓DC: bias voltageOutput voltage range F↓↓↓↓↓↓↓↓↓DC: bias voltageOutput voltage range R↓↓↓↓↓↓↓↓DC: bias voltageLoad regulation F↓OFF↓↓↓↓↓↓DC: bias voltageLoad regulation R↓↓↓↓↓↓↓DC: bias voltageLoad regulation R↓↓↓↓↓↓↓DC: bias voltageLine regulation R↓↓↓↓↓↓↓DC: bias voltageCutput offset voltage↓↓↓↓↓↓↓DC: bias voltageOutput offset voltage↓ONOFF↓↓↓↓DC: bias voltage(Controller pins)ONONOFFNORMOFFDCOFFOFFInput low level voltage 1↓↓↓↓↓↓↓↓Input low level voltage 2↓↓↓↓↓↓↓↓Input low level voltage 2↓↓↓↓↓↓↓↓↓Input low level currentOFFOFFOFF↓↓↓ <td< td=""><td>Slew rate</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>NORM</td><td>AC</td><td>AC</td><td>AC</td><td>AC</td><td>AC: 100 Hz square wave</td></td<>	Slew rate	Ļ	Ļ	Ļ	NORM	AC	AC	AC	AC	AC: 100 Hz square wave
Output voltage RIIIIIIIIIIOutput voltage range FIIIIIIIIIDC: bias voltageOutput voltage range RIIIIIIIIDC: bias voltageOutput voltage range RIIIIIIIDC: bias voltageLoad regulation FIOFFIIIIIDC: bias voltageLoad regulation RIIIIIIIDC: bias voltageLine regulationIIIIIIIDC: bias voltageOutput offset voltageIONOFFIIIIDC: bias voltage(Controller pins)Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput low level voltage 2IIIIIIIIIIIInput low level voltage 2IIIIIIIIIIIIInput low level voltage 2IIIIIIIIIIIIIIIInput low level currentOFFOFFOFFIIIIIIIIIIIIIInput low level currentOFFOFF <t< td=""><td>(Loading drivers)</td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td></td><td></td></t<>	(Loading drivers)				1					
Output voltage range FIIIIIIIIOutput voltage range RIIIIIIIDC: bias voltageOutput voltage range RIIIIIIIDC: bias voltageLoad regulation FIOFFIIIIIDC: bias voltageLoad regulation RIIIIIIDC: bias voltageLine regulation RIIIIIIIDC: bias voltageCoutput offset voltageIONOFFIIIIDC: bias voltageOutput offset voltageIONOFFIIIIDC: bias voltageInput high level voltage 1ONONOFFNORMOFFDCOFFOFFInput high level voltage 2IIIIIIIIInput low level voltage 2IIIIIIIIInput low level voltage 2IIIIIIIIIInput low level voltage 2IIIIIIIIIInput low level currentOFFOFFOFFIIIIII	Output voltage F	ON	ON	ON	NORM	OFF	DC	OFF	OFF	DC: bias voltage
Output voltage range RIIIIIIIIDC: bias voltageLoad regulation FIOFFIIIIIDC: bias voltageLoad regulation RIIIIIIIDC: bias voltageLine regulationIIIIIIIDC: bias voltageOutput offset voltageIONOFFIIIIIIIIDC: bias voltageOutput offset voltageIONOFFIIIIIIIIDC: bias voltage(Controller pins)Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput high level voltage 2IIIIIIIIIIIIIIIIIIIIInput low level voltage 2IIIIIIIIIIIIIIIIIIIIIIIIIIIIInput low level currentOFFOFFOFFIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Output voltage R	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Load regulation FIOFFIIIIIILoad regulation RIIIIIIIIIIIDC: bias voltageLine regulation RIIIIIIIIIIIIDC: bias voltageLine regulation RIIIIIIIIIIIIIIDC: bias voltageOutput offset voltageIIONOFFIIIIIIIIDC: bias voltageOutput offset voltageIIONOFFIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Output voltage range F	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Load regulation RIIIIIIIILine regulationIIIIIIIIDC: bias voltageOutput offset voltageIIIIIIIIDC: bias voltageOutput offset voltageIONOFFIIIIIIDC: bias voltage(Controller pins)Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput low level voltage 2IIIIIIIIIIIIIIIIIInput low level voltage 2IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Output voltage range R	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Line regulationIIIIIIIIOutput offset voltageIONOFFIIIIDC: bias voltageOutput offset voltageIONOFFIIIIIIIIDC: bias voltage(Controller pins)Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput low level voltage 2IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Load regulation F	Ļ	OFF	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Output offset voltageIIIIIIIIOutput offset voltageIONOFFIIIIIIIIDC: bias voltage (brake mode)(Controller pins)Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput low level voltage 1IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Load regulation R	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Output onset voltageIONOFFIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII <t< td=""><td>Line regulation</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>ţ</td><td>Ļ</td><td>Ļ</td><td>Ļ</td><td>DC: bias voltage</td></t<>	Line regulation	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	DC: bias voltage
Input high level voltage 1ONONOFFNORMOFFDCOFFOFFInput low level voltage 1 \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow Input high level voltage 2 \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow Input low level voltage 2 \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow Input low level currentOFFOFFOFF \downarrow \downarrow \downarrow \downarrow	Output offset voltage	Ļ	ON	OFF	ţ	ţ	t	Ļ	ţ	
Input low level voltage 1 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓<	(Controller pins)						1			
Input high level voltage 2IIIIIIInput low level voltage 2IIIIIIInput low level currentOFFOFFOFFIII	Input high level voltage 1	ON	ON	OFF	NORM	OFF	DC	OFF	OFF	
Input low level voltage 2 ↓ ↓ ↓ ↓ ↓ ↓ Input low level current OFF OFF ↓ ↓ OFF ↓	Input low level voltage 1	Ļ	Ļ	Ļ	Ļ	ţ	Ļ	Ļ	Ļ	
Input low level current OFF OFF OFF ↓ ↓ OFF ↓ ↓	Input high level voltage 2	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	
•	Input low level voltage 2	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	
〈5 V regulator〉	Input low level current	OFF	OFF	OFF	Ļ	Ļ	OFF	Ļ	Ļ	
	<5 V regulator>									
Output voltage OFF OFF OFF OFF OFF OFF OFF OFF OFF	Output voltage	OFF	OFF	OFF	NORM	OFF	OFF	OFF	OFF	
Load regulation	Load regulation	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	
Line regulation	Line regulation	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	Ļ	

* When measuring drivers (excluding loading driver), CTL voltage should be under 0.5 V.

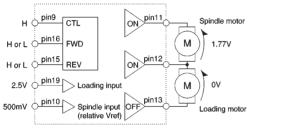
* I and IL, used in the test circuit diagram, are the same as the symbols used in electrical characteristics table.



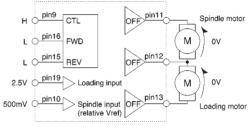
Circuit operation

(1) Switching between spindle and loading motor driver output modes (Vcc = 8V)

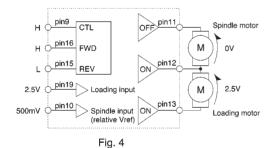
CTL	FWD	REV	Spindle		Loading	Dimentions		
		L						
с н	Н	ON		Fig. 2				
		L			OFF			
	п	н						
	1	L		OFF	High impedance	Fig. 3		
н	L	Н	OFF	ΟN	Reverse	Fig. 4		
	н	Г			Forward	Fig. 5		
		Н			Brake	Fig. 6		

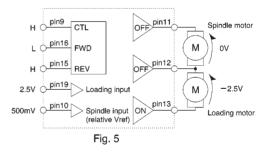


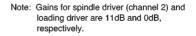


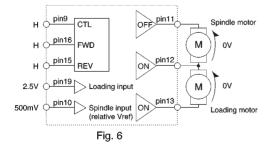






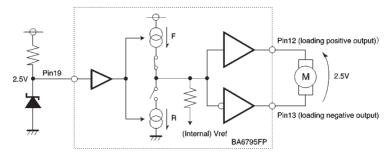






Circuit operation

(2) Loading motor driver voltage setting (forward mode)



Input voltage = output voltage (gain: 0 dB)

Note: When the loading input pin (pin 19) is opened, a voltage corresponding to the dynamic range of the power supply being used is output according to the mode.



•Application example

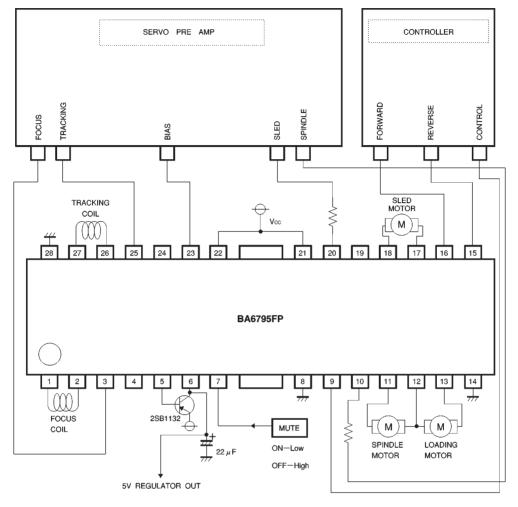


Fig.8

Operation notes

(1) The BA6795FP has an internal thermal shutdown circuit. Output current is muted when the chip temperature exceeds 175°C (typically).

(2) If the mute pin (pin 7) voltage is opened or lowered below 0.5V, the output current will be muted. Pin 7 should be pulled up above 2.0V during normal use.

(3) The bias pin (pin 23) is muted when lowered below1.4V (typically). Make sure it stays above 1.6V during normal use.

(4) Muting occurs during thermal shutdown, mute-on operations or a drop in the bias pin voltage or supply voltage. In each case, only the drivers are muted. During muting, the output pins remain at the internal bias voltage, roughly $(V_{CC}-V_F)/2$.

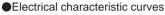
(5) The driver circuit shuts down when the supply voltage drops below 4.3V (typically), and starts up again when the voltage rises above 4.5V (typically).

(6) Fluctuation due to temperature occurs in the gain when using an attached resistor as the input resistor for a driver other than the spindle driver (typically 2200ppm per degree) or for the spindle driver (typically 4600ppm per degree. (Only when using the gain adjustment pin.)

(7) Be sure to connect the IC to a 0.1μ F bypass capacitor to the power supply, at the base of the IC.

(8) The radiating fin is connected to the package's internal GND, but should also be connected to an external ground.

(9) The capacitor between regulator output (pin 6) and GND also serves to prevent oscillation of the IC, so select one with good temperature characteristics.



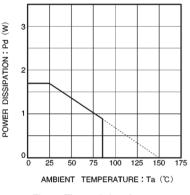


Fig. 9 Thermal derating curve

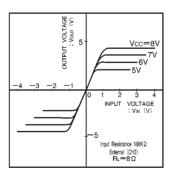


Fig. 12 Driver I / O characteristics (channel 2)

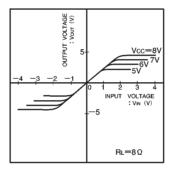


Fig. 10 Driver I / O characteristics (when load changes) (except channel 2)

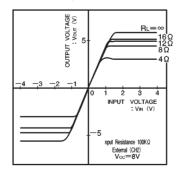


Fig. 13 Driver I / O characteristics (channel 2)

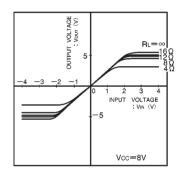


Fig. 11 Driver I / O characteristics (when power supply voltage power changes) (except channel 2)

•External dimensions (Units: mm)

