

AZ88943

High-Speed Limiting Post Amplifier

FEATURES

- Up to 2.5Gbps operation
- Differential PECL Inputs
- Differential PECL Outputs
- Open Drain TTL/CMOS SD Output
- TTL/CMOS Enable Input
- High-Speed SiGe Process

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
TSSOP 10	AZ88943T	AZ88943
TSSOP 10 T&R	AZ88943TR1	AZ88943
TSSOP 10 T&R	AZ88943TR2	AZ88943

DESCRIPTION

The AZ88943 is a limiting post amplifier usable at data rates up to 2.5Gbps. It is ideal for use as a post amplifier following a transimpedance amplifier.

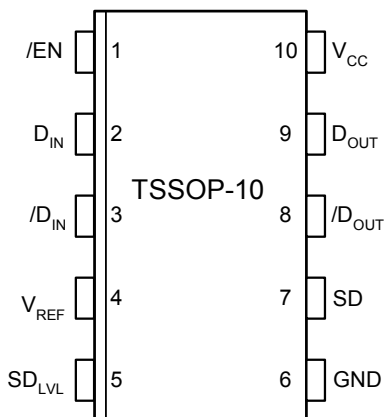
The AZ88943 contains a programmable signal detect function to determine when the input signal is present. This information can be used with the /EN input pin to disable the output under loss of signal conditions. The detect threshold can be set with a resistor divider between V_{CC} and V_{REF} . The SD output is an open drain compatible with CMOS and TTL.

The outputs produce standard PECL 100K voltage compensated levels.

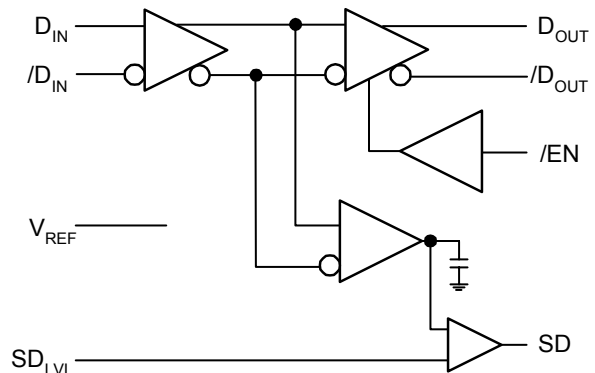
PIN DESCRIPTION

PIN	FUNCTION
D_{IN} , $/D_{IN}$	Differential Inputs
D_{OUT} , $/D_{OUT}$	PECL Outputs
/EN	Output Enable
SD_{LVL}	Signal Detect Threshold
SD	SD Output
V_{REF}	Reference Voltage Output
V_{CC}	Positive Voltage
GND	Ground

PINOUT ASSIGNMENT



BLOCK DIAGRAM



Absolute Maximum Ratings are those values beyond which device life may be impaired

Symbol	Character	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	V
T _A	Operating Temperature Range (In Free-Air)	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +125	°C
D _{IN} , /D _{IN}	Input Voltage	0 to V _{CC}	V
/EN	Input Voltage	0 to V _{CC}	V
LOS _{LVL}	Input Voltage	0 to V _{CC}	V
V _{REF}	Output Voltage	V _{CC} -2V to V _{CC}	V
D _{OUT} , /D _{OUT}	Output Voltage	V _{CC} -2V to V _{CC}	V

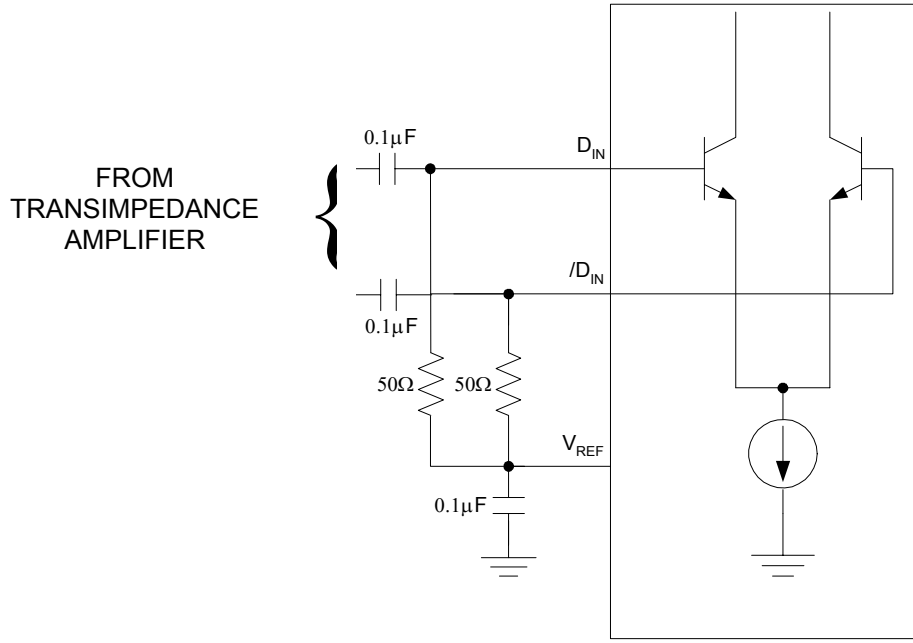
DC Characteristics (V_{CC} = 3.0V to 3.6V, R_{LOAD} = 50Ω to V_{CC}-2V)

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit
		Min	Max	Min	Max	Min	Typ	Max	Min	Max	
I _{EE}	Power Supply Current ¹		40		40		30	40		45	mA
V _{OH}	Output HIGH Voltage	V _{CC} -1085	V _{CC} -880	V _{CC} -1025	V _{CC} -880	V _{CC} -1025	V _{CC} -955	V _{CC} -880	V _{CC} -1025	V _{CC} -880	mV
V _{OL}	Output LOW Voltage	V _{CC} -1830	V _{CC} -1555	V _{CC} -1810	V _{CC} -1620	V _{CC} -1810	V _{CC} -1705	V _{CC} -1620	V _{CC} -1810	V _{CC} -1620	mV
V _{IH}	/EN Input HIGH Voltage	2.0		2.0		2.0			2.0		mV
V _{IL}	/EN Input LOW Voltage	0.8		0.8		0.8			0.8		mV
V _{OL}	SD Output LOW Voltage ²		0.5		0.5			0.5		0.5	V
V _{REF}	Reference Voltage	V _{CC} -1.38	V _{CC} -1.26	V _{CC} -1.38	V _{CC} -1.26	V _{CC} -1.38		V _{CC} -1.26	V _{CC} -1.38	V _{CC} -1.26	V
I _{IH}	/EN Input HIGH Current		100		100			100		100	μA
V _{CMR}	Common Mode Range	GND+2	V _{CC}	GND+2	V _{CC}	GND+2		V _{CC}	GND+2	V _{CC}	V

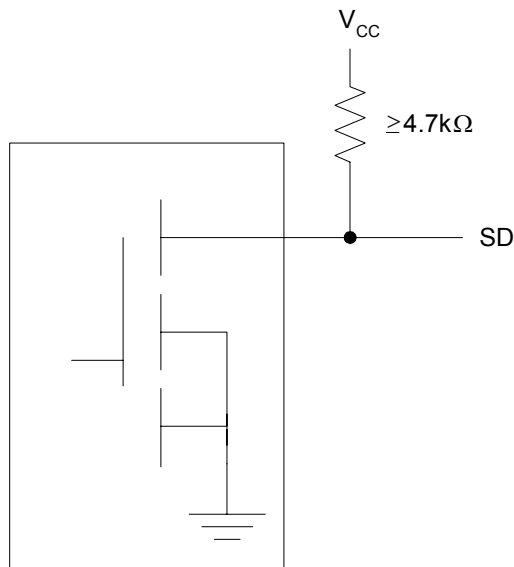
1. No output load.
2. I_{OL} = +2mA.

AC Characteristics (V_{CC} = 3.0V to 3.6V, R_{LOAD} = 50Ω to V_{CC}-2V)

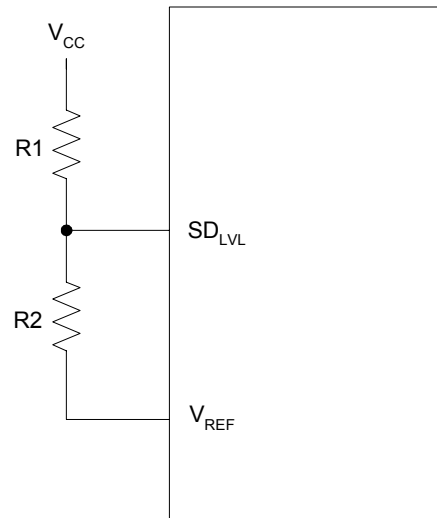
Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit
		Min	Max	Min	Max	Min	Typ	Max	Min	Max	
V _{ID}	Input Voltage Range	5	1800	5	1800	5		1800	5	1800	mV
t _r / t _f	Rise/Fall Time		150		150			150		150	ps
V _{OD}	Diff V _{ID} =15 mVp-p Out V _{ID} =5 mVp-p						600 200				MVp-p
HYS	SD Hysteresis	2	8	2	8	2	4.6	8	2	8	dB
t _{ONL}	SD Release Time Minimum Input		0.5		0.5		0.2	0.5		0.5	μs
t _{ONH}	SD Release Time Maximum Input		0.5		0.5		0.2	0.5		0.5	μs
t _{OFFL}	SD Assert Time		0.5		0.5		0.1	0.5		0.5	μs
V _{SR}	SD Sensitivity Range	5	50	5	50	5		50	5	50	MVp-p



DIFFERENTIAL INPUT CONFIGURATION



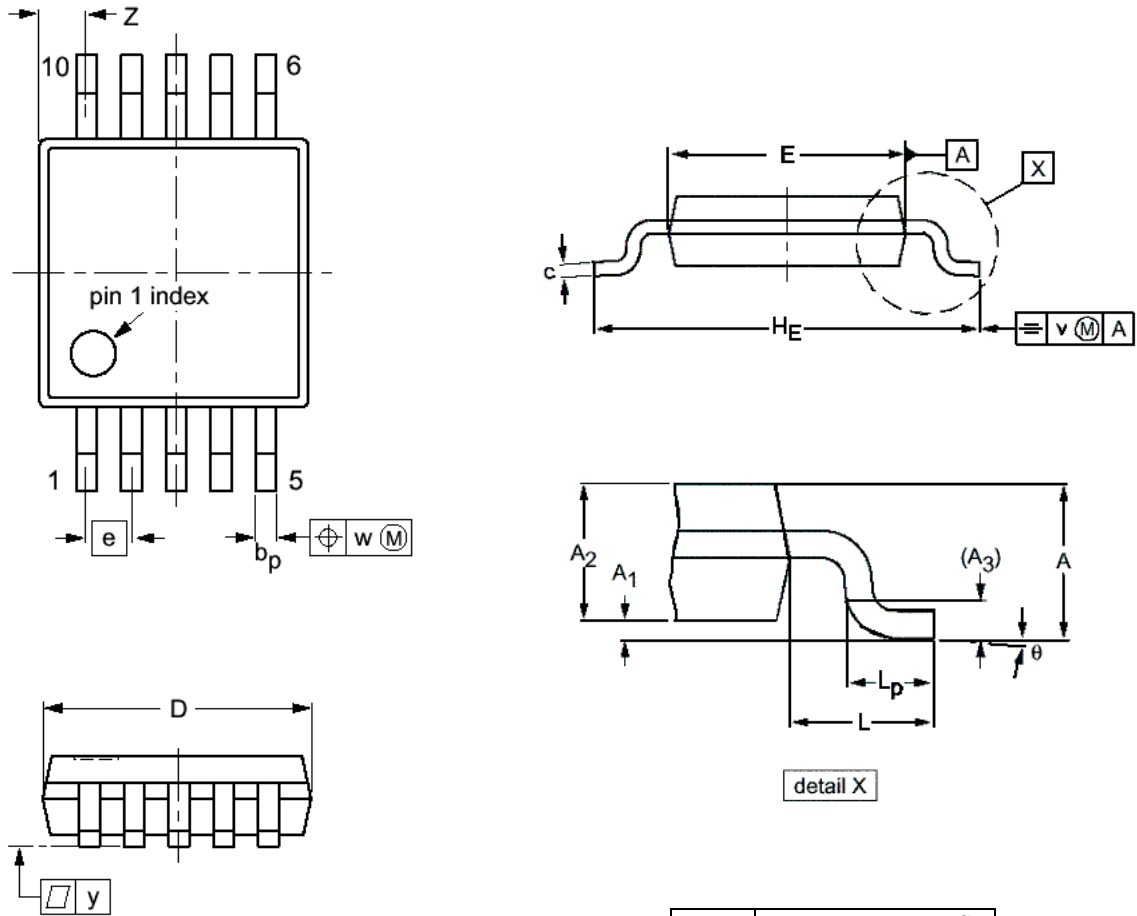
SD OUTPUT



SD_LVL CIRCUIT

NOTES:
 $SD_{LVL} = V_{CC} - 1.32V + \frac{R2 \times 1.32V}{R1 + R2}$
 $R1 + R2 \geq 2.6k\Omega$

**PACKAGE DIAGRAM
TSSOP 10**



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
 3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.80	0.95
A ₃	0.25	
b _p	0.15	0.30
c	0.15	0.23
D ¹	2.90	3.10
E ²	2.90	3.10
e	0.50	
H _E	4.80	5.00
L	0.95	
L _p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.34	0.67
θ	0°	6°

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