



MVSILICON

AU7842 USB HOST MP3/WMA DECODER SOC

AU7842 Datasheet

USB Host MP3/WMA Decoder SOC

Rev 1.0

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Revision History

| Data | Revision | Description |
|-------------|-----------------|--------------------|
| 2007-06-10 | 1.0 | Initial release |

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1. Overview

A highly integrated SOC for MP3/WMA player, AU7842 integrates MCU, MP3/WMA decoder, USB Host controller, SD/MMC card controller, a 16-bit audio decoder and an IR decoder in a single chip. Compared with traditional flash-MP3 player, AU7842 offers a lower cost, lower power consumption, flexible and more powerful Host MP3/WMA player solution.

1.1 Features

- Low power 0.18um CMOS technology
- Power supply 1.8V/3.3V, power consumption 110mW
- Enhanced 8051, up to 10 times faster than standard 8051
- USB2.0 full-speed host controller
- SD/MMC card controller
- Support MPEG 1/2/2.5 layer3 decoding, data rate 32kbps ~ 320kbps, including VBR
- Support WMA format, data rate 32kbps ~ 384kbps
- Support 9 sampling frequency:
8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 16-bit sigma-delta audio DAC
- Embedded headphone amplifier
- Support IR Remote control
- GPIO for various purposes
- Support in-system debug through external emulator
- In-system firmware upgrade through U-disk or SD/MMC

1.2 Chip Architecture

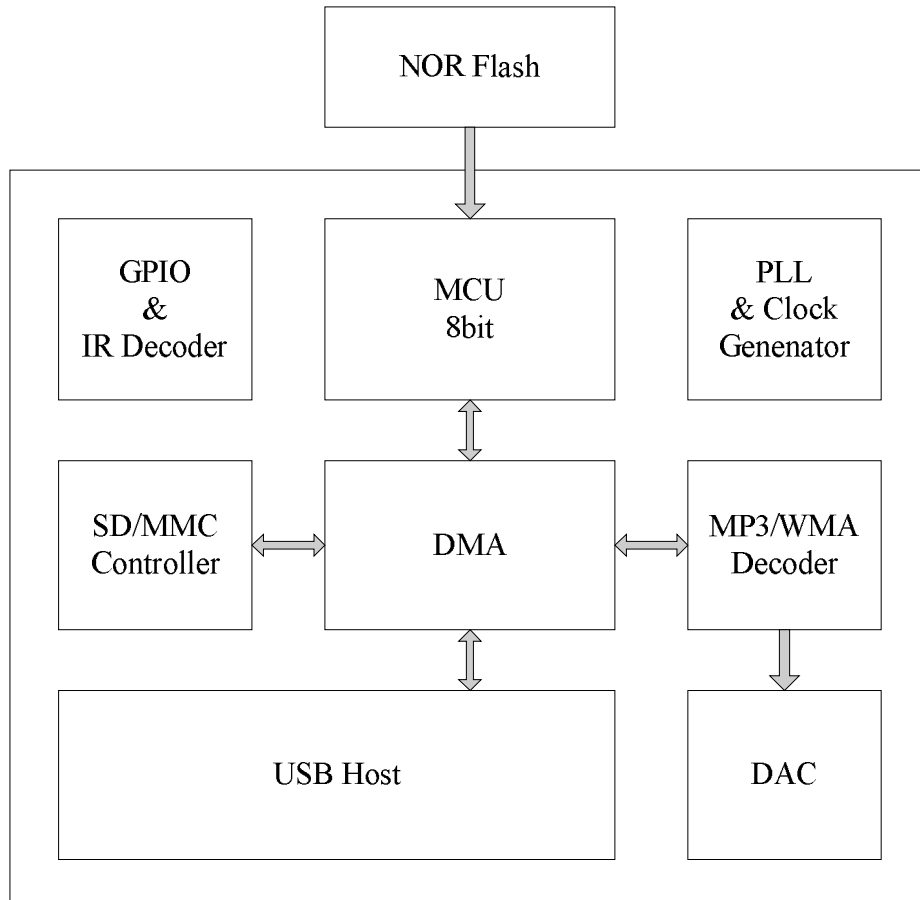


Figure 1 AU7842 Functional Block Diagram

2. System Application

- **MP3/WMA audio system**

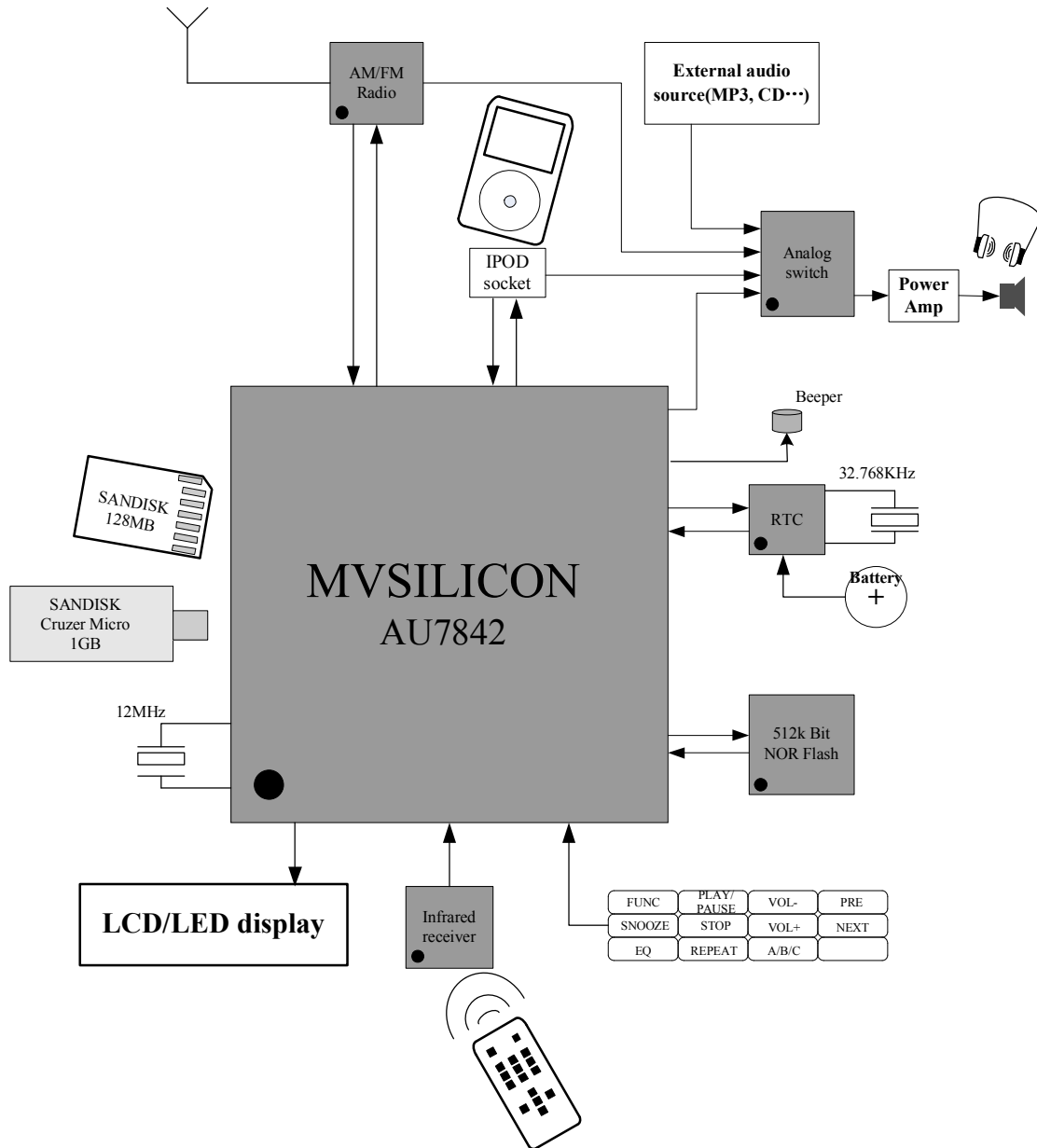


Figure 2 MP3/WMA Audio System



● MP3/WMA mini audio system

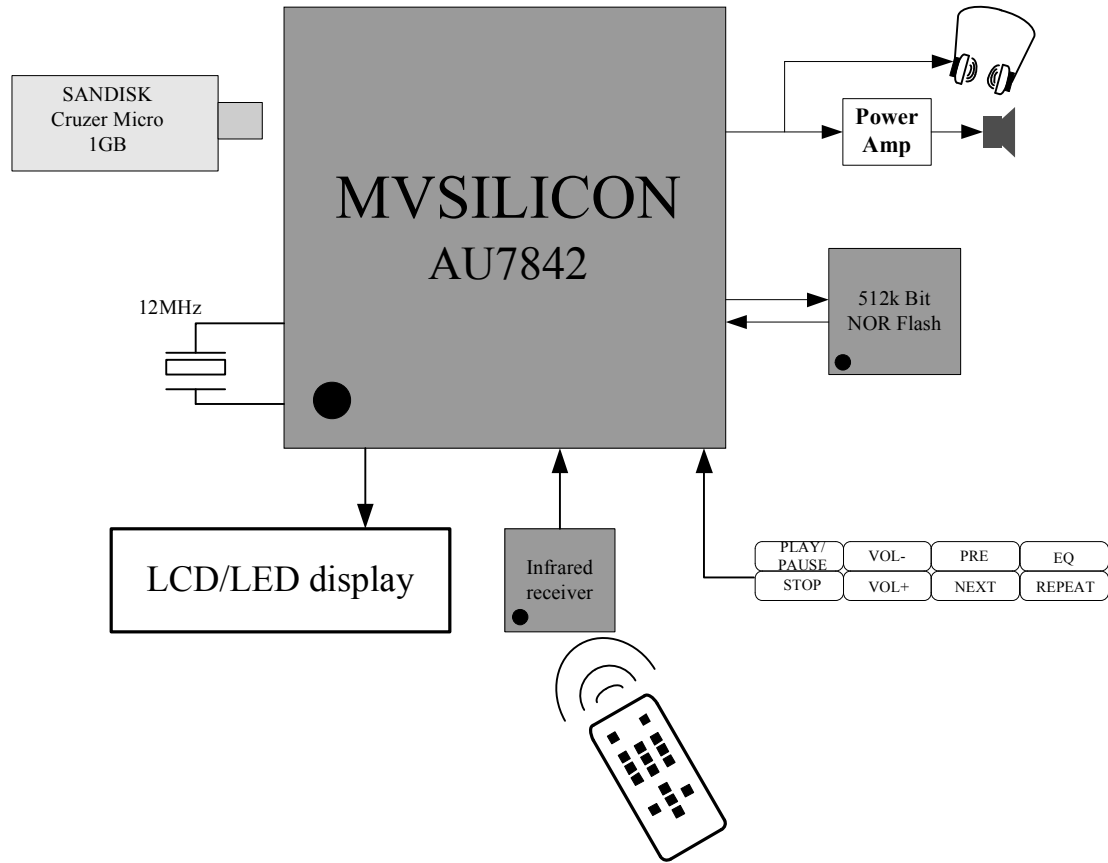


Figure 3 MP3/WMA Mini Audio System

3. Pin Description

AU7842 is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

| Notation | Description |
|----------|----------------------------------|
| I | Input |
| O | Output |
| I/O | Bidirectional |
| I/OD | Bidirectional, Open drain output |
| AI | Analog Input |
| AO | Analog Output |
| PWR | Power |
| GND | Ground |

3.1 AU7842 Pin Description

Table 1 AU7842 Pin Description

| Pin name | Pin # | Type | Description |
|--|-------|------|---------------------------|
| NOR flash memory interface pins | | | |
| FSH_DB [7:6] | 18:19 | I/O | Flash memory data bus |
| FSH_DB [5:2] | 22:25 | I/O | Flash memory data bus |
| FSH_DB [1:0] | 30:31 | I/O | Flash memory data bus |
| FSH_WR | 90 | I/O | Flash memory write signal |
| FSH_RD | 91 | I/O | Flash memory read signal |
| FSH_EN | 92 | I/O | Flash memory chip enable |
| FSH_AB[15:14] | 62:63 | I/O | Flash memory address bus |
| FSH_AB[13] | 64 | I/O | Flash memory address bus |
| FSH_AB[12] | 61 | I/O | Flash memory address bus |
| FSH_AB[11] | 67 | I/O | Flash memory address bus |
| FSH_AB[10] | 39 | I/O | Flash memory address bus |
| FSH_AB[9:8] | 66:65 | I/O | Flash memory address bus |
| FSH_AB[7:6] | 58:57 | I/O | Flash memory address bus |
| FSH_AB[5:4] | 40:41 | I/O | Flash memory address bus |
| FSH_AB[3:1] | 34:36 | I/O | Flash memory address bus |
| FSH_AB[0] | 38 | I/O | Flash memory address bus |
| USB interface pins | | | |
| USB_DP | 10 | I/O | USB Function D+ bus |
| USB_DM | 9 | I/O | USB Function D- bus |
| CARD interface pins | | | |
| SD_CLK | 51 | O | SD Card clock |



| | | | |
|---------------------------------|----------------------------------|------|---|
| SD_CMD | 53 | I/O | SD Card command line |
| SD_DAT | 54 | I/O | SD Card data line |
| Remote control pin | | | |
| IR | 75 | I | Inferred remote controller signal |
| DAC AUDIO interface pins | | | |
| DAC_HPOUTL | 3 | AO | Head phone left channel output |
| DAC_HPOUTR | 1 | AO | Head phone right channel output |
| DAC_VREF | 5 | AO | Internal voltage reference |
| GPIO/MCU IO pins | | | |
| P3[7:4] | 86:83 | I/OD | MCU P3 PORT |
| P3[3:0] | 72:69 | I/OD | MCU P3 PORT |
| P2[7:5] | 17:15 | I/OD | MCU P2 PORT |
| P2[4:3] | 87:88 | I/OD | MCU P2 PORT |
| P2[2:0] | 98:100 | I/OD | MCU P2 PORT |
| P1[7:4] | 47:44 | I/OD | MCU P1 PORT |
| P1[3:0] | 29:26 | I/OD | MCU P1 PORT |
| P0[1] | 56 | I/OD | MCU P0 PORT |
| P0[0] | 55 | I/OD | MCU P0 PORT |
| GPIO[7:3] | 80:76 | I/O | GPIO PORT |
| GPIO[2:0] | 50:48 | I/O | GPIO PORT |
| CLK & Reset pins | | | |
| XIN | 12 | I | Crystal oscillator input for PLL |
| XOUT | 13 | O | Crystal oscillator output for PLL |
| RESETn | 21 | I | System reset, active low |
| Debug pin | | | |
| DEBUG | 89 | I | When tied high, chip enter into debug mode and use external emulator. When tie low, chip works in normal mode |
| Power/Ground pins | | | |
| DAC_AVDD | 4 | PWR | Analog power for DAC(3.3V) |
| DAC_AVSS | 2 | GND | Analog ground for DAC |
| PLL_VSS | 6 | GND | Analog ground for PLL |
| PLL_VDD | 7 | PWR | Analog power for PLL(1.8V) |
| IO_VDD | 11 37 52 73 94 | PWR | Digital power for I/O(3.3V) |
| VSS | 8 20 33 42 59 81 | GND | Digital IO/core ground |
| VDD | 14 32 43 60 68 82 | PWR | Digital power for core (1.8V) |
| Reserved | 74 | | NC |



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| | | | |
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| | 97 | | |

4. Package

4.1 Package Diagram

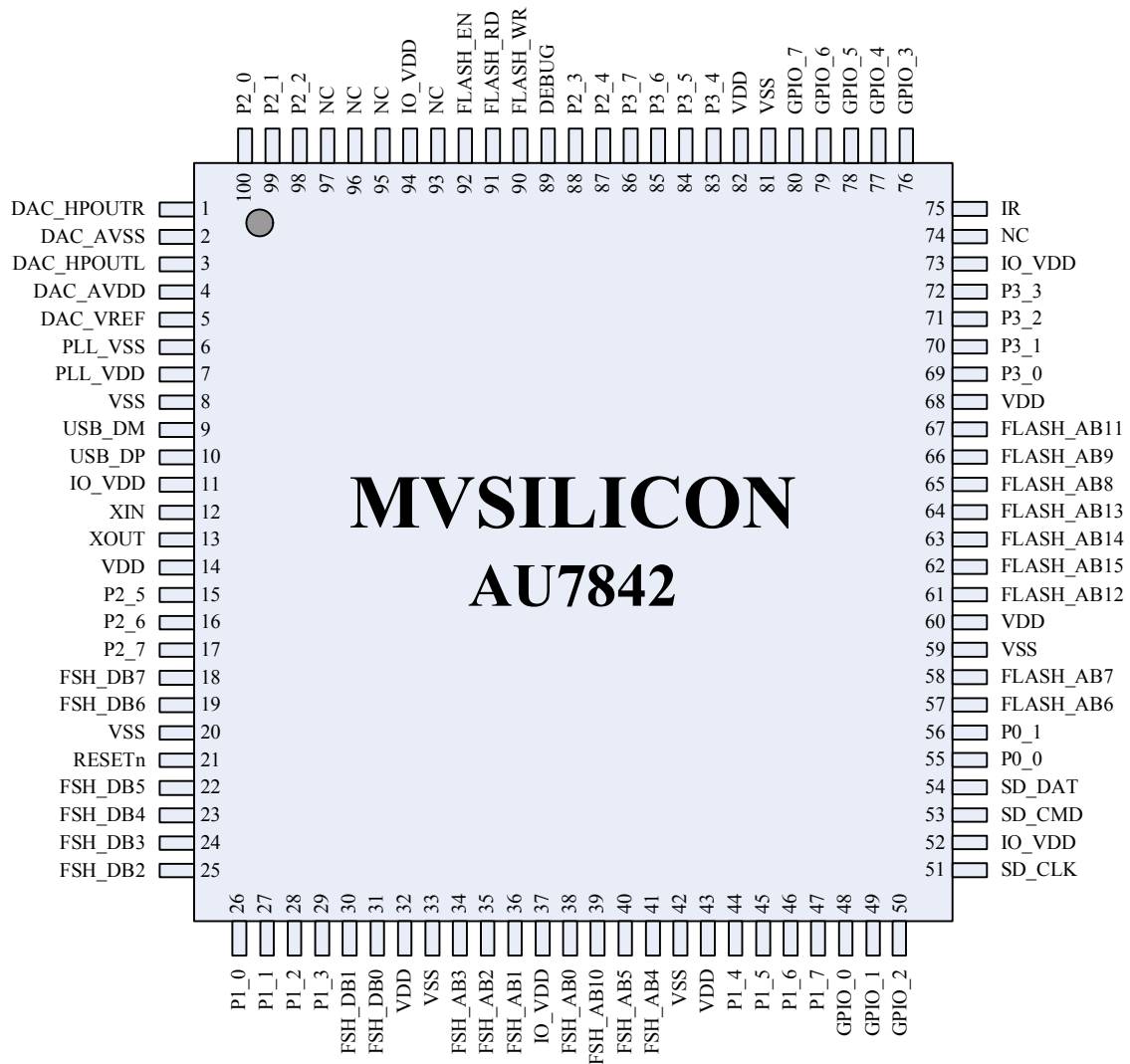


Figure 4 AU7842 Package Diagram (LQFP100-14x14mm / TOP View)

Notes: The “NC” IO in these diagrams means “not connected”, please refer to the application notes for detail.



4.2 Package Dimension Parameter

| SYMBOL | MILLIMETER | | |
|--------|------------|-------|-------|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | 0.15 | 0.25 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.54 | 0.64 | 0.74 |
| b | 0.19 | — | 0.27 |
| b1 | 0.18 | 0.20 | 0.23 |
| c | 0.13 | — | 0.18 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.80 | 14.00 | 14.20 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.80 | 14.00 | 14.20 |
| e | 0.50BSC | | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | 1.00BSC | | |
| θ | 0 | — | 8° |

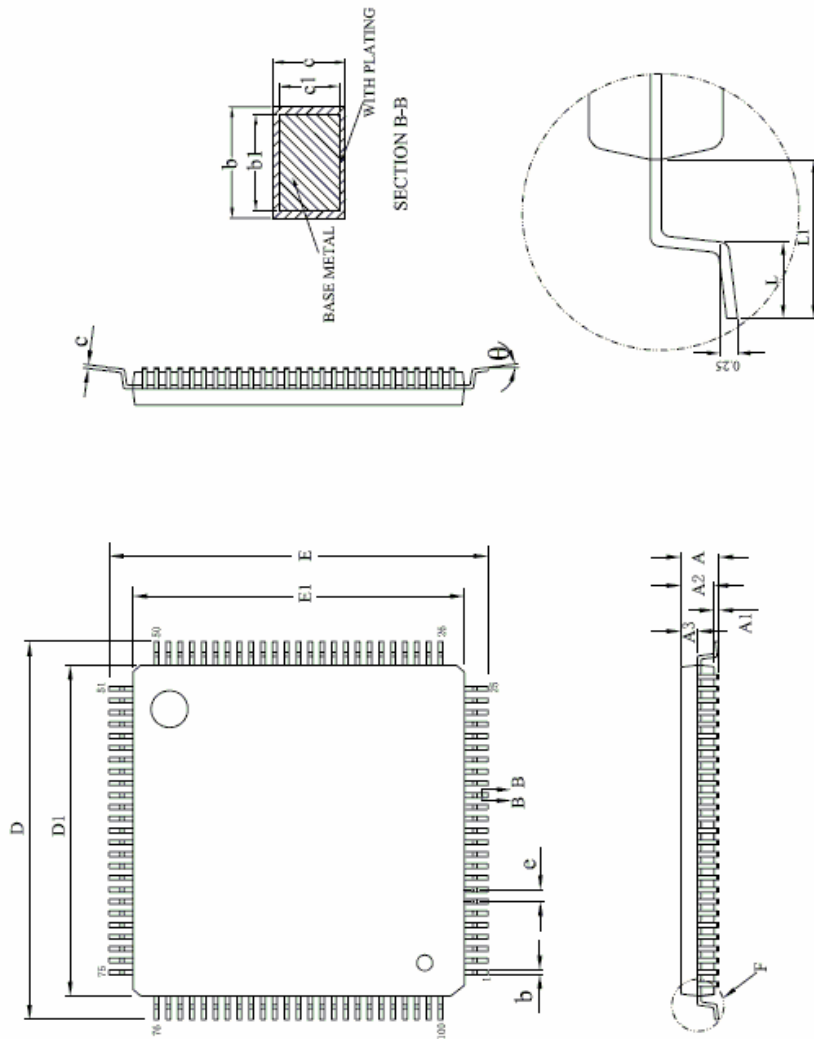


Figure 5 LQFP100-14x14mm Package Dimension Parameter

5. Electrical Specification

5.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|-----------------------------|-------------|-------------|------|
| Power Supply Voltage (IO) | VCC_IO_AB | -0.5 to 4.6 | V |
| Power Supply Voltage (Core) | VCC_CORE_AB | 0 to 2 | V |
| Power Supply Voltage (PLL) | VCC_PLL_AB | -0.2 to 2.2 | V |
| Power Supply Voltage (DAC) | VCC_DAC_AB | -0.3 to 3.6 | V |
| Storage Temperature | TEMP_STG | -20 to 125 | C |

5.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------------|-------------|------|-----|------|------|
| Power Supply Voltage (IO) | VCC_IO_OP | 3.0 | 3.3 | 3.6 | V |
| Power Supply Voltage (Core) | VCC_CORE_OP | 1.62 | 1.8 | 1.98 | V |
| Power Supply Voltage (PLL) | VCC_PLL_OP | 1.62 | 1.8 | 1.98 | V |
| Power Supply Voltage (DAC) | VCC_DAC_OP | 3.0 | 3.3 | 3.6 | V |
| Input Voltage (digital) | VIN | 0 | | 3.6 | V |
| Operating Temperature | TEMP_OPR | 0 | | 70 | C |

5.3 Electrical Characteristics

Table 4 Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-------------------|---------------------------------------|-------------------------|------|------|------|------|
| V _{IH} | Input High Voltage | | 2.0 | | 3.6 | V |
| V _{IL} | Input Low Voltage | | 0 | | 0.8 | V |
| V _{OH} | Output high voltage | @I _{OH} =2mA | 2.4 | | | V |
| V _{OL} | Output low voltage | @I _{OL} =2mA | | | 0.4 | V |
| I _{OL} | Low level output current for 8mA pins | @V _{OL} = 0.4V | 9.4 | 15.9 | 19.8 | mA |
| I _{OH} | Low level output current for 8mA pins | @V _{OH} = 2.4V | 11.2 | 23.8 | 38.3 | mA |
| I _L | Input leakage current | | -10 | | 10 | uA |
| I _{OZ} | Tri-state output leakage current | | -10 | | 10 | uA |
| P _{PLAY} | Power consumption when playing | Playing mode | | 110 | | mW |

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.



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