Li+ Charger Protection IC

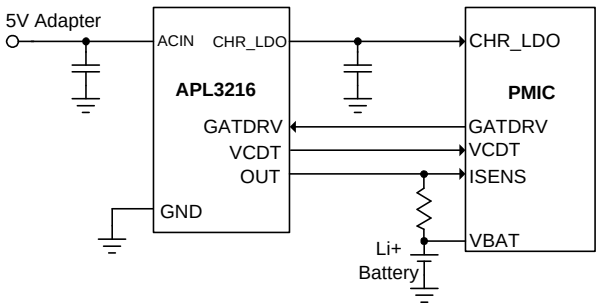
Features

- **Provide Input Over-voltage Protection**
- **Provide Input Over-current Protection**
- **Provide Over Temperature Protection**
- **Provide Reverse Current Blocking**
- **High Immunity of False Triggering**
- **High Accuracy Protection Threshold**
- **Low On Resistance 0.75Ω Typ.**
- **Compliance to IEC61000-4-2 (Level 4)**
  ±8kV (Contact Discharge)
  ±15kV (Air Discharge)
- **Available in TDFN2x2-8, SOT-23-6 Packages**
- **Lead Free and Green Devices Available**
  (RoHS Compliant)

Applications

- **Cell Phones**

Simplified Application Circuit



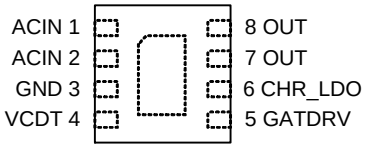
General Description

The APL3216 provides complete Li+ charger protection against Input over-voltage, input over-current and over-temperature. When any of the monitored parameters is over the threshold, the IC turns off the charging current. All protections also have deglitch time against false triggering due to voltage spikes or current transients.

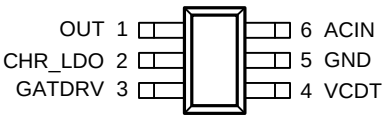
When ACIN voltage exceeds OVP threshold, the device will turn off charging current. The charging current is controlled by the GATDRV pin. When sourcing a current from the GATDRV pin, the OUT pin delivers the charging current which is 200-fold magnified in amplitude based on GATDRV's current.

Other features include accurate V_{VCDT}/V_{ACIN} Voltage divider, reverse current blocking from OUT to ACIN and OTP protection. The L3216 provides complete Li+ charger protections, that can save the external components for the charger of cell phone's PMIC. The above features and small package make the APL3216 an ideal part for cell phones applications.

Pin Configuration



TDFN2x2-8
(Top View)



SOT-23-6
(Top View)

Ordering and Marking Information

APL3216 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN2x2-8 C : SOT-23-6 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3216 QB: L16 • X	X - Date Code
APL3216 C: L16A • X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{ACIN}	ACIN Input Voltage (ACIN to GND)	-0.3 ~ 30	V
V_{CHR_LDO}	CHR_LDO to GND Voltage	-0.3 ~ 7	V
V_{GATDRV}	GATDRV to GND Voltage	-0.3 ~ V_{CHR_LDO}	V
V_{VCDT}	VCDT to GND Voltage	-0.3 ~ 7	V
V_{OUT}	OUT to GND Voltage	-0.3 ~ 7	V
I_{OUT}	OUT Output Current	Internally Limited	A
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1:Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions"is not implied. Exposure to absolute maximum rating conditions for extended periods may affect vice reliability.

Thermal Characteristic

Symbol	Parameter	Typical Value	Unit
θ_{JA}	TDFN2x2-8 Junction-to-Ambient Resistance in free air (Note 2)	80	°C/W
θ_{JA}	SOT-23-6 Junction-to-Ambient Resistance in free air (Note 2)	250	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN2x2-8 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{ACIN}	ACIN Input Voltage	4.5 ~ 9	V
I_{OUT}	Output Current	0.7	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C
C_{OUT}	Output Capacitor	0.1~1	µF

Note 3: Refer to the typical application circuit

Electrical Characteristics

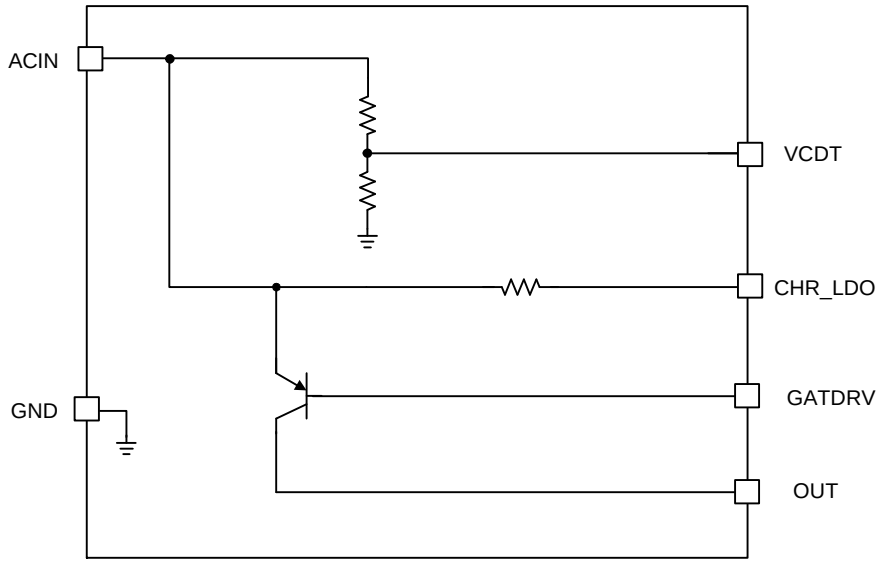
Unless otherwise specified, these specifications apply over V_{ACIN}=5V, T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3216			Unit
			Min	Typ	Max	
ACIN INPUT CURRENT and POWER-ON-RESET (POR)						
I_{ACIN}	ACIN Supply Current	I_{OUT}=0A, I_{CHR}=0A	-	250	500	µA
V_{POR}	ACIN POR Threshold	V_{ACIN} rising	-	2.6	-	V
	ACIN POR Hysteresis		-	250	-	mV
$T_{B(ACIN)}$	ACIN Power-On Blanking Time		-	8	-	ms
INTERNAL SWITCH ON RESISTANCE						
	ACIN to OUT On Resistance	I_{OUT}=0.6A		750		mΩ
	CHR_LDO Discharge Resistance		-	500	-	Ω
PROTECTIONS						
I_{CL}	Over-current Trip Threshold		0.9	1.25	1.6	A
-	Short-circuit Current Limit		-	0.75	-	
-	Input OVP Threshold		9.5	10	10.5	V
-	CHR_LDO Output Series Resistance		2.4	3	-	kΩ
VCDT INTERNAL DIVIDER						
	Divider Ratio	V_{VCDT} /V_{ACIN}	0.1035	0.1056	0.1078	V/V
CHARGE CURRENT CONTROL						
	Current Mirror Gain	I_{OUT}=0.6A, I_{OUT}/I_{GATDRV}	100	200	300	A/A
THERMAL SHUTDOW PROTECTION						
TOTP	Thermal Shutdown Threshold	T_J rising	-	160	-	°C
	Thermal Shutdown Hysteresis		-	40	-	°C

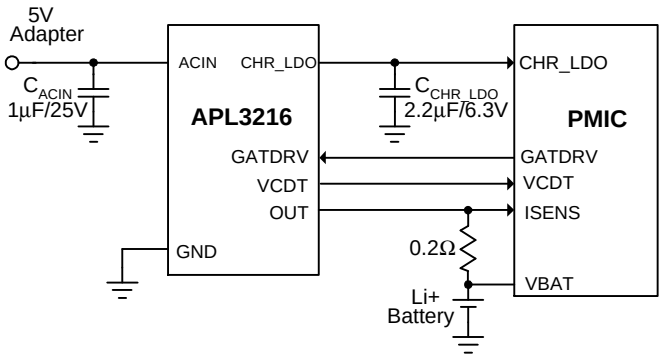
Pin Description

PIN			Function
TDFN2x2-8	SOT-23-6		
NO.	NO.	NAME	
1	6	ACIN	Power Supply Input. Connect this pin to external DC supply. Bypass to GND with a 1µF (minimum) ceramic capacitor.
2			
3	5	GND	Ground terminal.
4	4	VCDT	Provide an internal voltage divider. This pin divides ACIN voltage into 0.1056 ratio.
5	3	GATDRV	Charging current control pin. When sinking a current from this pin, the OUT pin will source out a current whose magnitude is 200x I_{GATDRV}.
6	2	CHR_LDO	Output Pin. The pin provides supply voltage to the PMIC input. Bypass to GND with a 1µF (minimum) ceramic capacitor.
7	1	OUT	Output Pins. The pin provides supply source current in series with a resistor to battery.
8			
Exposed Pad	-	GND	Exposed Thermal Pad. Must be electrically connected to the GND pin.

Block Diagram



Typical Application Circuit



Designation	Description
C_{ACIN}	1µF, 25V, X5R, 0603 Murata GRM188R61E105K
	1µF, 16V, X5R, 0603 Murata GRM188R61C105K
C_{CHR_LDO}	1µF, 6.3V, X5R, 0603 Murata GRM185R60J225KE26

Function Description

ACIN Power-On-Reset (POR)

The APL3216 is built-in a power-on-reset circuit to keep the output shut off until internal circuitry is operating properly. The POR circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the POR threshold and after 8ms blanking time, the output voltage starts a soft-start to reduce the inrush current.

ACIN Over-Voltage Protection (OVP)

The CHR_LDO output of the IC operates similar to a linear regulator. If the input voltage rises above V_{OVP}, the internal transistor will be turned off within 5µs to protect connected system on OUT pin. When the input voltage returns below the input OVP threshold minus the hysteresis, the transistor is turned on again after 1ms recovery time. The input OVP circuit has a 200mV hysteresis and a recovery time of $T_{ON(OVP)}$ to provide noise immunity against transient conditions.

Charging Current Control

The charging current is controlled by the GATDRV pin. When sourcing a current from the GATDRV pin, the OUT pin delivers the charging current which is 200-fold magnified in amplitude based on GATDRV?¡s current. The I_{OUT} current can be calculated by this following equation:

$$I_{OUT}=200*I_{GATDRV}$$

where
The I_{OUT} is the current flowing out from OUT pin.
The I_{GATDRV} is the current flowing out from GATDRV pin.

Current Limit

The output current is monitored by the internal Current Limit circuit. When the output current reaches the over current trip threshold, the device limits the output current at current limit threshold.

Temperature Protection

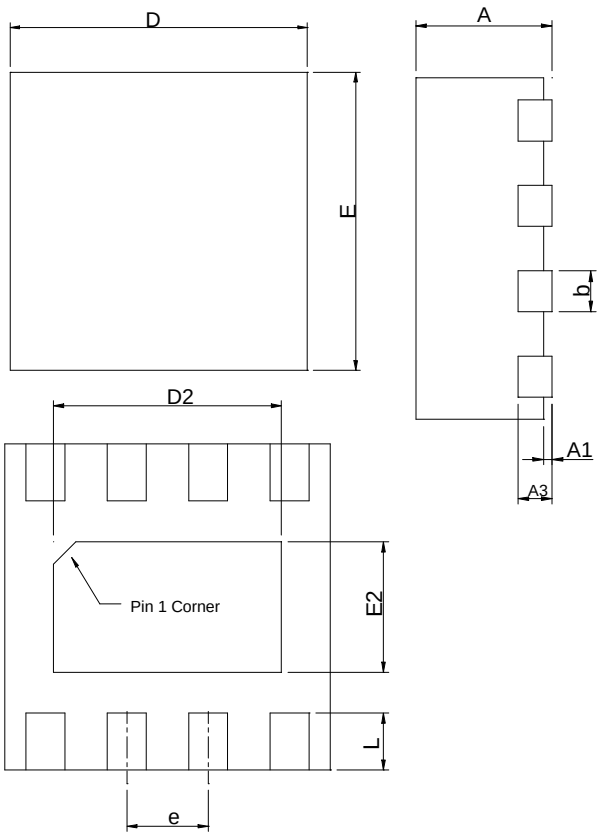
When the junction temperature exceeds 160°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

ESD Tests

The APL3216 VIN input pin fully supports the IEC61000-4-2. That means the VIN pin has immunity of ±15kV ESD discharge in Air condition, and immunity of ±8kV ESD discharge in Contact condition.

Package Information

TDFN2x2-8

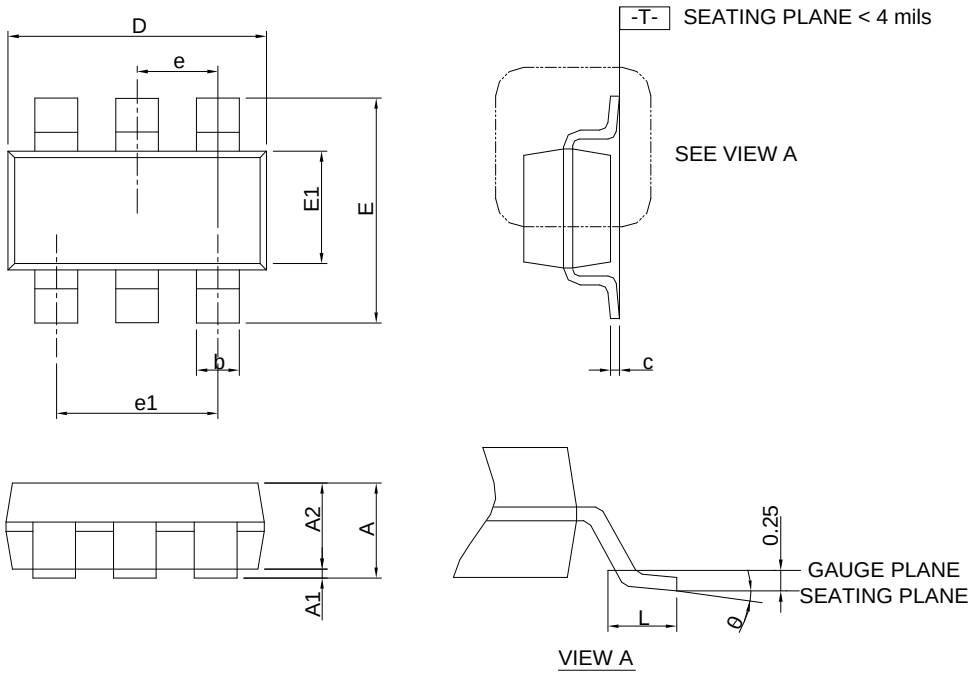


SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018

Note : 1. Follow from JEDEC MO-229 WCCD-3.

Package Information

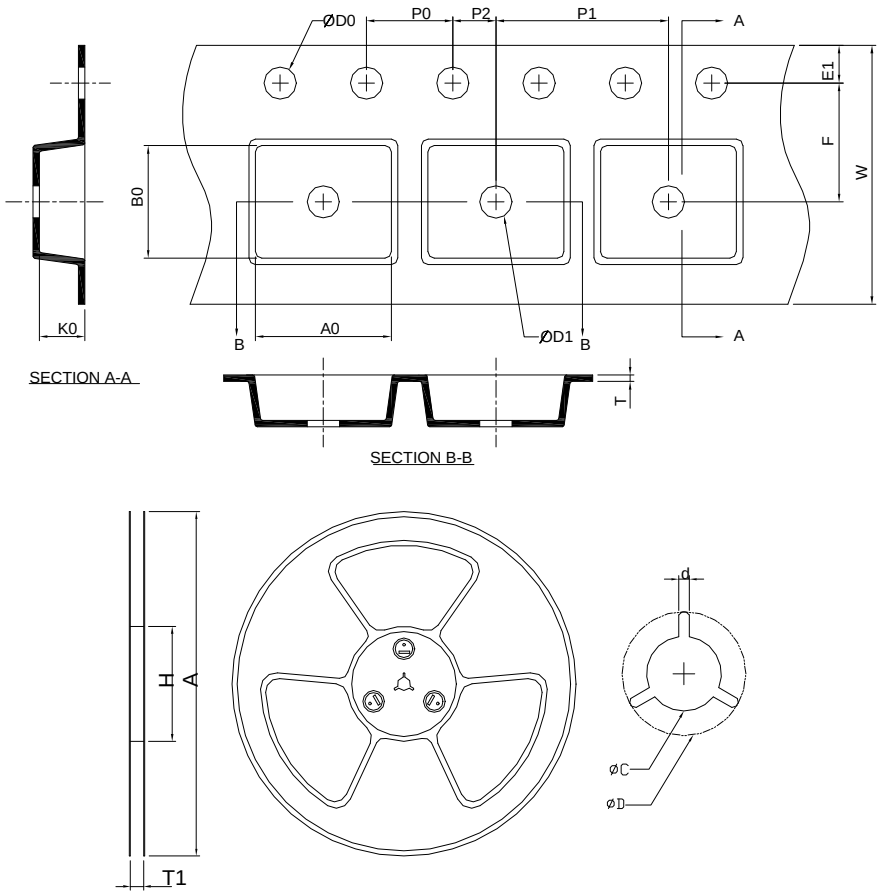
SOT-23-6



SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20
SOT-23-6	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

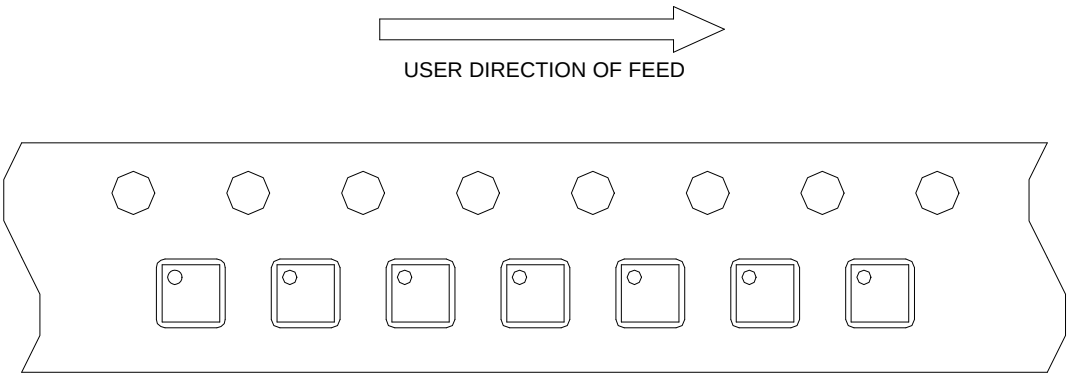
(mm)

Devices Per Unit

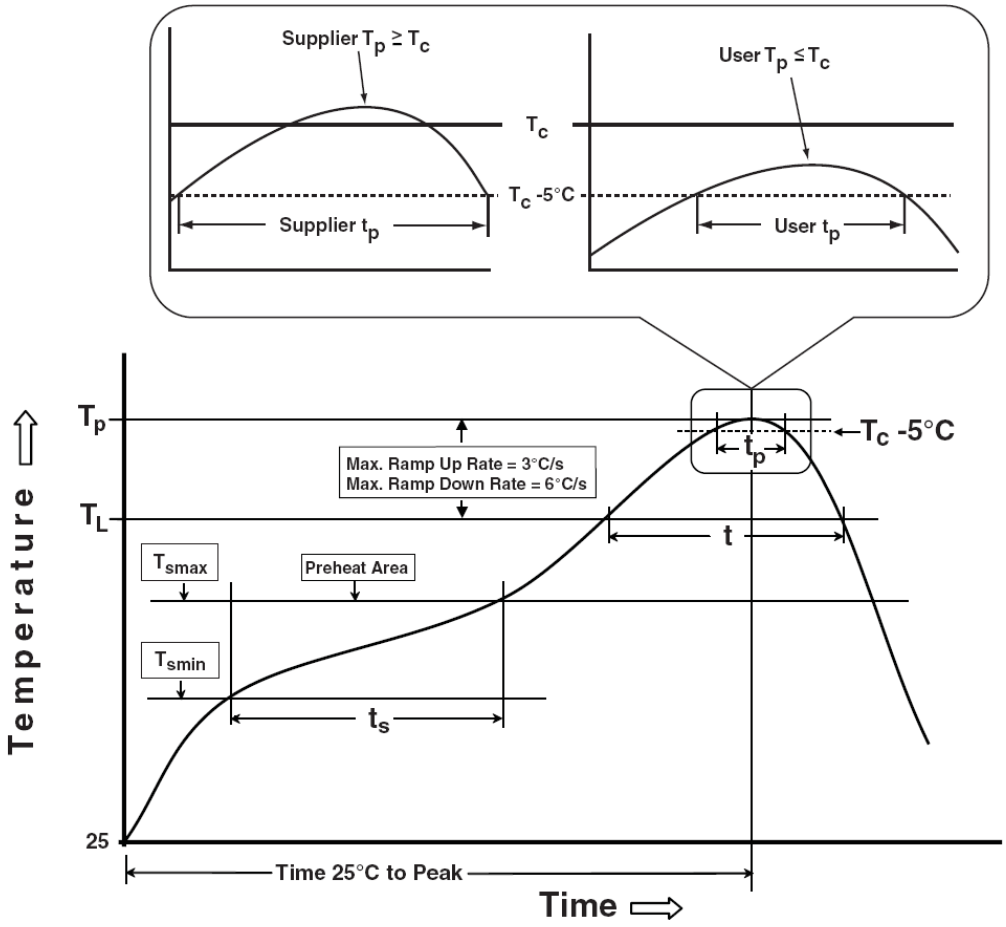
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000
SOT-23-6	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	JESD-22, A114; A115	VHBM≧2KV, VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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