

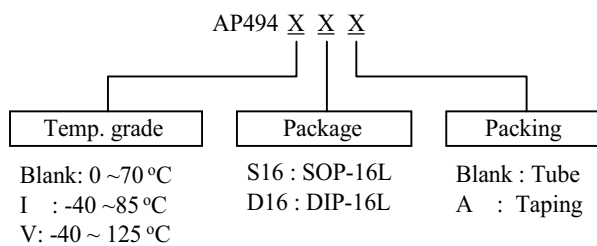
AP494

Voltage Mode PWM Controller

■ Features

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply with 3% Tolerance
- Circuit Architecture allows Easy Synchronization

■ Ordering Information



■ Description

The AP494 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, this device offers the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

The AP494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 3%-precision regulator, and output-control circuits.

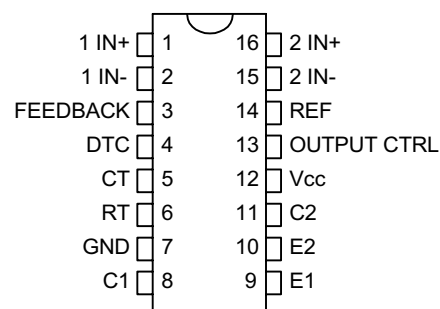
The error amplifiers exhibit a common-mode voltage range from $-0.3V$ to $V_{CC} - 2V$. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator may be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it may drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The AP494 provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The AP494 is characterized for operation from 0°C to 70°C.

■ Connection Diagram

(TOP VIEW)

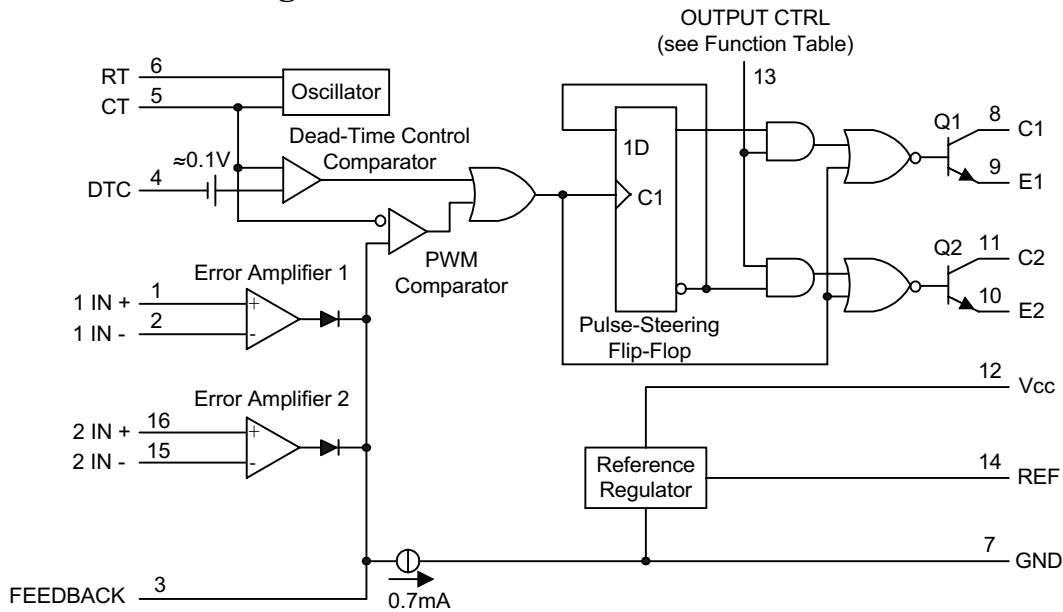


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Functional Block Diagram



Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Collector Output Voltage	V_{C1}, V_{C2}	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	500	mA
Amplifier Input Voltage Range	V_{IR}	-0.3 to +40	V
Power Dissipation @ $T_A \leq 45^\circ\text{C}$	P_D	1000	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Operating Junction Temperature	T_J	125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Derating Ambient Temperature	T_A	45	$^\circ\text{C}$

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	-	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	-	-	200	mA
Amplified Input Voltage	V_{in}	-0.3	-	$V_{CC}-2.0$	V
Current Into Feedback Terminal	I_{fb}	-	-	0.3	mA
Reference Output Current	I_{ref}	-	-	10	mA
Timing Resistor	R_T	1.8	30	500	$k\Omega$
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{OSC}	1.0	40	200	kHz

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■ Electrical Characteristics

($V_{CC}=15V$, $C_T=0.01\mu F$, $R_T=12\text{ k}\Omega$, unless otherwise noted.) For typical values $T_A=25^\circ C$, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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REFERENCE SECTION

Reference Voltage ($I_O=1.0\text{mA}$)	I_{ref}	4.85	5.0	5.15	V
Line Regulation ($V_{CC}=7.0\text{ V to }40\text{V}$)	Reg_{line}	-	2.0	25	mV
Load Regulation ($I_O=1.0\text{mA to }20\text{mA}$)	Reg_{load}	-	3.0	15	mA
Short Circuit Output Current ($I_{ref}=0\text{ V}$)	I_{SC}	4.5	60	75	mA

OUTPUT SECTION

Collector Off-State Current ($V_{CC}=40\text{V}$, $V_{CE}=40\text{V}$)	$I_{C(off)}$	-	2.0	100	μA
Emitter Off-State Current ($V_{CC}=40\text{V}$, $V_C=40\text{V}$, $V_E=0\text{V}$)	$I_{E(off)}$	-	-	-100	μA
Collector-Emitter Saturation Voltage (Note 1) Common-Emitter ($V_E=0\text{V}$, $I_C=200\text{mA}$)	$V_{sat(C)}$	-	1.1	1.5	V
Emitter-Follower ($V_C=15\text{V}$, $I_E=-200\text{mA}$)	$V_{sat(E)}$	-	1.5	2.5	
Output Control Pin Current Low State ($V_{OC}\leq 0.4\text{V}$)	I_{OCL}	-	10	-	μA
High State ($V_{OC}=V_{ref}$)	I_{OCH}	-	0.2	3.5	mA
Output Voltage Rise Time Common-Emitter (See Figure 4) Emitter-Follower (See Figure 5)	t_r	-	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 4) Emitter-Follower (See Figure 5)	t_f	-	25	100	ns

NOTE: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ERROR AMPLIFIER SECTION

Input Offset Voltage ($V_{O(Pin\ 3)}=2.5\text{V}$)	V_{IO}	-	2.0	10	mV
Input Offset Current ($V_{O(Pin\ 3)}=2.5\text{V}$)	I_{IO}	-	5.0	250	nA
Input Bias Current ($V_{O(Pin\ 3)}=2.5\text{V}$)	V_{IB}	-	-0.1	-0.1	μA
Input Common Mode Voltage Range ($V_{CC}=40\text{V}$, $T_A=25^\circ C$)	I_{ICR}	-0.3 to $V_{CC}-2.0$			V
Open Loop Voltage Gain ($\Delta V_O=3.0\text{V}$, $V_O=0.5\text{V to }3.5\text{V}$, $R_L=2.0\text{ k}\Omega$)	A_{VOL}	70	95	-	dB
Unity-Gain Crossover Frequency ($V_O=0.5\text{V to }3.5\text{V}$, $R_L=2.0\text{ k}\Omega$)	f_c	-	350	-	kHz
Common Mode Rejection Ratio ($V_{CC}=40\text{V}$)	CMRR	64	90	-	dB
Output Sink Current ($V_{O(Pin\ 3)}=0.7\text{V}$)	I_{O-}	0.3	0.7	-	mA
Output Source Current ($V_{O(Pin\ 3)}=3.5\text{V}$)	I_{O+}	-10	-15	-	mA

PWM COMPARATOR SECTION (Test Circuit Figure 1)

Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	-	2.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}=0.7\text{V}$)	I_L	0.3	0.7	-	mA

DEADTIME CONTROL SECTION (Test Circuit Figure 1)

Input Bias Current (Pin 4) ($V_{Pin4}=0\text{V to }5.25\text{V}$)	$I_{IB(DT)}$	-	-2.0	-10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin4}=0\text{V}$, $C_T=0.01\mu F$, $R_T=12\text{ k}\Omega$)	DC_{max}	45	48	50	%
Input Threshold Voltage (Pin4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{th}	-	2.8	3.3	V
		0	-	-	

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OSCILLATOR SECTION

Frequency ($C_T=0.01\mu\text{F}, R_T=12\text{ k}\Omega$)	f_{OSC}	-	10	-	kHz
Standard Deviation of Frequency* ($C_T=0.001\mu\text{F}, R_T=30\text{ k}\Omega$)	σf_{OSC}	-	3.0	-	%
Frequency Change with Voltage ($V_{\text{CC}}=7.0\text{V to }40\text{V}, T_A=25^\circ\text{C}$)	$\Delta f_{\text{OSC}} (\Delta V)$	-	0.1	-	%
Frequency Change with Temperature ($\Delta T_A=T_{\text{low}} \text{ to } T_{\text{high}}$) ($C_T=0.01\mu\text{F}, R_T=12\text{ k}\Omega$)	$\Delta f_{\text{OSC}} (\Delta T)$	-	-	12	%

TOTAL DEVICE

Standby Supply Current (Pin6 at V_{ref} , All other inputs and outputs open) ($V_{\text{CC}}=15\text{V}$) ($V_{\text{CC}}=40\text{V}$)	I_{CC}	-	5.5 7.0	10 15	mA
Average Supply Current ($C_T=0.01\mu\text{F}, R_T=12\text{ k}\Omega, V_{(\text{pin}4)}=2.0\text{V}$) ($V_{\text{CC}}=15\text{V}$) (See Figure 4)		-	7.0	-	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, σ

$$\sigma = \sqrt{\frac{\sum_{n=1}^N (X_n - \bar{X})^2}{N-1}}$$

Figure 1. PARAMETER MEASUREMENT INFORMATION

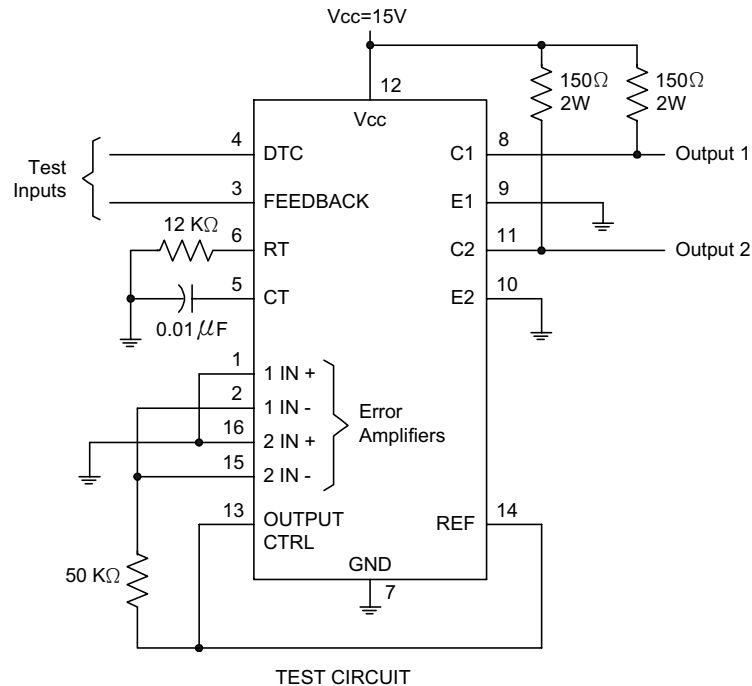


Figure 2. OPERATIONAL TEST CIRCUIT AND WAVEFORMS

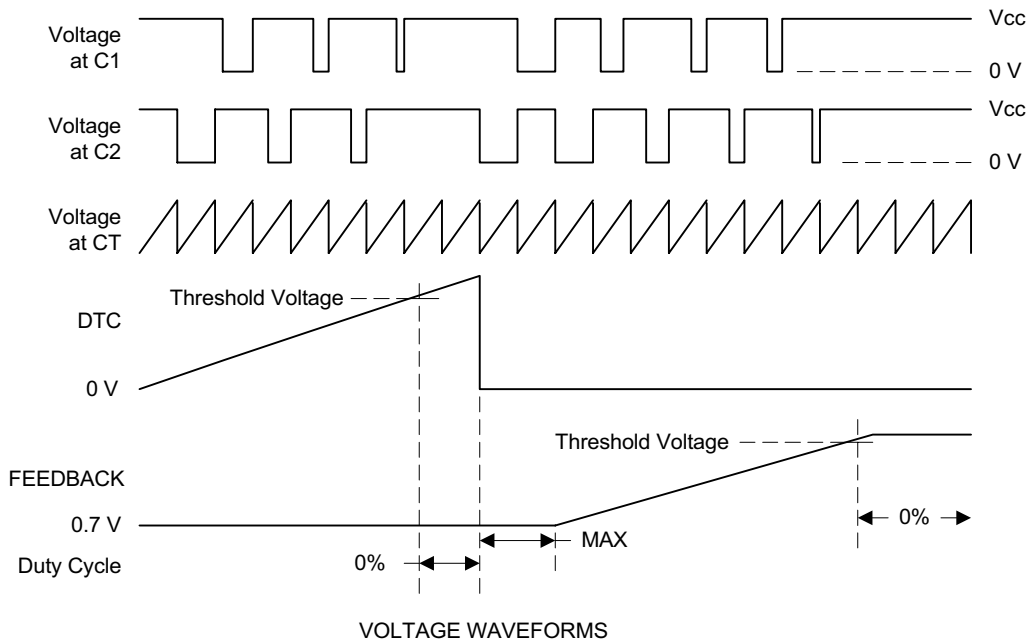


Figure 3. AMPLIFIER CHARACTERISTICS

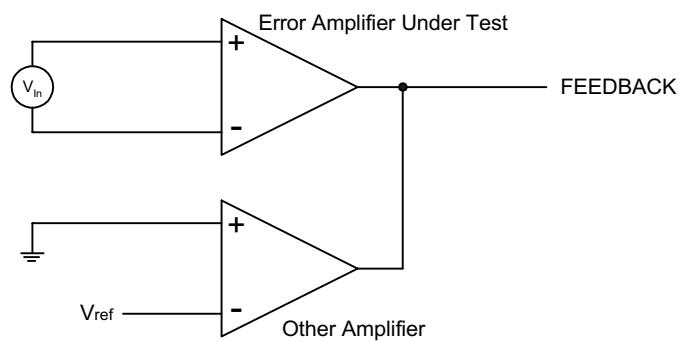
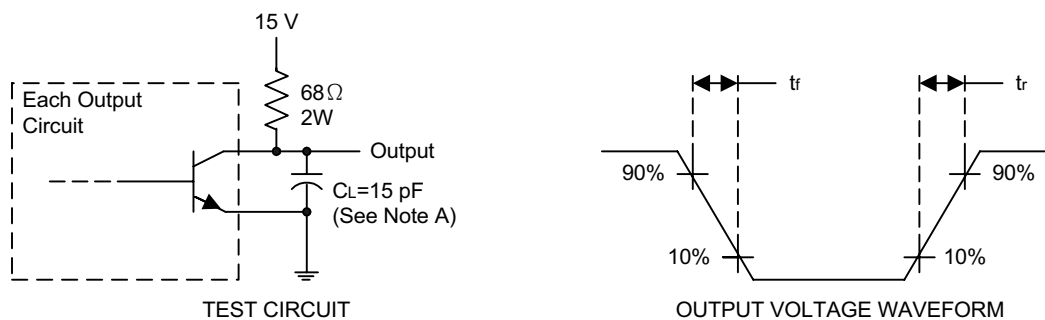
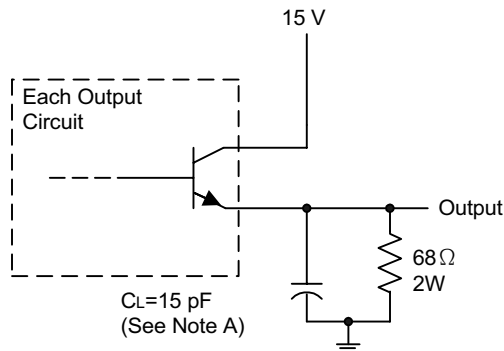


Figure 4. COMMON-EMITTER CONFIGURATION



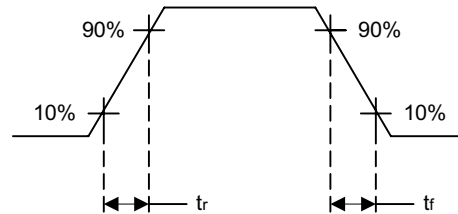
NOTE A. C_L includes probe and jig capacitance.

Figure 5. EMITTER-FOLLOWER CONFIGURATION



TEST CIRCUIT

NOTE A. CL includes probe and jig capacitance.



OUTPUT VOLTAGE WAVEFORM

Figure 6.

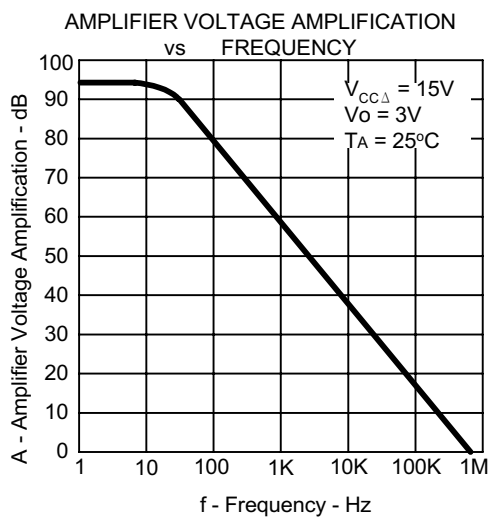


Figure 8.

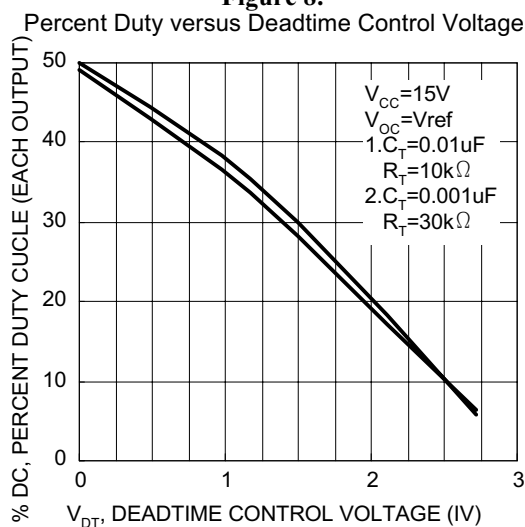


Figure 7.

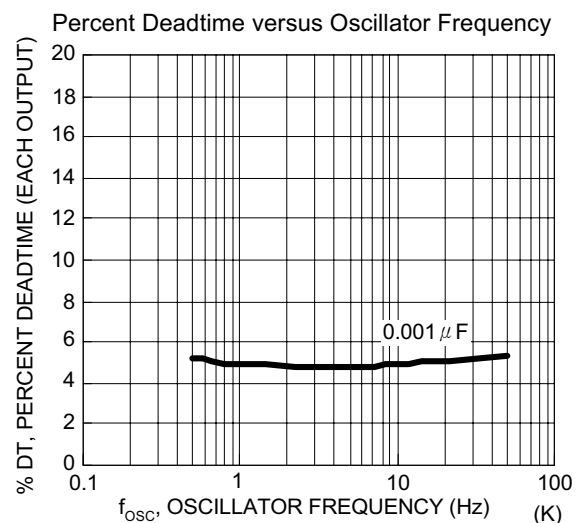


Figure 9.

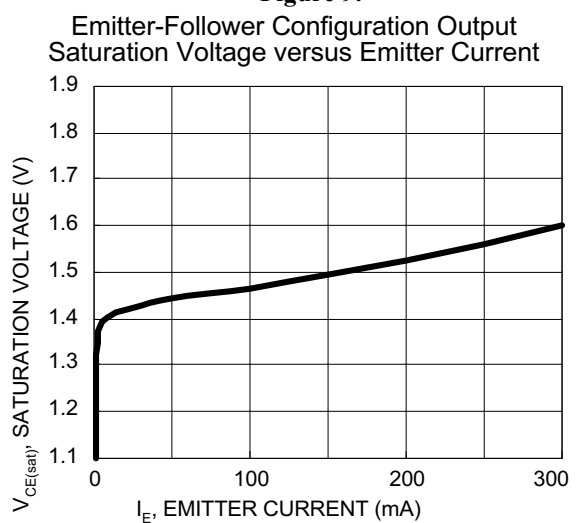


Figure 10.

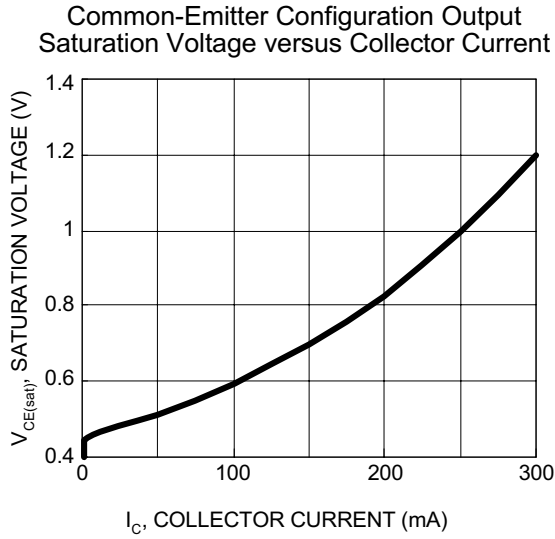


Figure 11.

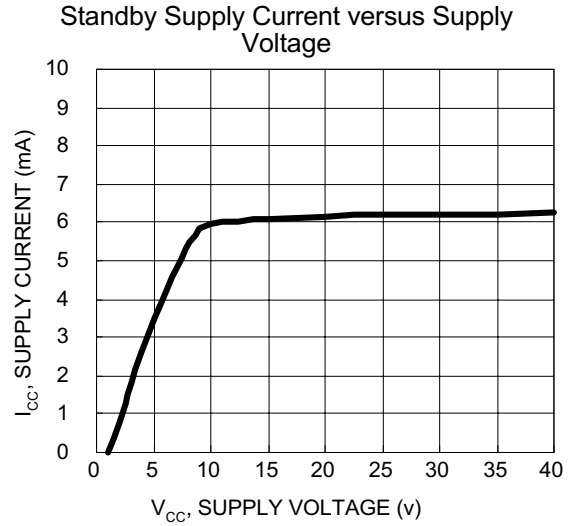
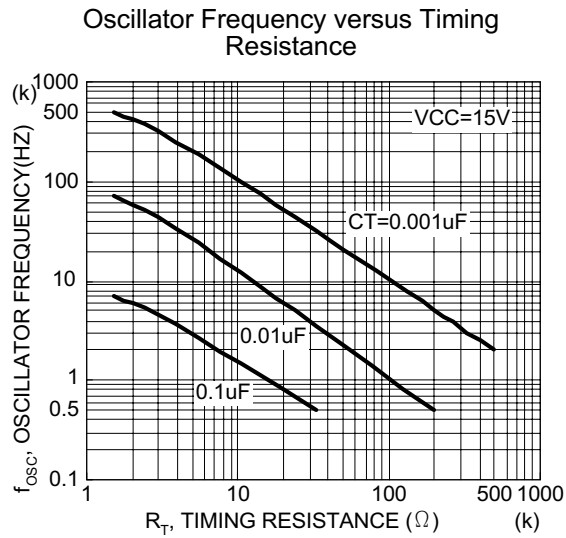


Figure 12.



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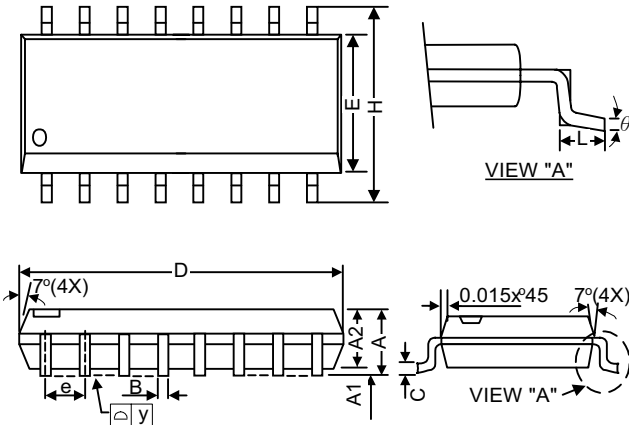
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■ Package Dimension

(1) SOP-16L

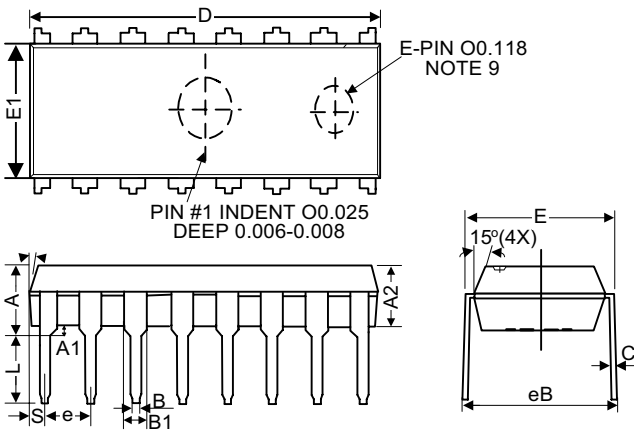
Package Dimension



Symbols	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.010
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.007 5	0.008	0.009 8
D	9.80	9.91	10.01	0.386	0.390	0.394
E	3.80	3.91	4.00	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
Θ	0	-	8	0	-	8

(2) PDIP-16L

Package Dimension



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	*	*	5.33
A1	0.38	*	*
A2	3.1	3.3	3.5
B	0.36	0.46	0.56
B1	1.4	1.52	1.65
B2	0.81	0.99	1.14
C	0.2	0.25	0.36
D	18.9	19.10	19.30
E	7.62	7.94	8.26
E1	6.15	6.35	6.55
e	*	2.54	*
L	2.92	3.3	3.81
eB	8.38	8.89	9.4
S	0.71	0.84	0.97