# High-Frequency, High-Efficiency Buck Converter Design For Multi-Cell Battery Configured Systems Using Si9167

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## INTRODUCTION

The Si9167 is a high-frequency synchronous dc-to-dc switching buck regulator, with an operating range suitable for two-cell Li+ battery-powered applications. Capable of operation up to 2 MHz, the Si9167 can be used to supply power amplifiers and to power up baseband circuits in satellite phones. Its high operating frequency reduces the size of inductor and capacitor components, while its low on-resistance internal driver ensures maximum power conversion efficiency. Additional features include an integrated input undervoltage lockout, power on reset, integrated soft start, light load pulse skipping mode selection, synchronization, clock output for master-slave configuration of multiple regulators, uncommitted power-good comparator, and over temperature protection. An output power in excess of 2 W at 3.6 $V_O$ is possible in 0.3 square inches.

## TYPICAL APPLICATION CIRCUIT

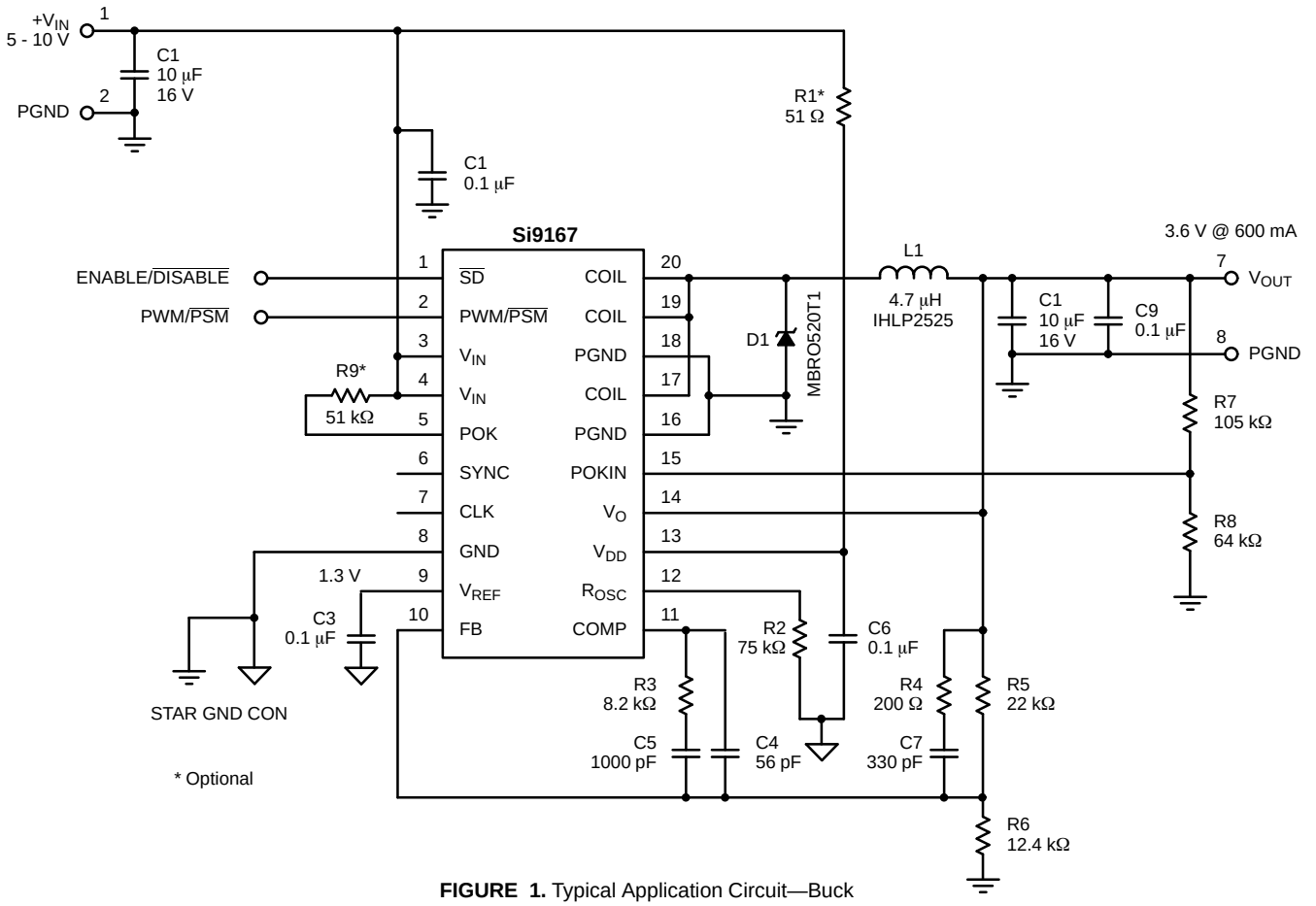



**FIGURE 1.** Typical Application Circuit—Buck

## FUNCTIONAL BLOCK DIAGRAM

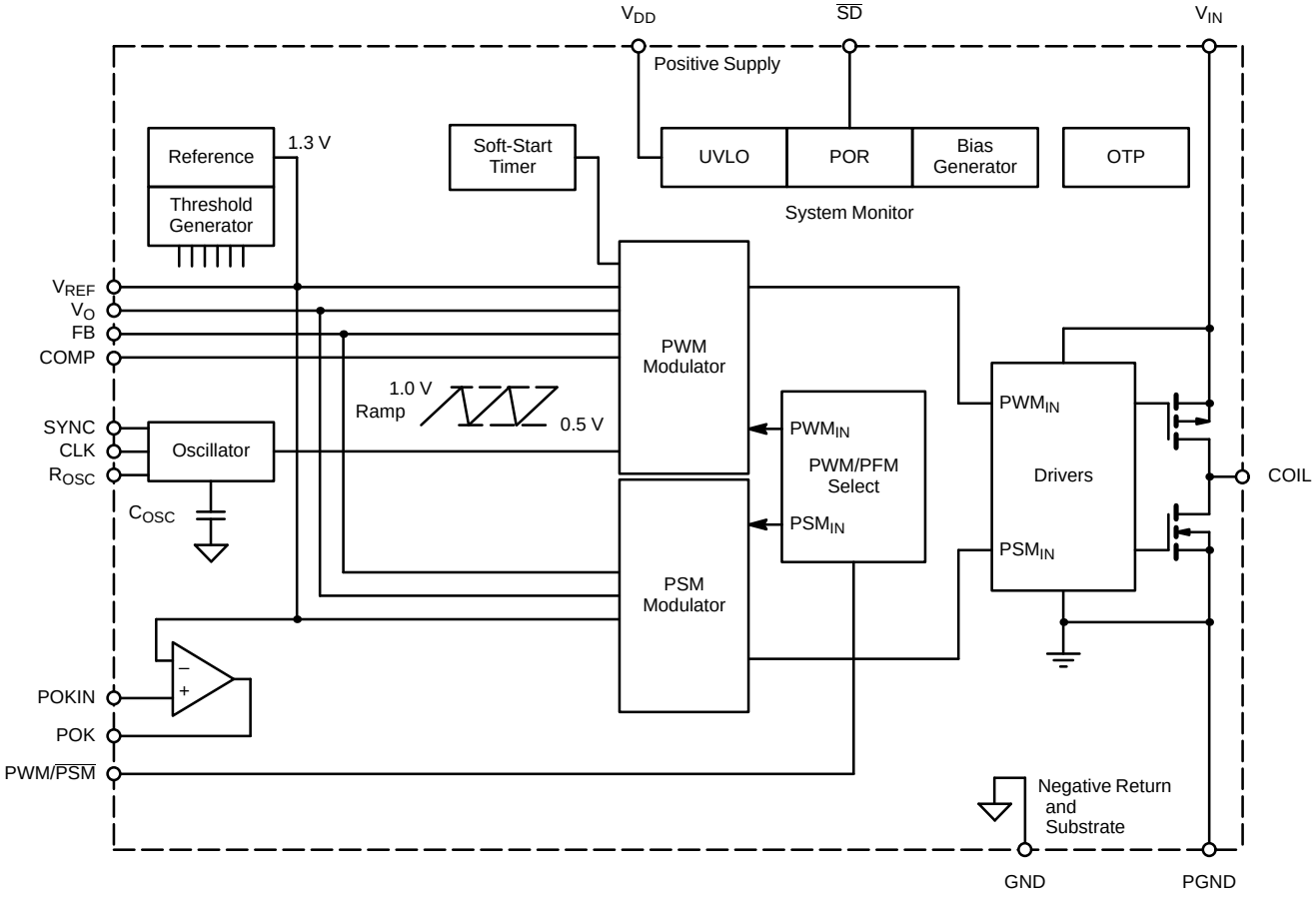



**FIGURE 2.**

## DESIGN GUIDELINES

The following section describes key device features and provides general guidelines for designing a buck regulator with the Si9167.

### Voltage Mode Control

For cellular phone and PDA applications, voltage-mode control provides a number of advantages, including the avoidance of power dissipation in current sensing elements, greater noise immunity (since the PWM signal can be as high as 1 V), and a less complicated single feedback loop to compensate with.

The BiCMOS process used in the Si9167 improves voltage-mode performance by increasing the operating frequency and thereby pushing the closed loop bandwidth to more than 100 kHz. Since the intended applications for this device involves a battery input, such that rapid changes in voltage level are not involved, there is no need for a fast input dynamic response as offered by current mode control.

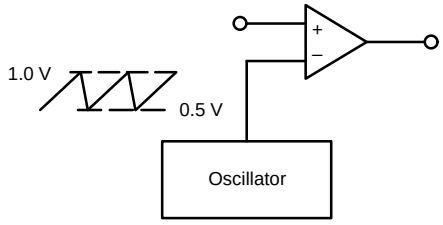



**FIGURE 3.** Voltage Mode Control

In the Si9167, the error amplifier output is compared with the 0.5-V peak-to-peak sawtooth waveform elevated by a 0.5-V offset (Figure 3). The offset provides sufficient noise immunity, even at 2-MHz switching frequencies and 1V/nSec MOSFET switching. The error amplifier has an open loop gain of 60 dB with a 2-MHz unity gain bandwidth. This feature helps to simplify compensation and further increase the closed loop bandwidth. The only external component required to set the oscillator frequency is a resistor at $R_{osc}$ (pin12). The oscillator generates a ±20% tolerance frequency with a ±1% resistor.

### High Frequency Operation

Low power dc-to-dc regulator designers must consider both the on-resistance of the switches and the gate charge required to turn them on and off. Conventional MOSFETs need more gate charge per ampere of current rating, while Vishay Siliconix's extremely low gate charge, PWM optimized MOSFET technology offers optimum performance even above 1-MHz switching frequencies. The Si9167 has 180-mΩ internal drivers and requires a very low gate charge drive, translating into lower switching losses at higher frequencies. Moreover, lower gate charge helps increase the switching speed for a given drive power. This further improves efficiency by reducing crossover losses. For this reason, the Si9167 can achieve up to 93% efficiency even when operating at 1 MHz. Efficiency curves for a 3.6-V buck regulator at various input voltage levels are provided in Figure 4.

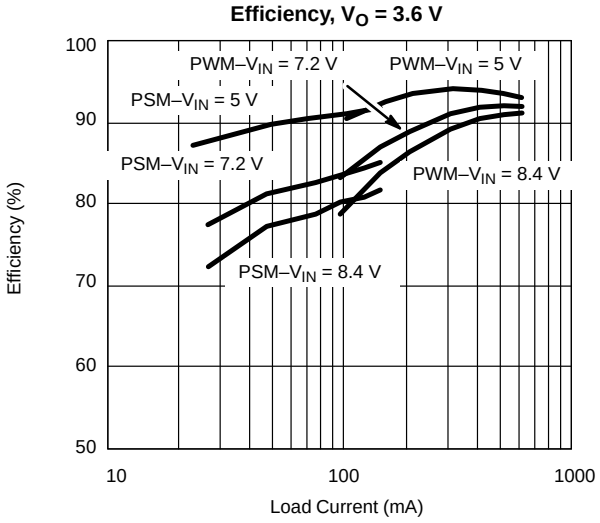


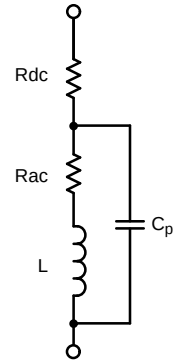

**FIGURE 4.** Efficiency vs. Output Load

### Passive Components

Within limits, high switching frequencies reduce the size of passive components. Frequency-dependent skin effect and hysteresis losses in an inductor, as well as ESR losses in capacitors, are the limiting factors in going to higher operating frequencies. Moreover, the effective impedance of capacitors and inductors at higher operating frequencies are dominated by ESL, ESR, and interlayer capacitance, which causes inductors to behave more like capacitors and capacitors to behave more like inductors.

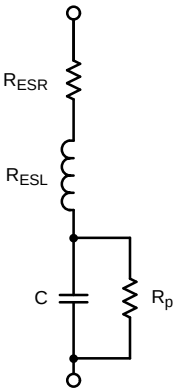
The low-profile, high-current IHLP inductor series from Vishay Dale offers excellent high-frequency performance, as do very low-ESR, high-capacity multilayer ceramic capacitors, such that output ripple is inversely proportional to the switching frequency and not determined by the ESR. The X5R series from Murata and the Y5U series from Tokin are recommended dielectrics.

**Practical Inductor**



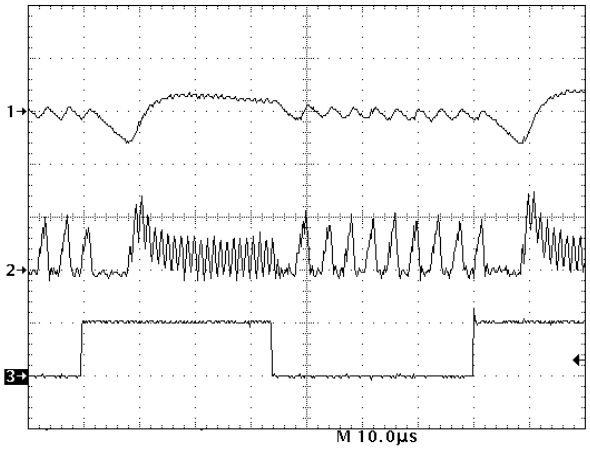

Rdc = dc Resistance of Copper
Rac = Skin Effect Related ac resistance
Cp = Interlayer Capacitance
L Ideal Inductance

**Practical Capacitor**




$R_{ESR}$ = Equivalent Series Resistance
Rp = Insulation Resistance
C = Interlayer Capacitance
$R_{ESL}$ Equivalent Series Inductance

**FIGURE 5.**




$V_{IN}$ = 7.2 V, $V_O$ = 3.6 V, $I_O$ = 150 mA
Ch1: $V_{OUT}$ (200 mV/div)
Ch2: Inductor Current (500 mA/div)
Ch3: PWM/$\overline{PSM}$ (High PWM, Low PSM)

**FIGURE 6.** PSM-PWM-PSM Transition

### PSM-PWM Operation

The Si9167 can operate in either fixed-frequency PWM mode or fixed on-time pulse skipping mode (PSM). Switching losses resulting from the gate charge of the driver and internal BICMOS circuitry are fixed irrespective of the output power drawn from the converter. At lower output levels, the percentage of these losses is high, which makes the circuit less efficient. Therefore, at output loads lower than 150 mA, PSM operation is recommended. PSM operation reduces the operating frequency, depending upon the load, which in turn reduces the switching losses proportionally and keeps the efficiency high at all load current levels.

Low operating frequencies can become a concern if they are in the audible range. Special care has been taken in the Si9167 to ensure that the operating frequency will always be above 20 kHz in pulse-skipping mode at output load currents as low as 6 mA. A load current of 150 mA is guaranteed in PSM, while PWM mode is used for higher load current operation. In this way, converter efficiency is always optimized. Efficiency versus load plots are provided in figures 14 and 15.

Two different sections control the operation of the converter in either PWM mode or PSM. When PWM mode is selected, the PWM control section is active, thereby disabling the PSM control and vice versa. During the PWM-to-PSM transition, there is an overlapping time between the PWM and the PSM circuit activation, which keeps the output voltage from drooping. However, while transitioning from PSM to PWM, there is no such overlap. The time needed to activate the PWM circuit, after the PSM circuit is turned off, is called the blanking time. During this time there are no pulses. This blanking time is typically between 5 to 10 µs. Figure 6 shows the behavior of the output voltage, output, and coil current during the PSM-PWM-PSM transition. The sag in the output depends upon the output capacitance and ESR. The capacitor must be selected for an acceptable droop in output voltage at a maximum load current in PSM, and is given by the following equation:

$$V_{O\_DROP} = I_{OUT}\left(\frac{t_{BLANK}}{C_{OUT}} + ESR\right) \quad (1)$$

Where

$V_{O\_DROP}$ = Output droop during Transition (V)
$t_{BLANK}$ = Blanking time (S)
$C_{OUT}$ = Output Capacitor (F)
ESR = ESR of output Capacitor (Ω)
$I_{OUT}$ = Output Load (A)

### Inductor Selection

A wide selection of inductors is available from vendors such as Vishay Dale, Coiltronix, and Sumida. Major factors to consider include inductance value, saturating current, and equivalent series resistance (RL).

Since the Si9167 can be operated at up to 2 MHz, required inductance for a given output capacitor and ripple current could be as low as 1.5 µH, where:

$$L_{MIN} = \frac{\left(\left(V_{INMAX} - V_{DSQP}\right) - \left(V_{OUT} + V_{R\_DROP}\right)\right)\delta MIN}{0.72 \times Fsw \times \Delta I} \quad (2)$$

$$\delta MIN = \frac{V_{OUT} + V_{R\_DROP}}{V_{INMAX} - V_{DSQP}}$$

$$V_{DSQP} = 0.42 \times I_{OUT}$$

$$V_{R\_DROP} = \left(R_L + R_{TRACE}\right) \times I_{OUT}$$

Where

$V_{INMAX}$ = Maximum input voltage (V)
$V_{OUT}$ = Output Voltage (V)
$V_{DSQP}$ = Voltage drop across the main switch (V)
$\Delta I$ = Max ripple current allowed for acceptable ripple (A)
$\delta$MIN= Duty ratio at $V_{INMAX}$.
$V_{R\_DROP}$ = Resistive drop through inductor and PCB traces (V)
$I_{OUT}$ = Rated output current (A)
$R_L$ = Equivalent Series Resistance ($\Omega$)
$R_{TRACE}$ = Combined resistance of positive and negative output traces ($\Omega$)
Fsw = Oscillator Frequency (Hz)

Refer to Figure 7 when deciding the inductance and frequency. The frequency $V_S$ inductance plot assumes a 10-$\mu$F ceramic multilayer chip capacitor with a 20-m$\Omega$ maximum ESR and 10-mVp-p output ripple.

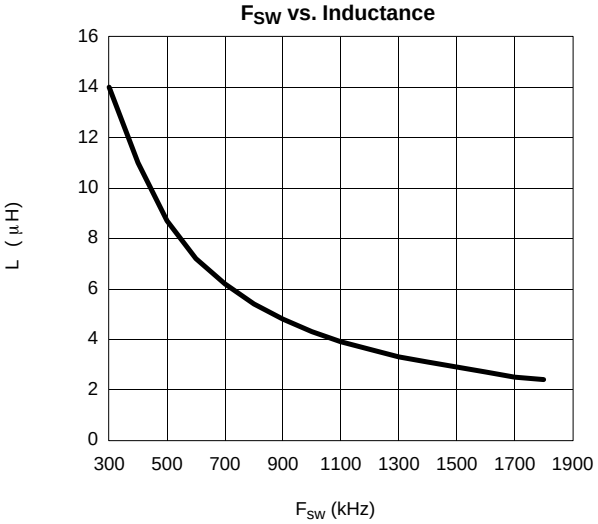



**FIGURE 7.** Inductor Value Selection for 10-$\mu$F Ceramic Output Capacitor

### Output Voltage

The divider resistor pair, R5 and R6 in Figure 1 determine the output regulation point. Since R5 is part of the compensation network, it is strongly recommended that R6 be adjusted in order to change the regulation voltage without affecting the loop gain. With fixed R5, R6 can be easily calculated by (3) for the desired output voltage setting.

$$R6 = \frac{R5}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (3)$$

The typical value for $V_{REF}$ is 1.3 V.

### Power_Good Comparator

The inverting input is internally connected to the reference voltage of 1.3 V (see functional block diagram, Figure 2). This uncommitted comparator, with about 50 mV hysteresis, is intended to be used to sense the output voltage and raise a high flag once the output voltage Vout reaches its regulation limit. The 50-mV hysteresis at the comparator input is provided while output is transitional from high to low. The output is capable of sourcing 2 $\mu$A and sinking 1 mA current. The source current can be increased up to 1 mA by pulling the output high with an external resistor (Figure 1). Use following equation for the POK to switch to high at a $V_{OL}$ and to low at $[V_{OL} - V_{HYSTERESIS}]$.

$$V_{OL} = 1.3 \times \frac{(R7 + R8)}{R8} \text{ Volts} \quad (4)$$

$$V_{HYSTERESIS} = 50 \times \frac{(R7 + R8)}{R8} \text{ mVolts}$$

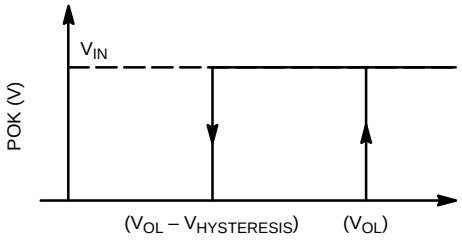



**FIGURE 8.** $V_{OUT}$ (V)

### Synchronization

Systems using more than one converter for power management functions often face EMC problems. The reflected ripple at the inputs from these independent converters, which operate at different frequencies and phases, can create a wide frequency range of harmonics. Obviously, it is difficult, if not impossible, to eliminate all of these from the emission spectrum. The alternatives are to incorporate a heavy filter at the input of each converter or let all converters oscillate at the same frequency and phase.

With the Si9167, synchronization is possible without the use of any extra components. With the external clock, the circuit synchronizes during the falling edge. More than one Si9167 can be configured in a master-slave mode as shown in Figure 9. The SYNC pin may also be driven from a very stable external system clock signal, which locks the slave frequency within a very tight tolerance. Although synchronization is possible only during PWM, circuit performance is not affected when either the master or slave is in PSM. (Switching frequencies for master, slaves and CLK condition in PSM are provided in Table 1.) In addition, since the SYNC is a high-impedance gate, it does not load the CLK when it is in the high state.

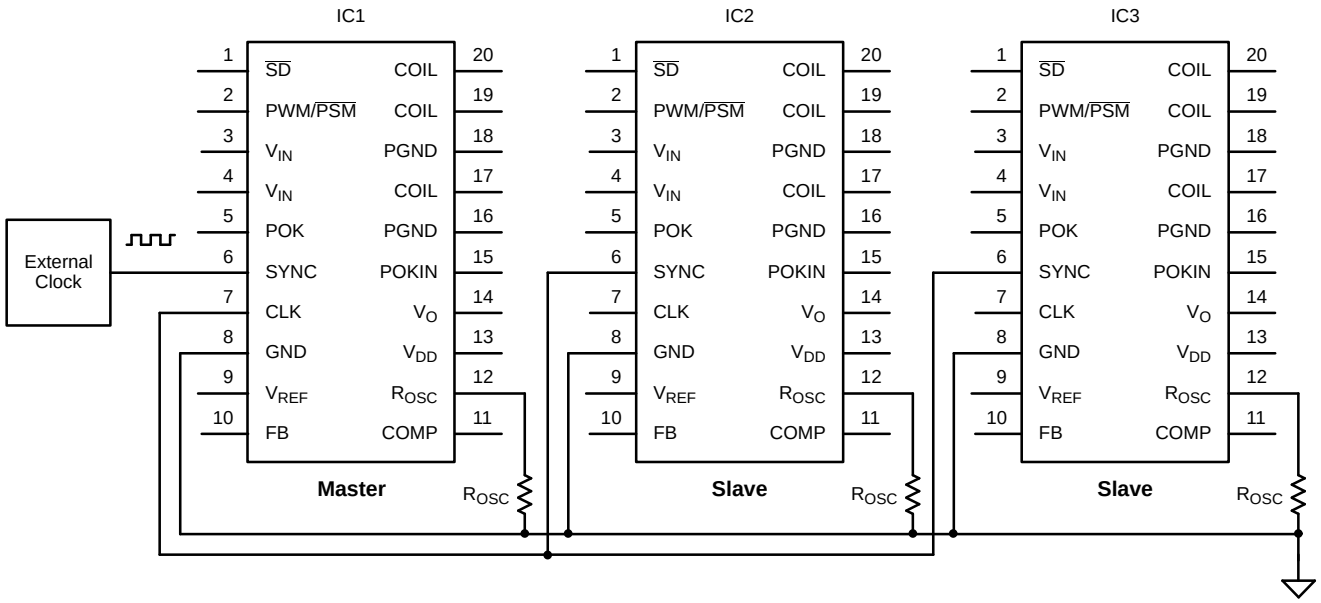
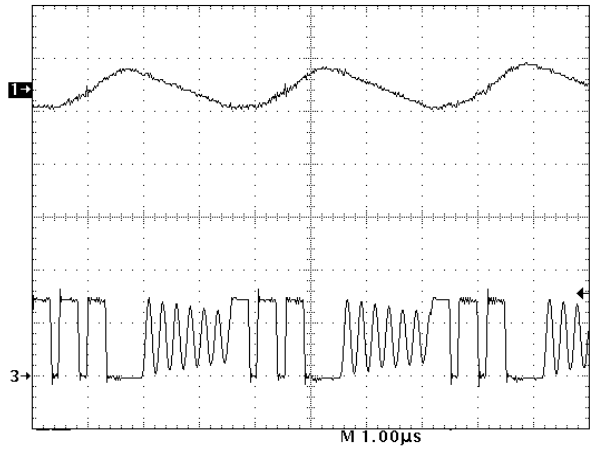



**FIGURE 9.**

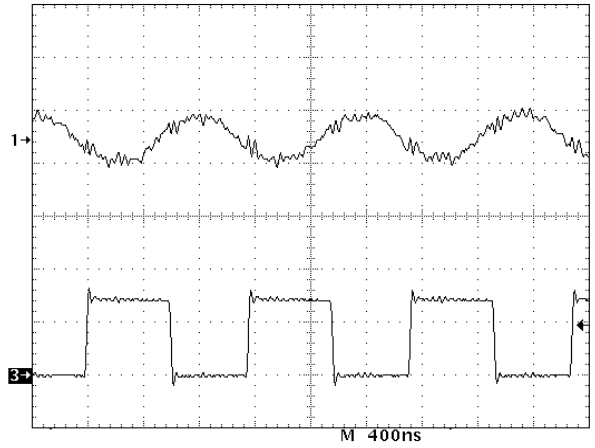
**TABLE 1. MASTER AND SLAVE SWITCH FREQUENCIES DURING SYNCHRONIZATION**

| Mode | | Switch Frequency | | |
|---|---|---|---|---|
| Master | Slave | Master | Slave | Master CLK Pin |
| PWM | PWM | CLK_Master | CLK_Master | ⎍⎍ |
| PWM | PSM | CLK_Master | PSM_Slave | ⎍⎍ |
| PSM | PWM | PSM_Master | CLK_Slave | High |
| PSM | PSM | PSM_Master | PSM_Slave | High |



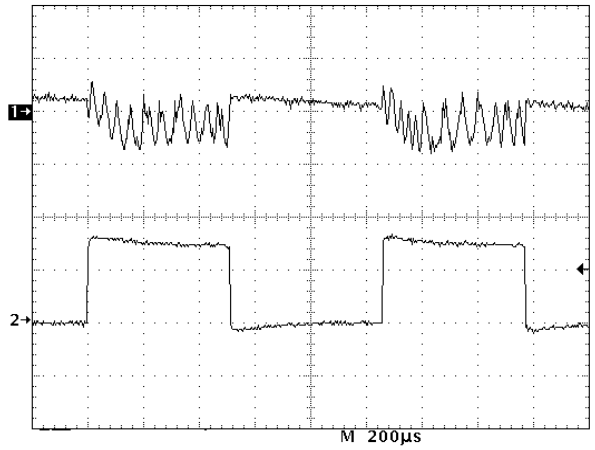

$V_{IN}$ = 7.2 V, $V_O$ = 3.6 V, $I_O$ = 150 mA
Ch1: $V_{OUT}$ (50 mV/div)
Ch3: Coil (5 V/div)

**FIGURE 10.** PSM Output Ripple



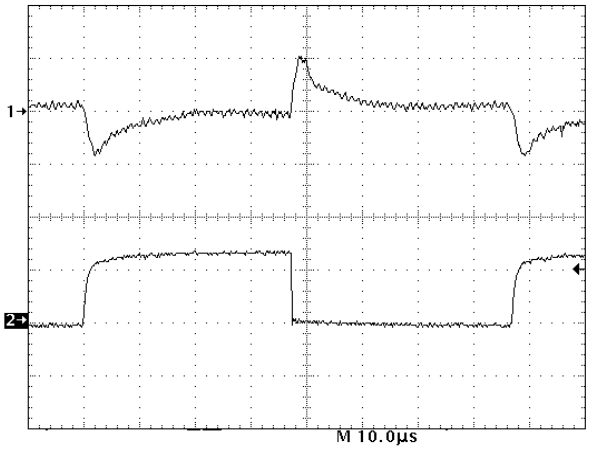

$V_{IN}$ = 7.2 V, $V_O$ = 3.6 V, $I_O$ = 600 mA
Ch1: $V_{OUT}$ (10 mV/div)
Ch3: Coil (5 V/div)

**FIGURE 11.** PWM Output Ripple




$V_{IN}$ = 7.2 V, $V_O$ = 3.6 V, Step $I_O$ = 0 to 150 mA
Step Load Slew Rate = 1 A/µsec
Ch1: $V_{OUT}$ (50 mV/div)
Ch2: $I_{OUT}$ (100 mA/div)

**FIGURE 12.** Transient Response PSM Mode




$V_{IN}$ = 7.2 V, $V_O$ = 3.6 V, Step $I_O$ = 0 to 600 mA
Step Load Slew Rate = 1 A/µsec
Ch1: $V_{OUT}$ (100 mV/div)
Ch2: $I_{OUT}$ (500 mA/div)

**FIGURE 13.** Transient Response PWM Mode

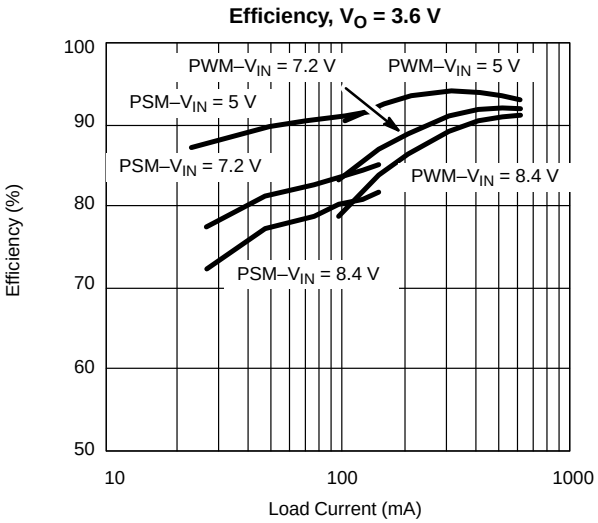



**FIGURE 14.**

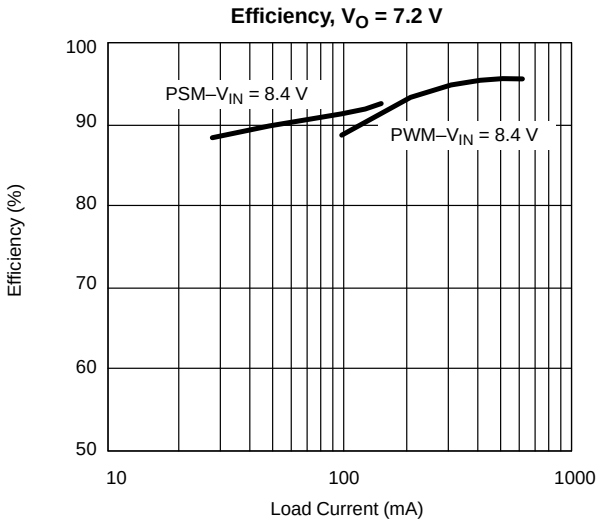



**FIGURE 15.**