# AN-6921

## Integrated Critical Mode PFC / Quasi-Resonant Current Mode PWM Controller FAN6921

## 1. Introduction

This application note presents practical step-by-step design considerations for power supply system employing Fairchild's FAN6921 PFC/PWM combination controller, which combines a Boundary Conduction Mode (BCM) Power Factor Correction (PFC) controller and Quasi-Resonant (QR) PWM controller. Figure 1 shows the typical application circuit, where the BCM PFC converter is in the front end and the Quasi-Resonant flyback converter is in the back end.

FAN6921 achieves high efficiency with relatively low cost for 75~200W applications where BCM and QR operation with a single switch show best performance. BCM boost PFC converter can achieve better efficiency with lower cost than continuous conduction mode (CCM) boost PFC converter. These benefits result from the elimination of the reverse-recovery losses of the boost diode and zero-voltage switching (ZVS) or near ZVS (also called valley switching) of boost switch. The QR flyback converter for the DC/DC conversion achieves higher efficiency than the conventional hard-switching converter with valley switching.

Moreover, FAN6921 has variable PFC output voltage function that can improve the overall efficiency by reducing the conduction loss of PFC converter and switching loss of DC/DC converter stage at low-line condition.

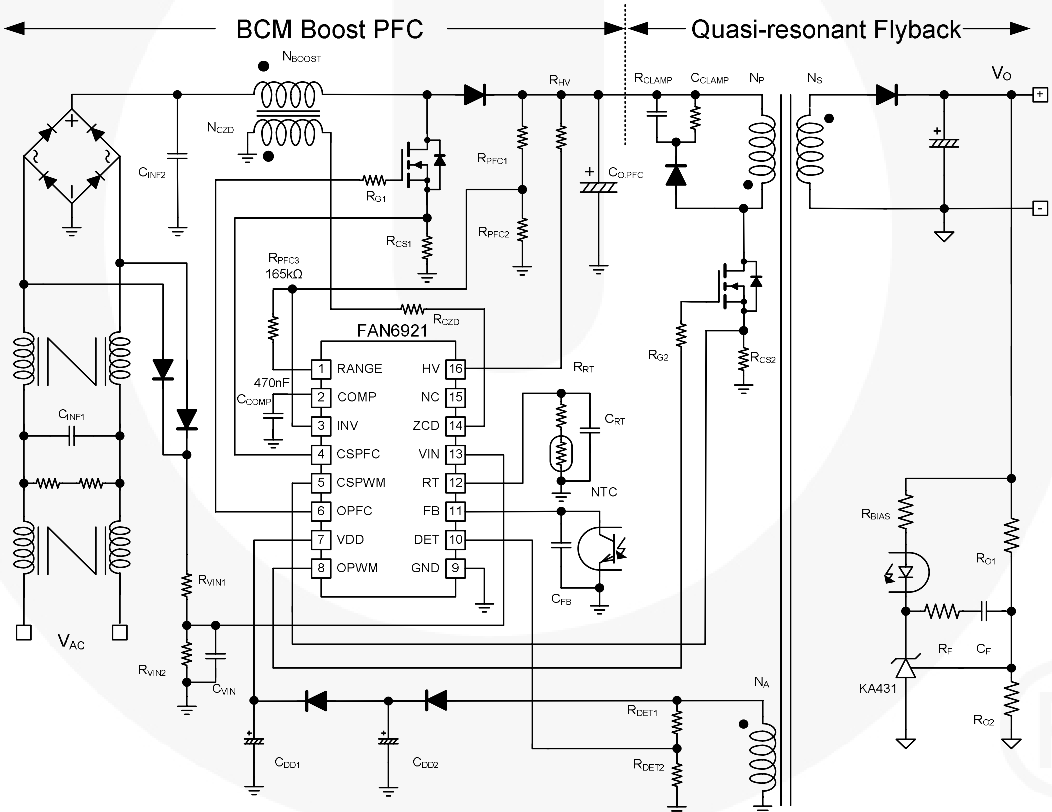


**Figure 1. Typical Application Circuit**

## 2. Operation Principle of BCM Boost PFC Converter

The most widely used operation modes for the boost converter are continuous conduction mode (CCM) and boundary conduction mode (BCM). These refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. As the names indicate, the inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. Even though the BCM operation has higher RMS current in the inductor and switching devices, it allows better switching condition for the MOSFET and the diode. As shown in Figure 2, the diode reverse recovery is eliminated and a fast silicon carbide (SiC) diode is not needed. MOSFET is also turned on with zero current, which reduces the switching loss.

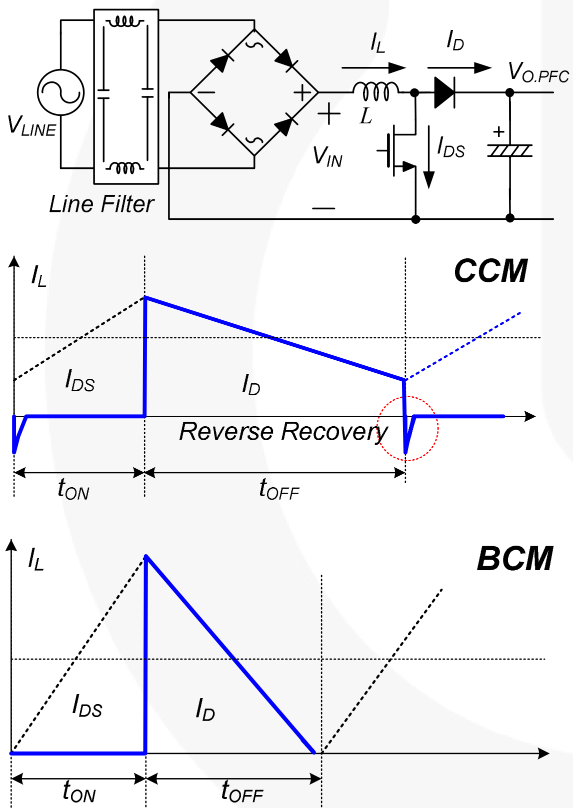


**Figure 2. CCM vs. BCM Control**

The fundamental idea of BCM PFC is that the inductor current starts from zero in each switching period, as shown in Figure 3. When the power transistor of the boost converter is turned on for a fixed time, the peak inductor current is proportional to the input voltage. Since the current waveform is triangular, the average value in each switching period is also proportional to the input voltage. In the case of a sinusoidal input voltage, the input current of the converter follows the input voltage waveform with a very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation an ideal candidate for power factor correction.

A by-product of the BCM is that the boost converter runs with variable switching frequency that depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input current follows the sinusoidal input voltage waveform, as shown in Figure 3. The lowest frequency occurs at the peak of sinusoidal line voltage.

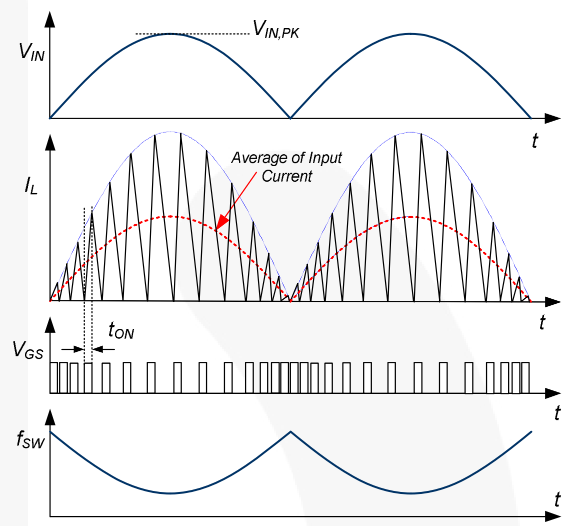


**Figure 3. Operation Waveforms of BCM PFC**

The voltage-second balance equation for the inductor is:

$$V_{IN}(t)\cdot t_{ON} = (V_{O.PFC} - V_{IN}(t))\cdot t_{OFF} \tag{1}$$

where $V_{IN}(t)$ is the rectified line voltage.

The switching frequency of BCM boost PFC converter is obtained as:

$$\begin{aligned} f_{SW} &= \frac{1}{t_{ON}+t_{OFF}} = \frac{1}{t_{ON}}\cdot\frac{V_{O.PFC}-V_{IN}(t)}{V_{OUT}} \\ &= \frac{1}{t_{ON}}\cdot\frac{V_{O.PFC}-V_{IN,PK}\cdot|\sin(2\pi f_{LINE}t)|}{V_{O.PFC}} \end{aligned} \tag{2}$$

where $V_{IN,PK}$ is the amplitude of the line voltage and $f_{LINE}$ is the line frequency.

Figure 4 shows how the MOSFET on time and switching frequency change as output power decreases. When the load decreases, as shown in the right side of Figure 4, the peak inductor current diminishes with reduced MOSFET on time and the switching frequency increases.

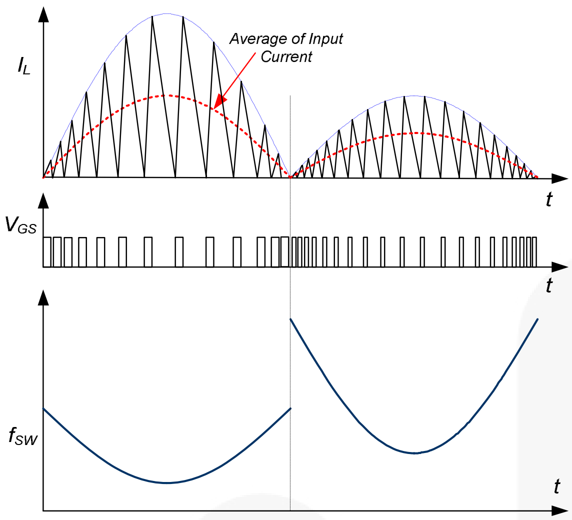


**Figure 4. Frequency Variation of BCM PFC**

Since the design of line filter and inductor for a BCM PFC converter with variable switching frequency should be done at minimum frequency condition, it is worthwhile to examine how the minimum frequency of BCM PFC converter changes with operating conditions.

Figure 5 shows the minimum switching frequency, which occurs at the peak of line voltage, as a function of the RMS line voltage for different output voltage settings. For universal line application, the minimum switching frequency occurs at high line (265$V_{AC}$) as long as the output voltage is lower than about 405V.

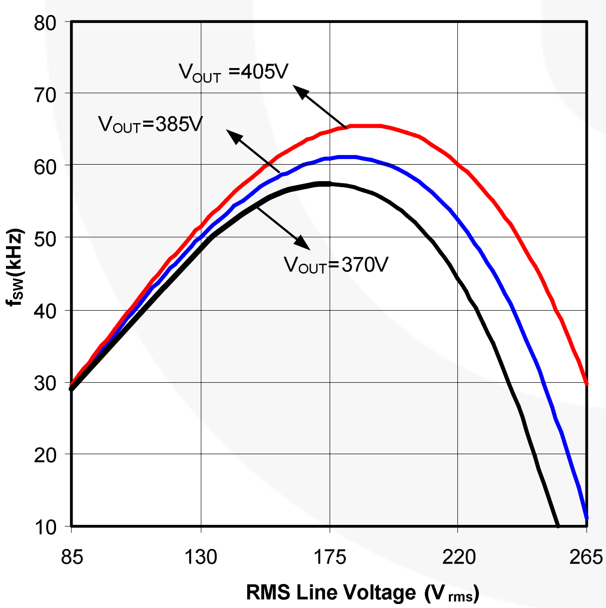


**Figure 5. Minimum Switching Frequency vs. RMS Line Voltage (L = 780µH, $P_{OUT}$ = 100W)**

# 3. Operation Principle of Quasi-Resonant Flyback Converter

QR flyback converter topology can be derived from a conventional square wave, pulse-width modulated (PWM), flyback converter without adding additional components. Figure 6 and Figure 7 show the simplified circuit diagram of a quasi-resonant flyback converter and its typical waveforms. The basic operation principles are:

- During the MOSFET on time ($t_{ON}$), input voltage ($V_{IN}$) is applied across the primary-side inductor ($L_m$). MOSFET current ($I_{DS}$) increases linearly from zero to the peak value ($I_{pk}$). During this time, the energy is drawn from the input and stored in the inductor.
- When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to turn on. During the diode ON time ($t_D$), the output voltage ($V_o$) is applied across the secondary-side inductor and the diode current ($I_D$) decreases linearly from the peak value to zero. At the end of $t_D$, all the energy stored in the inductor has been delivered to the output. During this period, the output voltage is reflected to the primary side as $V_o\times N_p/N_s$. Then, the sum of input voltage ($V_{IN}$) and the reflected output voltage ($V_o\times N_p/N_s$) is imposed across the MOSFET.
- When the diode current reaches zero, the drain-to-source voltage ($V_{DS}$) begins to oscillate by the resonance between the primary-side inductor ($L_m$) and the MOSFET output capacitor ($C_{oss}$) with an amplitude of $V_o\times N_p/N_s$ on the offset of $V_{IN}$, as depicted in Figure 7. Quasi-resonant switching is achieved by turning on the MOSFET when $V_{DS}$ reaches its minimum value. This reduces the MOSFET turn-on switching loss caused by the capacitance loading between the drain and source of the MOSFET.

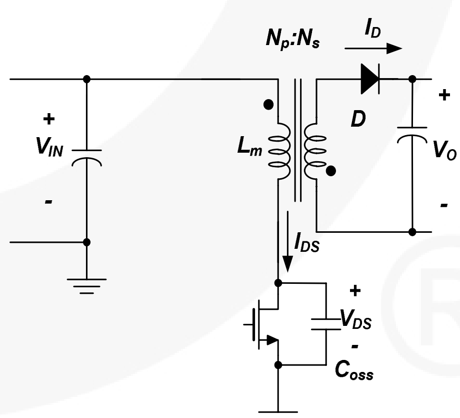


**Figure 6. Schematic of QR Flyback Converter**

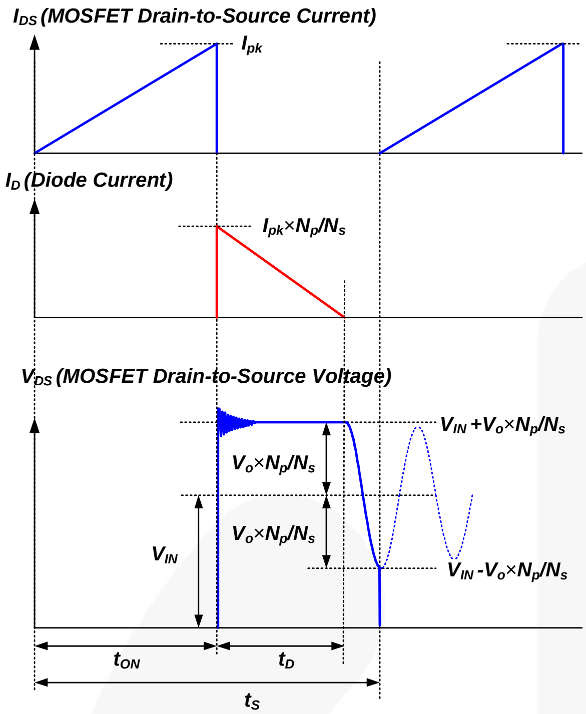


**Figure 7. Typical Waveforms of QR Flyback Converter**

## 4. Design Considerations

This design procedure uses the schematic in Figure 1 as a reference. A 90W PFC application with universal input range is selected as a design example. The design specifications are:

- Line Voltage Range: 90~264$V_{AC}$ (60Hz)
- Output of DC/DC Converter: 19V/4.7A (90W)
- PFC Output Voltage for High Line: 400V ($V_{O.PFC.H}$)
- PFC Output Voltage for Low Line: 260V ($V_{O.PFC.L}$)
- Minimum PFC Switching Frequency: > 50kHz
- Brownout Protection Line Voltage: 70$V_{AC}$
- Output Over-Voltage Protection Trip Point: 22.5V
- Overall Efficiency: 90%
  (PFC Stage: 95%, DC/DC Stage: 95%)

### Part A. PFC Section

#### [STEP-A1] Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. From Equation 2, the minimum frequency with a given line voltage and MOSFET on time is obtained as:

$$f_{SW,MIN} = \frac{1}{t_{ON}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE}}{V_{O.PFC}} \quad (3)$$

where:
$V_{LINE}$ is RMS line voltage;
$t_{ON}$ is the MOSFET conduction time; and
$V_{O.PFC}$ is the PFC output voltage.

The MOSFET conduction time with a given line voltage at a nominal output power is given as:

$$t_{ON} = \frac{2 \cdot P_{O.PFC} \cdot L}{\eta \cdot V_{LINE}^2} \quad (4)$$

where:
η is the overall efficiency;
L is the boost inductance; and
$P_{OUT}$ is the nominal output power.

Using Equation 4, the minimum switching frequency of Equation 3 can be expressed as:

$$f_{SW,MIN} = \frac{\eta \cdot V_{LINE}^2}{2 \cdot P_{OUT} \cdot L} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE}}{V_{O.PFC}} \quad (5)$$

Since the minimum frequency occurs at high line as long as the PFC output voltage is lower than 405V, as observed in Figure 5; once the output voltage and minimum switching frequency are set, the inductor value is given as:

$$L = \frac{\eta \cdot (V_{LINE.MAX})^2}{2 \cdot P_{OUT} \cdot f_{SW,MIN}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE.MAX}}{V_{O.PFC}} \quad (6)$$

where $V_{LINE,MAX}$ is the maximum line voltage.

As the minimum frequency decreases, the switching loss is reduced, while the inductor size and line filter size increase. Thus, the minimum switching frequency should be determined by the trade-off between efficiency and the size of magnetic components. The minimum switching frequency must be above 20kHz to prevent audible noise.

Once the inductance value is decided, the maximum peak inductor current at the nominal output power is obtained at low-line condition as:

$$I_{L.PK} = \frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{LINE,MIN}} \quad (7)$$

where $V_{LINE,MIN}$ is the minimum line voltage.

Since the maximum on time is internally limited at 20µs, it should be smaller than 20µs as:

$$t_{ON}^{MAX} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE.MIN}^2} < 20\mu s \quad (8)$$

The number of turns of boost inductor should be determined considering the core saturation. The minimum number is given as:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L}{A_e \cdot \Delta B} \quad (9)$$

where is Ae is the cross-sectional area of core and ΔB is the maximum flux swing of the core in Tesla. ΔB should be set below the saturation flux density.

**(Design Example)** Since the output voltage is 400V for high line and 260V for low line, the minimum frequency occurs at high-line (264$V_{AC}$) and full-load condition. Assuming the overall efficiency is 90% and selecting the minimum frequency as 58kHz, the inductor value is obtained as:

$$L = \frac{\eta \cdot V_{LINE,MAX}^{\ 2}}{2 \cdot P_{OUT} \cdot f_{SW,MIN}} \cdot \frac{V_{O.PFC.H} - \sqrt{2}V_{LINE,MAX}}{V_{O.PFC.H}}$$

$$= \frac{0.9 \cdot 264^2}{2 \cdot 90 \cdot 58 \times 10^3} \cdot \frac{400 - \sqrt{2} \cdot 264}{400} = 400\mu H$$

The maximum peak inductor current at nominal output power is calculated as:

$$I_{L,PK} = \frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{LINE,MIN}} = \frac{2\sqrt{2} \cdot 90}{0.9 \cdot 90} = 3.14A$$

$$t_{ON}^{\ MAX} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE.MIN}^{\ 2}} = \frac{2 \cdot 90 \cdot 400 \times 10^{-6}}{0.9 \cdot 90^2}$$

$$= 9.87\mu s < 20\mu s$$

Assuming RM10 core (PC40, $A_e$=98mm$^2$) is used and setting ΔB as 0.23T, the primary winding should be:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L}{A_e \cdot \Delta B} = \frac{3.14 \cdot 400 \times 10^{-6}}{98 \times 10^{-6} \cdot 0.23} = 55.7 \, turns$$

Thus, the number of turns ($N_{BOOST}$) of boost inductor is determined as 60.

### [STEP-A2] Auxiliary Winding Design

Figure 9 shows the internal block for zero-current detection (ZCD) for the PFC. FAN6921 indirectly detects the inductor zero current instant using an auxiliary winding of the boost inductor.

The auxiliary winding should be designed such that the voltage of the ZCD pin rises above 2.1V when the boost switch is turned off to trigger internal comparator as:

$$\frac{N_{ZCD}}{N_{BOOST}}(V_{O.PFC.H} - \sqrt{2}V_{LINE.MAX}) > 2.1V \quad (10)$$

where $V_{O.PFC.H}$ is the PFC output voltage for high line condition.

The ZCD pin has upper voltage clamping and lower voltage clamping at 10V and 0.65V, respectively. When the ZCD pin voltage is clamped at 0.65V, the maximum sourcing current is 1.5mA and, therefore, the resistor $R_{ZCD}$ should be properly designed to limit the current of the ZCD pin below 1.5mA in the worst case as:

$$R_{ZCD} > \frac{V_{IN}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} = \frac{\sqrt{2}V_{LINE.MAX}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} \quad (11)$$

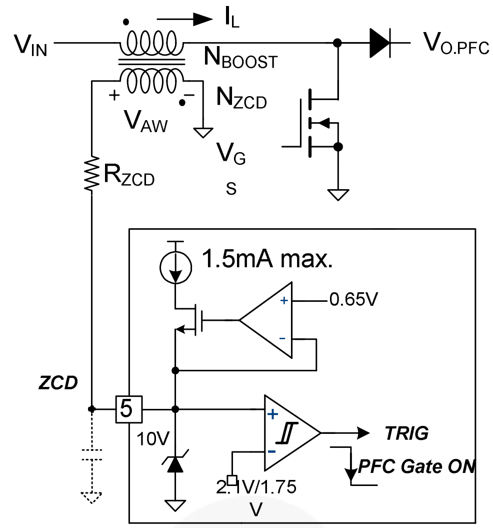


**Figure 8. Internal Block for ZCD**

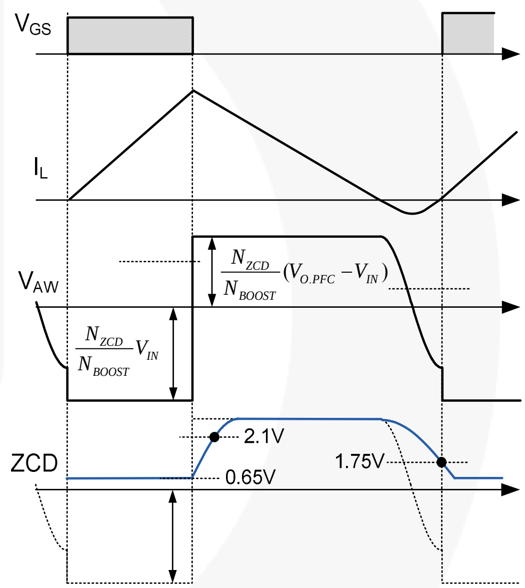


**Figure 9. ZCD Waveforms**

**(Design Example)** The number of turns for the auxiliary ZCD winding is obtained as:

$$N_{ZCD} > \frac{2.1 N_{BOOST}}{(V_{O.PFC.H} - \sqrt{2}V_{LINE.MAX})} = 4.7 turns$$

With a margin, $N_{AUX}$ is determined as 8 turns.

Then $R_{ZCD}$ is selected from:

$$R_{ZCD} > \frac{\sqrt{2}V_{LINE.MAX}}{1.5mA} \cdot \frac{N_{ZCD}}{N_{BOOST}} = \frac{\sqrt{2} \cdot 265}{1.5 \times 10^{-3}} \cdot \frac{8}{60} = 33k\Omega$$

as 68kΩ.

### [STEP-A3] Design $V_{IN}$ and $V_{O.PFC}$ Sense Circuit

FAN6921 senses the line voltage using the averaging circuit shown in Figure 10, where the VIN pin is connected to the AC line through a voltage divider and low-pass filter capacitor. When VIN pin voltage drops below 1V, the COMP pin is clamped at 1.6V to limit the energy delivered to output. Then $V_{O.PFC}$ decreases with the INV pin voltage. When INV pin voltage drops below 1.2V, brownout protection is triggered, stopping gate drive signals of PFC and DC/DC. This protection is reset when $V_{DD}$ drops below the turn-off threshold (UVLO threshold). When $V_{DD}$ rises to the turn-on voltage after dropping below the turn-off threshold, FAN6921 resumes normal operation (if $V_{VIN}$ is higher than 1.3V).

The brownout protection level can be determined as:

$$V_{LINE.BO} = \frac{\pi}{2\sqrt{2}} \cdot \frac{R_{VIN1} + R_{VIN2}}{R_{VIN2}} \qquad (12)$$

The minimum line voltage for PFC startup is given as:

$$V_{LINE.STR} = 1.3 \cdot V_{LINE.BO} \qquad (13)$$

FAN6921 has a variable output voltage function that reduces the PFC output voltage at low-line condition. When the voltage of the VIN pin is higher than 2.45V, the internal switch QR is turned on and the lower resistor $R_{PFC2}$ of the voltage divider is in parallel with $R_{PFC3}$. Then, the PFC output voltage for high line is given as:

$$V_{O.PFC.H} = 2.5 \cdot \left(\frac{R_{PFC1}}{R_{PFC2} // R_{PFC3}} + 1\right) \qquad (14)$$

When the voltage of the VIN pin is lower than 2.1V, the lower resistor $R_{PFC2}$ of the voltage divider is not in parallel with $R_{PFC3}$. Then, the PFC output voltage for low line is given as:

$$V_{O.PFC.L} = 2.5 \cdot \left(\frac{R_{PFC1}}{R_{PFC2}} + 1\right) \qquad (15)$$

The ratio between the nominal PFC output voltage and reduced PFC output voltage is approximated as:

$$\frac{V_{O.PFC.H}}{V_{O.PFCL}} \cong \frac{R_{PFC2}}{R_{PFC3}} + 1 \qquad (16)$$

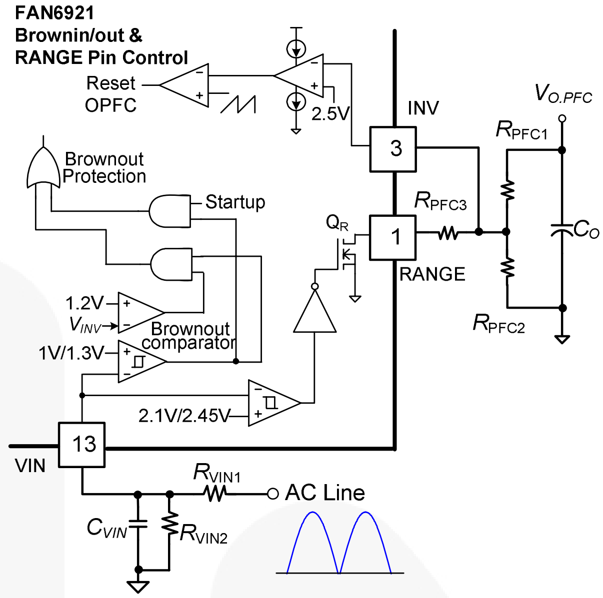


**Figure 10. $V_{IN}$ Sensing Internal Block**

**(Design Example)** Setting the brownout protection trip point as $69V_{AC}$:

$$\frac{R_{VIN1} + R_{VIN2}}{R_{VIN2}} = V_{LINE.BO} \cdot \frac{2\sqrt{2}}{\pi} = 62$$

Determining $R_{VIN2}$ as 154kΩ, $R_{VIN1}$ is determined as 9.4MΩ.

The line voltage to start up the PFC is obtained as:

$$V_{LINE.STR} = 1.3 \cdot V_{LINE.BO} = 90V_{AC}$$

To regulate the PFC output voltage at high line as 400V:

$$V_{O.PFC} = 2.5 \cdot \left(\frac{R_{PFC1}}{R_{PFC2} // R_{PFC3}} + 1\right) = 400$$

By selecting $R_{PFC1}$=9.4MΩ:

$$R_{PFC2} // R_{PFC3} = \frac{9.4M\Omega}{\left(\frac{400}{2.5} - 1\right)} = 59.1k\Omega$$

To regulate the PFC output voltage at low line as 260V:

$$\frac{V_{O.PFC.H}}{V_{O.PFC.L}} = \frac{400}{260} \cong \frac{R_{PFC2}}{R_{PFC3}} + 1$$

By selecting $R_{PFC2}$=165kΩ:

$$R_{PFC3} = \left(\frac{400}{260} - 1\right) R_{PFC2} = 89k\Omega$$

So $R_{PFC1}$, $R_{PFC2}$, and $R_{PFC3}$ are selected from the off-the-shelf components as 9.4MΩ, 91kΩ, and 165kΩ, respectively.

### [STEP-A4] Current Sensing Resistor for PFC

FAN6921 has pulse-by-pulse current limit function. It is typical to set the pulse-by-current limit level at 20~30% higher than the maximum inductor current:

$$R_{CS1} = \frac{0.85}{I_{L.PK}(1+K_{MARGIN})} \quad (17)$$

where $K_{MARGIN}$ is the margin factor and 0.85V is the pulse-by-pulse current limit threshold.

**(Design Example)** Choosing the margin factor as 35%, the sensing resistor is selected as:

$$R_{CS1} = \frac{0.85}{I_{L.PK}(1+K_{MARGIN})} = \frac{0.85}{3.14(1+0.35)} = 0.2\Omega$$

### [STEP-A5] Output Capacitor Selection

For a given minimum PFC output voltage during the hold-up time, the PFC output capacitor is obtained as:

$$C_{O.PFC} > \frac{2P_{OUT}\cdot t_{HOLD}}{V_{O.PFC.L}{}^2 - V_{O.PFC,HLD}{}^2} \quad (18)$$

where:

$P_{OUT}$ is total nominal output power;

$t_{HOLD}$ is the required holdup time; and

$V_{O.PFC,HLD}$ is the allowable minimum output voltage during the hold-up time.

For PFC output capacitor, it is typical to use 0.5~1µF per 1W output power for 400V PFC output. Meanwhile, it is reasonable to use about 1µF per 1W output power for variable output PFC due to the larger voltage drop during the hold-up time than 400V output.

**(Design Example)** Assuming the minimum allowable PFC output voltage during the hold-up time is 160V, the capacitor should be:

$$C_{O.PFC} > \frac{2P_{OUT}\cdot t_{HOLD}}{V_{O.PFC.H}{}^2 - V_{O.PFC.HLD}{}^2} = \frac{2\cdot 90\cdot 20\times 10^{-3}}{258^2 - 160^2} = 88\mu F$$

A 100µF capacitor is selected for the output capacitor. The minimum PFC output voltage during the hold-up time is:

$$V_{O.PFC.HOLD} = \sqrt{V_{OUT}{}^2 - \frac{2P_{OUT}\cdot t_{HOLD}}{C_{OUT}}} = \sqrt{258^2 - \frac{2\cdot 90\cdot 20\times 10^{-3}}{100\times 10^{-6}}} = 175V$$

### [STEP-A6] Design Compensation Network

The feedback loop bandwidth must be lower than 20Hz for the PFC application. If the bandwidth is higher than 20Hz, the control loop may try to reduce the 120Hz ripple of the output voltage and the line current is distorted, decreasing power factor. A capacitor is connected between COMP and GND to attenuate the line frequency ripple voltage by 40dB. If a capacitor is connected between the output of the error amplifier and the GND, the error amplifier works as an integrator and the error amplifier compensation capacitor can be calculated by:

$$C_{COMP} > \frac{100\cdot g_M}{2\pi\cdot 2 f_{LINE}}\cdot\frac{2.5}{V_{O.PFC.H}} \quad (19)$$

To improve the power factor, $C_{COMP}$ must be higher than the calculated value. However, if the value is too high, the output voltage control loop may become slow.

**(Design Example)**

$$C_{COMP} > \frac{100\cdot g_M}{2\pi\cdot 2 f_{LINE}}\cdot\frac{2.5}{V_{O.PFC.H}} = \frac{100\cdot 125\times 10^{-6}}{2\pi\cdot 2\cdot 60}\cdot\frac{2.5}{400} = 103nF$$

470nF is selected for better power factor.

## Part B. DC/DC Section

### [STEP-B1] Determine the Reflected Output Voltage ($V_{RO}$)

Figure 11 shows the typical operation waveforms of a quasi-resonant flyback converter. When the MOSFET is turned off, the input voltage (PFC output voltage), together with the output voltage reflected to the primary ($V_{RO}$), is imposed on the MOSFET. When the MOSFET is turned on, the sum of input voltage reflected to the secondary side and the output voltage is applied across the diode. Thus, the maximum nominal voltage across the MOSFET ($V_{ds}^{nom}$) and diode are given as:

$$V_{DS}^{nom} = V_{O.PFC.H} + n(V_O + V_F) = V_{O.PFC.H} + V_{RO}$$

where:

$$n = \frac{V_{RO}}{V_O + V_F} \tag{20}$$

$$V_D^{nom} = V_O + \frac{V_{O.PFC.H}}{n} = V_O + \frac{V_{O.PFC.H}}{V_{RO}}(V_O + V_F) \tag{21}$$

By increasing $V_{RO}$ (i.e. the turns ratio, n), the capacitive switching loss and conduction loss of the MOSFET are reduced. This also reduces the voltage stress of the secondary-side rectifier diode. However, this increases the voltage stress on the MOSFET. Therefore, $V_{RO}$ should be determined by a trade-off between the voltage stresses of the MOSFET and diode. It is typical to set $V_{RO}$ such that $V_{DS}^{norm}$ and $V_D^{nom}$ are 75~85% of their voltage ratings.

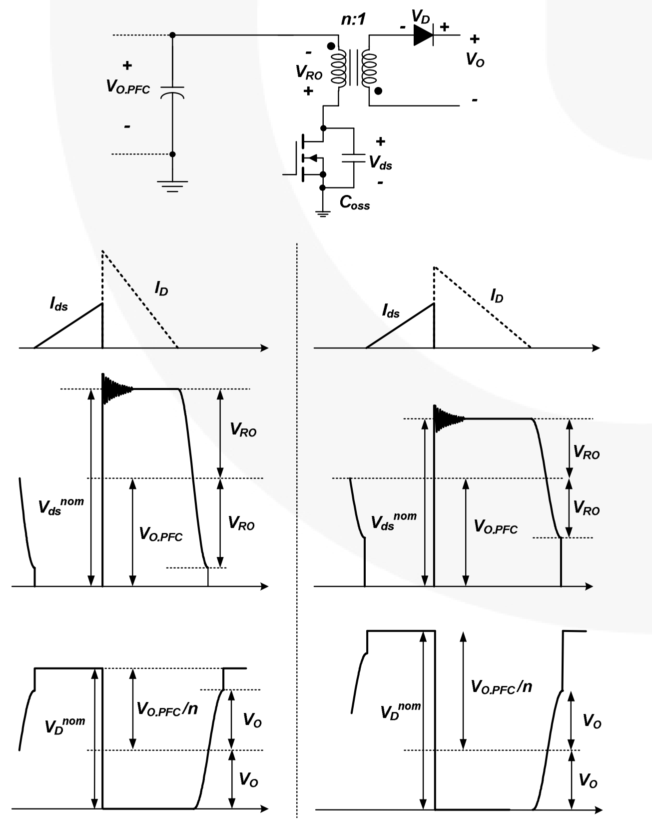


**Figure 11. Typical Waveforms of QR Flyback Converter**

**(Design Example)** Assuming 650V MOSFET and 100V MOSFET are used for primary side and secondary side, respectively, with 18% voltage margin:

$$0.82 \cdot 650V > V_{DS}^{nom} = V_{O.PFC} + V_{RO}$$
$$\therefore V_{RO} < 0.82 \cdot 650 - V_{O.PFC} = 133V$$

$$0.82 \cdot 100 > V_D^{nom} = V_O + \frac{V_{O.PFC}}{V_{RO}}(V_O + V_F)$$

$$\therefore V_{RO} > V_D^{nom} = \frac{V_{O.PFC}}{0.82 \cdot 100 - V_O}(V_O + V_F) = 121V$$

$V_{RO}$ is determined as 130V.

### [STEP-B2] Transformer Design

Figure 12 shows the typical switching timing of a quasi-resonant converter. The sum of MOSFET conduction time ($t_{ON}$), diode conduction time ($t_D$), and drain voltage falling time ($t_F$) is the switching period ($t_S$). To determine the primary-side inductance ($L_m$), the following parameters should be determined first.

**Minimum Switching Frequency ($f_{S.QR}^{min}$)**
The minimum switching frequency occurs at the minimum input voltage and full-load condition, which should be higher than 20kHz to avoid audible noise. By increasing $f_{S.QR}^{min}$, the transformer size can be reduced. However, this results in increased switching losses. Determine $f_{S.QR}^{min}$ by a trade-off between switching losses and transformer size. Typically $f_{S.QR}^{min}$ is set to around 50kHz.

**Falling Time of the MOSFET Drain Voltage** ($t_F$)
As shown in Figure 12, the MOSFET drain voltage fall time is half of the resonant period of the MOSFET's effective output capacitance and primary-side inductance. The typical value for $t_F$ is 0.6~1.2µs.

**Non-Conduction Time of the MOSFET** ($t_{OFF}$) FAN6921 has a minimum non-conduction time of MOSFET (8µs), during which turning on of MOSFET is prohibited. To maximize the efficiency, it is necessary to turn on the MOSFET at the first valley of MOSFET drain-to-source voltage at heavy-load condition. Therefore, the MOSFET non-conduction time at heavy load condition should be larger than 8µs.

After determining $f_{S.QR}^{min}$ and $t_F$, the maximum duty cycle is calculated as:

$$D_{max} = \frac{V_{RO}}{V_{RO} + V_{O.PFC.L}} \cdot (1 - f_{S.QR}^{min} \cdot t_F) \tag{22}$$

Then, the primary-side inductance is obtained as:

$$L_m = \frac{\eta_{QR} \cdot (V_{O.PFC.L} \cdot D_{max})^2}{2 \cdot f_{S.QR}^{min} P_{OUT}} \tag{23}$$

Once $L_m$ is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as:

$$I_{DS}{}^{PK} = \frac{V_{O.PFC.L} \cdot D_{\max}}{L_m f_{S.QR}{}^{\min}} \quad (24)$$

$$I_{DS}{}^{RMS} = I_{DS}{}^{PK}\sqrt{\frac{D_{\max}}{3}} \quad (25)$$

The MOSFET non-conduction time at heavy load and low line is obtained as:

$$t_{OFF.L} = \frac{(1 - D_{\max})}{f_{S.QR}{}^{min}} \quad (26)$$

The MOSFET non-conduction time at heavy load and high line is obtained as:

$$t_{OFF.H} = t_{OFF.L} \cdot \frac{V_{O.PFC.L}}{V_{O.PFC.H}} \cdot \frac{V_{O.PFC.H} + V_{RO}}{V_{O.PFC.L} + V_{RO}} \quad (27)$$

To guarantee the first valley switching at high line and heavy-load condition, $t_{OFF.H}$ should be larger than 8µs.

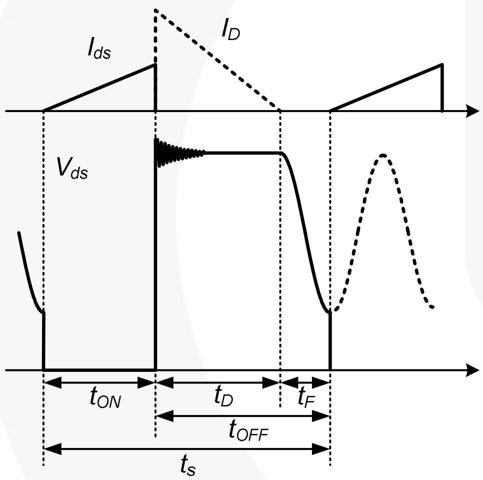


**Figure 12. Switching Timing of QR Flyback Converter**

When designing the transformer, the maximum flux density swing in normal operation (B) as well as the maximum flux density in transient ($B_{max}$) should be considered. The maximum flux density swing in normal operation is related to the hysteresis loss in the core, while the maximum flux density in transient is related to the core saturation.

The minimum number of turns for the transformer primary side to avoid the over temperature in the core is given by:

$$N_P{}^{\min} = \frac{L_m I_{DS}{}^{PK}}{A_e \Delta B} \quad (28)$$

where $B$ is the maximum flux density swing in Tesla. If there is no reference data, use $B$ =0.25~0.30T.

Once the minimum number of turns for the primary side is determined, calculate the proper integer for $N_S$ so that the resulting $N_P$ is larger than $N_p{}^{min}$ as:

$$N_P = n \cdot N_S > N_P{}^{\min} \quad (29)$$

The number of turns of the auxiliary winding for $V_{DD}$ is given as:

$$N_{AUX} = \frac{V_{DD}{}^{nom} + V_{FA}}{(V_O + V_F)} \cdot N_S \quad (30)$$

where $V_{DD}{}^{nom}$ is the nominal $V_{DD}$ voltage, which is typically 18V and $V_{FA}$ is forward voltage drop of $V_{DD}$ diode.

Once the number of turns of the primary winding is determined, the maximum flux density when the drain current reaches its pulse-by-pulse current limit level should be checked to guarantee the transformer is not saturated during transient or fault condition.

The maximum flux density ($B_{max}$) when drain current reaches $I_{LIM}$ is given as:

$$B_{\max} = \frac{L_m I_{LIM}}{A_e N_P} < B_{sat} \quad (31)$$

$B_{max}$ should be smaller than the saturation flux density. If there is no reference data, use $B_{sat}$ =0.35~0.40T.

**(Design Example)** Setting the minimum frequency is 52kHz and the falling time is 0.8µs:

$$D_{\max} = \frac{V_{RO}}{V_{RO} + V_{O.PFC.L}} \cdot (1 - f_{S.QR}{}^{\min} \cdot t_F)$$
$$= \frac{130}{130 + 260} \cdot (1 - 52\times10^3 \cdot 0.8\times10^{-6}) = 0.319$$

$$L_m = \frac{\eta_{QR} \cdot (V_{O.PFC.L} \cdot D_{\max})^2}{2 \cdot f_{S.QR}{}^{\min} P_O}$$
$$= \frac{0.95 \cdot (260 \cdot 0.319)^2}{2 \cdot 52\times10^3 \cdot 90} = 700\mu H$$

$$I_{DS}{}^{PK} = \frac{260 \cdot 0.319}{700\times10^{-6} \cdot 52\times10^3} = 2.28A$$

$$t_{OFF.L} = \frac{(1 - D_{\max})}{f_{S.DD}{}^{min}} = \frac{1 - 0.319}{52\times10^3} = 13\mu s$$

$$t_{OFF.H} = t_{OFF.L} \cdot \frac{V_{O.PFC.L}}{V_{O.PFC.H}} \cdot \frac{V_{O.PFC.H} + V_{RO}}{V_{O.PFC.L} + V_{RO}}$$
$$= 13\mu s \cdot \frac{260}{400} \cdot \frac{400 + 130}{260 + 130} = 11.48\mu s > 8\mu s$$

Assuming POT3319 (Ae=159mm$^2$) core is used and the flux swing is 0.26T

$$N_P^{\min} = \frac{L_m I_{DS}^{PK}}{A_e \Delta B} = \frac{700\times10^{-6}\cdot 2.28}{159\times10^{-6}\cdot 0.26} = 38.6$$

$$N_P = n\cdot N_S = 6.84\cdot 5 = 34 < N_P^{\min}$$
$$= n\cdot N_S = 6.84\cdot 6 = 41 > N_P^{\min}$$

$$N_{AUX} = \frac{V_{DD}^{nom} + V_{FA}}{(V_O + V_F)}\cdot N_S = \frac{18+1.2}{19}\cdot 6 = 6$$

Assuming the pulse-by-pulse current limit for low PFC output voltage is 125% of peak drain current at heavy load:

$$B_{\max} = \frac{L_m I_{LIM}}{A_e N_P} = \frac{700\cdot 2.28\cdot 1.25}{159\cdot 41} = 0.31T$$

### [STEP-B3] Design the Valley Detection Circuit

The valley of MOSFET voltage is detected by monitoring the current flowing out of DET pin. The typical application circuit is shown as Figure 13 and typical waveforms are shown in Figure 14. The DET pin has upper and lower voltage clamping at 5V and 0.7V, respectively. The valley detection circuit is blanked for 8µs after the MOSFET is turned off. When $V_{AUX}$ drops below zero, $V_{DET}$ is clamped at 0.7V and current flows out of the DET pin. MOSFET is turned on with 200ns time delay once the current flowing out of DET pin exceeds 30µA. To guarantee that valley detection circuit is triggered when DET pin is clamped at 0.7V, the current flowing through $R_{DET2}$ should be larger than 30µA as:

$$\frac{0.7}{R_{DET2}} > 30\mu A \qquad (32)$$

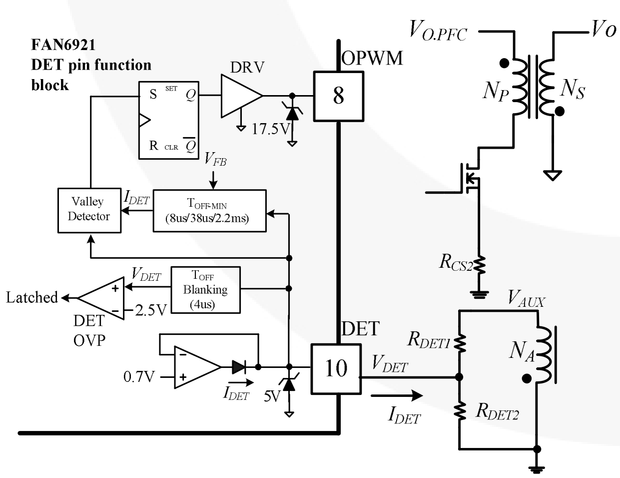


**Figure 13. Typical Application Circuit of DET Pin**

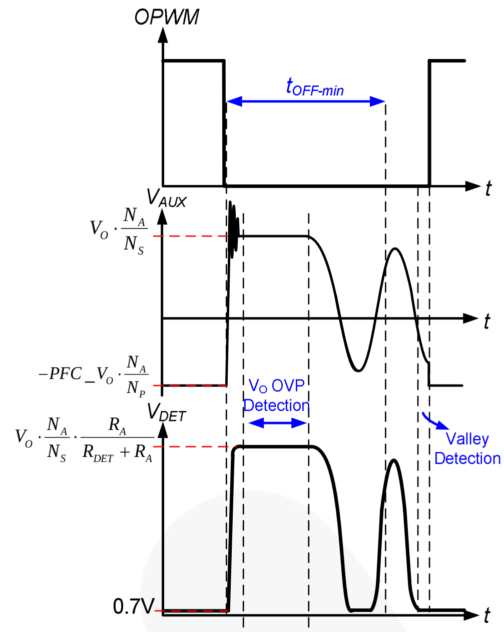


**Figure 14. Waveforms of Valley Detection and $V_O$ OVP Detection**

The output voltage is indirectly monitored for over-voltage protection using the DET pin voltage while the MOSFET is turned off. Thus, the ratio of $R_{DET1}$ and $R_{DET2}$ should be determined as:

$$2.5 = \frac{R_{DET2}}{R_{DET1}+R_{DET2}}\frac{N_A}{N_S}V_{OVP} = \frac{1}{K_{DET}+1}\frac{N_A}{N_S}V_{OVP} \qquad (33)$$

where the ratio between $R_{DET1}$ and $R_{DET2}$ is obtained as:

$$K_{DET} = \frac{R_{DET1}}{R_{DET2}} = \frac{N_A}{N_S}\cdot\frac{V_{OVP}}{2.5} - 1 \qquad (34)$$

For a quasi-resonant flyback converter, the peak drain current with a given output power decreases as input voltage increases. Thus, constant power limit cannot be achieved by just using pulse-by-pulse current limit with constant threshold. FAN6921 has high/low line over power compensation that reduces the pulse-by-pulse current limit level as input voltage increases. FAN6921 senses the input voltage using the current flowing out of the DET pin while the MOSFET is turned on. The pulse-by-pulse current limit level vs. DET current is depicted in Figure 16.

The DET pin current for low line and high line PFC output voltages are given as:

$$I_{DET.L} = \frac{V_{O.PFC.L}\frac{N_A}{N_P} + 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}} \cong \frac{V_{O.PFC.L}\frac{N_A}{N_P}}{R_{DET1}} \qquad (35)$$

$$I_{DET.H} = \frac{V_{O.PFC.H}\frac{N_A}{N_P} + 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}} \cong \frac{V_{O.PFC.H}\frac{N_A}{N_P}}{R_{DET1}} \qquad (36)$$

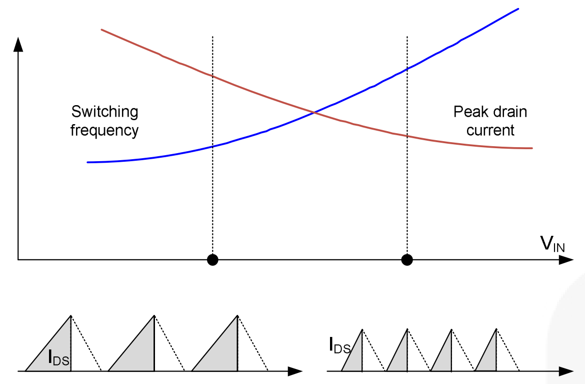


**Figure 15. Switching Frequency and Peak Drain Current Change as Input Voltage Increases**

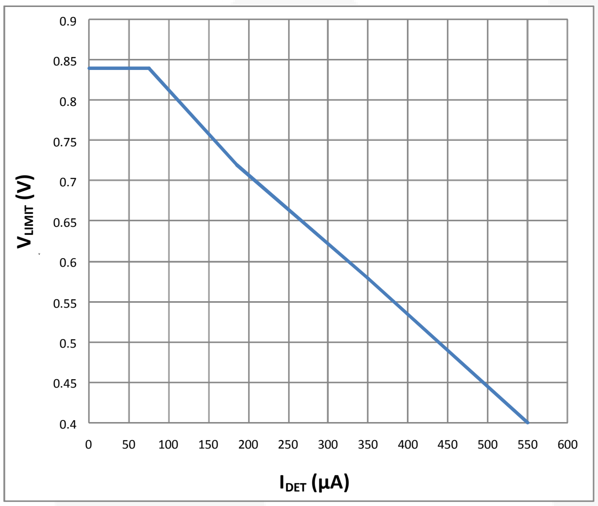


**Figure 16. $I_{DET}$-$V_{LIMIT}$ Curve**

The relationship between $I_{DET}$ and $V_{LIMIT}$ in the linear region ($I_{DET}$=100~500µA) can be approximated as:

$$V_{LIMIT} = -877 \cdot I_{DET} + 0.882 \quad (37)$$

For a given output power, the ratio between drain peak currents at low line and highline is obtained as:

$$\frac{I_{DS}^{PK.L}}{I_{DS}^{PK.H}} = \frac{V_{O.PFC.H}}{V_{O.PFC.L}} \cdot \frac{V_{O.PFC.L} + V_{RO}}{V_{O.PFC.H} + V_{RO}} \quad (38)$$

For a given output power, the ratio between pulse-by-pulse current limit levels at low line and high line is obtained as:

$$\frac{V_{LIMIT.L}}{V_{LIMIT.H}} \cong \frac{-994 \cdot V_{O.PFC.L}\frac{N_A}{N_P} + R_{DET1}}{-994 \cdot V_{O.PFC.H}\frac{N_A}{N_P} + R_{DET1}} \quad (39)$$

To get a constant power limit, $R_{DET1}$ should be determined such that Equations (38) and (39) are equal. However, for actual design, it is typical to use 105~120% of Equation (38), considering the pulse-by-pulse turn-off delay and increased PFC output voltage ripple at low line.

Once the current limit threshold voltage is determined with $R_{DET1}$, the current sensing resistor value is obtained as:

$$V_{LIMIT} = -877 \cdot \left(\frac{V_{O.PFC.L}\frac{N_A}{N_P} + 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}}\right) + 0.882 \quad (40)$$

The current sensing resistor value can be obtained from:

$$R_{CS2} = \frac{V_{LIMIT}}{I_{DS}^{LIM}} \quad (41)$$

**(Design Example)**

$$\frac{0.7}{R_{DET2}} > 30\mu A \ , \ R_{DET2} < 23.3k\Omega$$

Setting the OVP trip point at 22.5V,

$$K_{DET} = \frac{R_{DET1}}{R_{DET2}} = \frac{N_A}{N_S} \cdot \frac{V_{OVP}}{2.5} - 1 = \frac{6}{6} \cdot \frac{22.5}{2.5} - 1 = 8$$

Then $R_{DET1} = K_{DET} \cdot R_{DET2} < 196k\Omega$

$$\frac{I_{DS}^{PK.L}}{I_{DS}^{PK.H}} = \frac{V_{O.PFC.H}}{V_{O.PFC.L}} \cdot \frac{V_{O.PFC.L} + V_{RO}}{V_{O.PFC.H} + V_{RO}} = \frac{400}{260} \cdot \frac{260+130}{400+130} = 1.13$$

Using 116% of 1.13,

$$\frac{V_{LIMIT.L}}{V_{LIMIT.H}} = 1.31 \cong \frac{-994 V_{O.PFC.L}\frac{N_A}{N_P} + R_{DET1}}{-994 \cdot V_{O.PFC.H}\frac{N_A}{N_P} + R_{DET1}}$$

$$= \frac{-994 \cdot \frac{260}{6.8} + R_{DET1}}{-994 \cdot \frac{400}{6.8} + R_{DET1}} = \frac{-38{,}018 + R_{DET1}}{-58{,}490 + R_{DET1}}$$

Then, $R_{DET1} = 124.5k\Omega$ and $R_{DET2} = 15.6k\Omega$

$R_{DET1}$ and $R_{DET2}$ are selected from the off-the-shelf components as 120kΩ and 15kΩ, respectively.

Then, the pulse by pulse current limit threshold voltage is obtained as:

$$V_{LIMIT} = -877 \cdot \left(\frac{V_{O.PFC.L}\frac{N_A}{N_P} + 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}}\right) + 0.882$$

$$= 0.56V$$

To set current limit level at low line as 125% of $I_{DS}^{PK}$

$$\frac{0.56}{2.28A \times 1.25} = 0.2\Omega$$

## [STEP-B4] Design the Feedback Circuit

Figure 17 is a typical feedback circuit mainly consisting of a shunt regulator and a photo-coupler. $R_{01}$ and $R_{02}$ form a voltage divider for output voltage regulation. $R_F$ and $C_F$ are adjusted for control-loop compensation. A small-value RC filter (e.g. $R_{FB}$ = 100Ω, $C_{FB}$ = 1nF) placed from the FB pin to GND can increase stability substantially. The maximum source current of the FB pin is about 1.2mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor, $R_{BIAS}$, is determined as:

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \cdot CTR > 1.2 \times 10^{-3} \quad (42)$$

where $V_{OPD}$ is the drop voltage of photodiode, about 1.2V; $V_{KA}$ is the minimum cathode to anode voltage of shunt regulator (2.5V); and CTR is the current transfer rate of the opto-coupler.

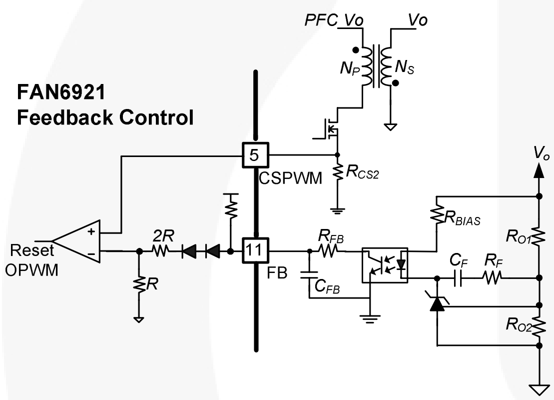


**Figure 17. Feedback Circuit**

**(Design Example)** Assuming CTR is 100%;

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \cdot CTR > 1.2 \times 10^{-3}$$

$$R_{BIAS} < \frac{V_O - V_{OPD} - V_{KA}}{1.2 \times 10^{-3}} = \frac{19 - 1.2 - 2.5}{1.2 \times 10^{-3}} = 12.75k\Omega$$

220Ω resistor is selected for $R_{BIAS}$.

The voltage divider resistors for $V_O$ sensing are selected as 68kΩ and 10kΩ.

## [STEP-B5] Design the Over-Temperature Protection Circuit

The adjustable Over-Temperature Protection (OTP) circuit is shown in Figure 18. As can be seen, a constant sourcing current source ($I_{RT}$) is connected to the RT pin. Once $V_{RT}$ is lower than 0.8V for longer than 10ms debounce time, FAN6921 is latched off. $R_{RT}$ can be determined by:

$$0.8V = (R_{RT} + R_{NTC@OT}) \times 100\mu A \quad (43)$$

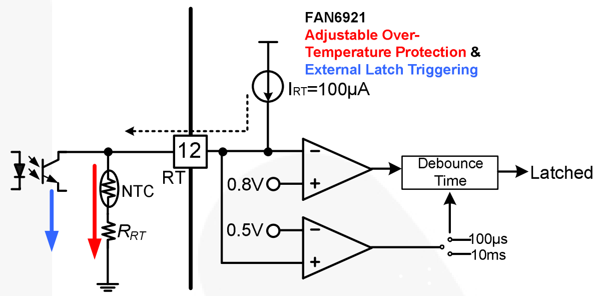


**Figure 18. Adjustable Over-Temperature Protection and External Latched-off Function**

**(Design Example)** Assuming the resistance of NTC at over-temperature protection point is 4.3kΩ;

$$R_{RT} = \frac{0.8V}{100\mu A} - 4.3k\Omega = 3.7k\Omega$$

# Final Schematic of Design Example

This section summaries the final design example. The key system specifications are summarized in Table 1 and the key design parameters are summarized in Table 2. The final schematic is in Figure 19. To have enough hold-up time for $V_{DD}$ during startup, a two-stage circuit is used for $V_{DD}$.

**Table 1. System Specifications**

| Input | |
|---|---|
| Input Voltage Range | 90~264$V_{AC}$ |
| Line Frequency Range | 47~63Hz |
| **Output** | |
| Output Voltage ($V_o$) | 19V |
| Output Power ($P_o$) | 90W |

**Table 2. Key Design Parameters**

| PFC Stage | |
|---|---|
| PFC Output Voltage Level 1 ($V_{O.PFC.L}$) | 260V |
| PFC Output Voltage Level 2 ($V_{O.PFC.L}$) | 400V |
| PFC Inductor ($L_{BOOST}$) | 385µH |
| Turns of PFC Inductor ($N_{BOOST}$) | 60T |
| Turns of ZCD Auxiliary Winding ($N_{ZCD}$) | 8T |
| Minimum Switching Frequency ($f_{S.PFC}^{min}$) | 55kHz |
| **PWM Stage** | |
| Turns of Primary Inductor of PWM Transformer ($N_P$) | 41T |
| Turns of Auxiliary Winding of PWM Transformer ($N_{AUX}$) | 6T |
| Turns Ratio of PWM Transformer (*n*) | 6.8 |
| Primary Inductor ($L_P$) | 700µH |
| Minimum switching Frequency ($f_{s.QR}^{min}$) | 52kHz |

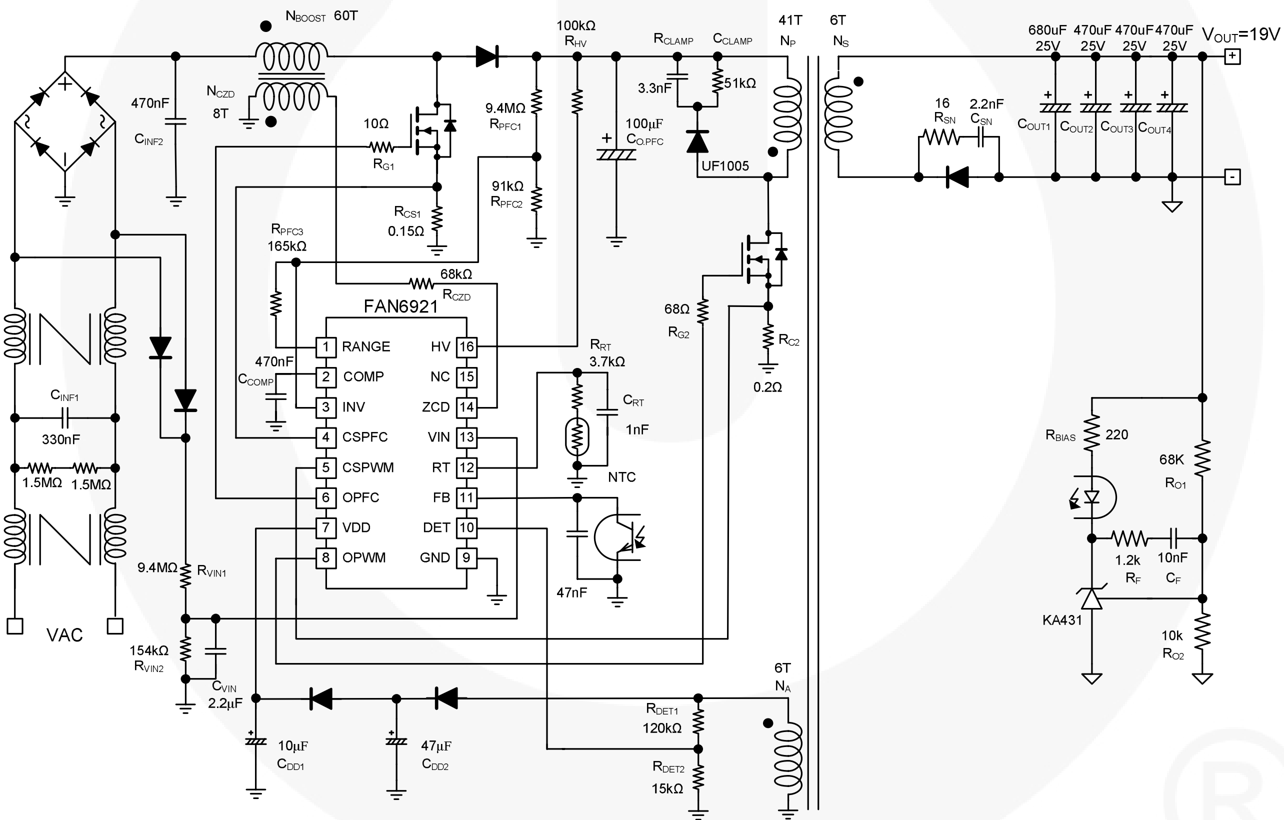


**Figure 19. Final Schematic of Design Example**

## Lab Note

Before modifying or soldering/desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be damaged by external high-voltage.

This device is sensitive to electrostatic discharge (ESD). To improve the production yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

# Printed Circuit Board Layout

Printed circuit board layout and design are very important for switching power supplies where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes EMI and prevents the power supply from being disrupted during surge/ESD tests.

## Guidelines

### IC Side:

- Reference ground of the COMP, INV, CSPFC, and CSPWM pins are connected together and then connect to IC's GND directly.
- Reference ground of VIN, RT, FB, and DET pins are connected to IC's GND directly.
- Small capacitors around IC should be connected to IC directly.
- The trace line of CSPFC, CSPWM, OPFC, and OPWM should not be paralleled and should be close to each other to avoid introducing noise.
- Connections of IC's GND, $C_{Bulk}$'s ground, and auxiliary winding of PWM XFMR:

  **Approach 1:** Auxiliary winding's ground ➔ IC's GND ➔ $C_{Bulk}$'s ground.
  **Approach 2:** IC's GND ➔ Auxiliary winding's ground ➔ $C_{Bulk}$'s ground (Trace **2**➔Trace **1**➔ Trace **3**).
  **Approach 3:** IC's GND ➔ $C_{Bulk}$'s ground and auxiliary winding's ground ➔ $C_{Bulk}$'s ground.

### System Side

### PFC Stage

- Auxiliary winding of PFC choke and $R_{CS,PFC}$ should be connected to $C_{Bulk}$'s ground singly (Trace **4** and Trace **5**).
- Ground of bridge and the C-L-C filter should be connected to $C_{Bulk}$'s ground directly.
- Current loop constructed by the PFC choke, PFC diode, PFC MOSFET, $R_{CS,PFC}$, and $C_{Bulk}$ should be as short as possible (Loop **7**).

### PWM Stage

- $R_{CS}$ should be connected to $C_{Bulk}$'s ground directly. Keep it short and wide (Trace **6**).
- Current loop constructed by the $C_{Bulk}$, XFMR, PWM MOSFET, and $R_{CS}$ should be as short as possible (Loop **8**).
- RCD snubber should be close to XFMR and drain of PWM MOSFET.
- Ground of photo-coupler should be connected to IC's GND.
- On the secondary side, current loop constructed by XFMR, Schottky, and output capacitor should be as short as possible (Loop **9**).
- Connections of Y Capacitor:

  **Approach 1:** Y CAP's primary ground ➔ $C_{Bulk}$'s ground ➔ bridge's ground.
  **Approach 2:** Y CAP's primary ground ➔ bridge's ground ➔ $C_{Bulk}$'s ground.

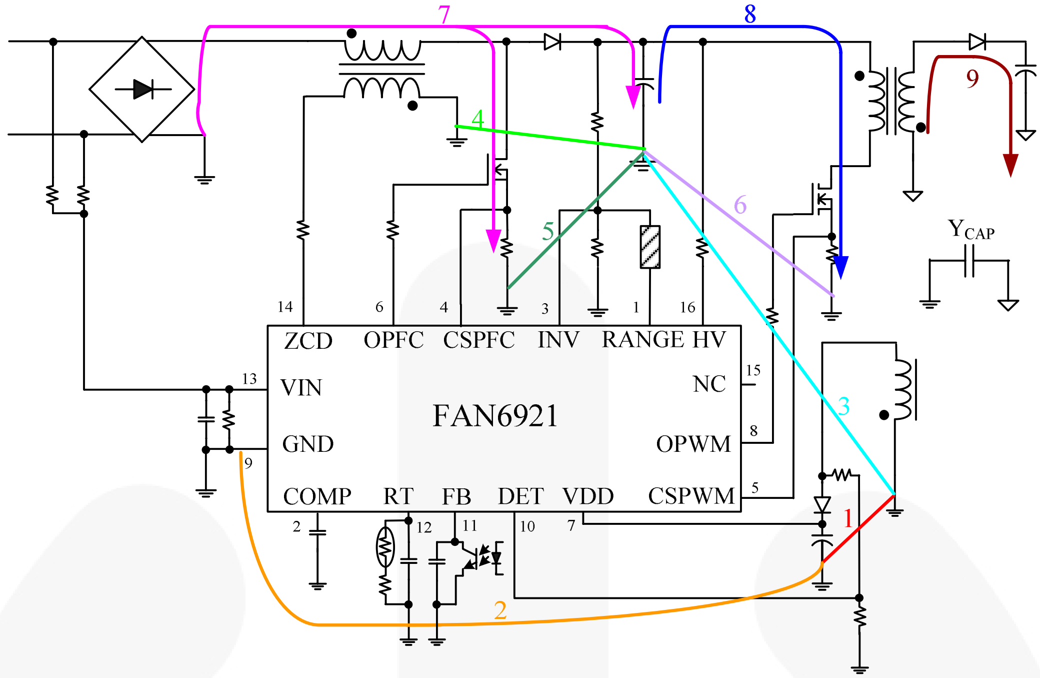


**Figure 20. Layout Considerations**

# Related Documents

*FAN6921MR — Integrated Critical Mode PFC and Quasi-Resonant Current Mode PWM Controller*
*FAN6921ML — Integrated Critical Mode PFC/Quasi-Resonant Current Mode PWM Controller*