1.0 General Description

AMI Semiconductor's AMIS-722402 (PI5002D) contact image sensor (CIS) consists of 1376 active pixels which enables the selection of 2400, 1200, 600, or 300 dots per inch (dpi) resolutions, and employs AMI Semiconductor's proprietary CMOS image sensing technology. The sensor contains an on-chip output amplifier, power down circuitry and parallel transfer features that are uniquely combined with the present-day active-pixel-sensor technology. The image sensors are designed to be cascaded end-to-end on a printed circuit board (PCB) and packaged in an image sensing module. Applications for the sensor array includes facsimiles, PC scanners, check readers, and office automation equipment.

Figure 1 is a block diagram of the sensor, showing 1376 active pixels, their associated multiplexing switches, buffers, and an output amplifier circuit with a power down feature. The sensors pixel-pixel spacing is approximately 10.58µm. The size of each sensor without the scribe lines is 14560µm by 230µm.

2.0 Key Features

- 2400, 1200, 600, and 300dpi selectable resolutions
- 1376 image sensor elements (pixels)
- 10.58µm (2400dpi) pixel center-to-center spacing
- On-chip amplifier
- Single 3.3V power supply
- 3.3V input clocks and control signals
- 3MHz maximum pixel rate
- Parallel / integrate and transfer
- Power-down circuit
- High sensitivity
- Low power
- Low noise

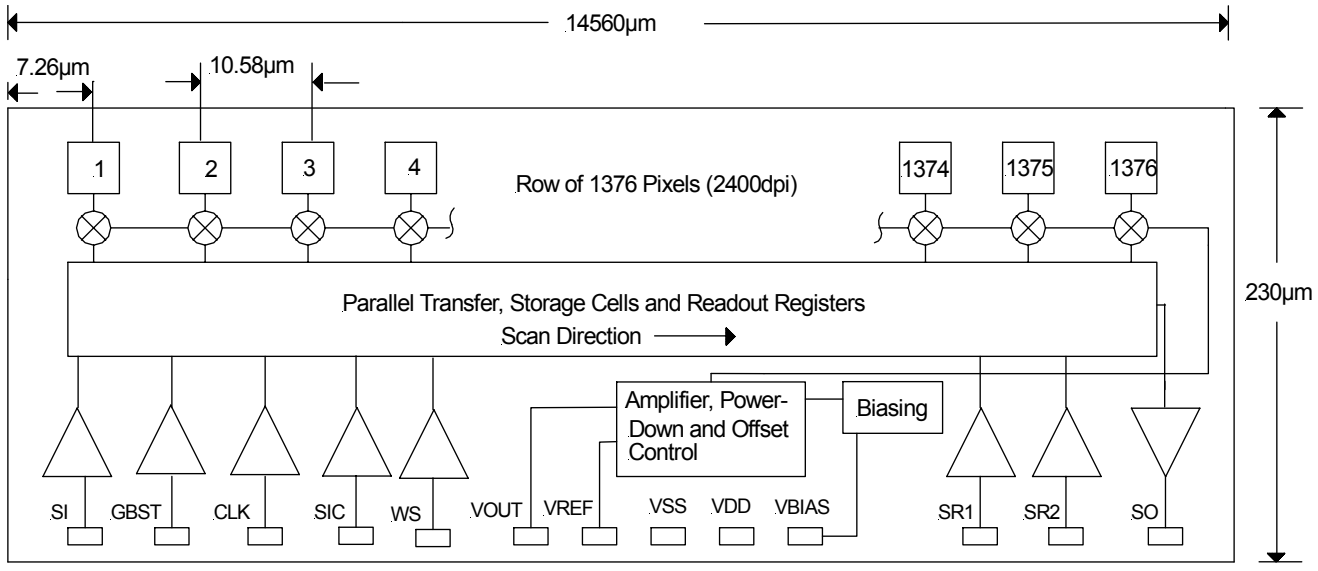


Figure 1: Sensor Block Diagram

3.0 Unique Features

There are six unique features incorporated into the AMIS-722402 which improve the sensor's performance.

3.1 Pixel-to-pixel Offset Cancellation Circuit

The sensor employs a pixel-to-pixel offset cancellation circuit, which reduces the fixed pattern noise (FPN), and amplifier offsets. In addition, this innovative circuit design greatly improves the optical linearity and low noise sensitivity.

3.2 Parallel Integrate, Transfer and Hold

The sensor has a parallel integrate, transfer and hold feature, which allows the sensor to be read out while photon integration is taking place. These features are approached through the use of an integrate-and-hold cell, located at each pixel site. Each pixel's charge is read from its storage site as the sensor's shift register sequentially transfers each pixel's charge onto a common video line.

3.3 Dual Scan Initiation Inputs, GBST and SI

Each sensor has two scan initiation inputs, the global start pulse (GBST) and the start pulse (SI), which are compatible with standard 3.3V CMOS clocks. These clocks help to reduce the sensor-to-sensor transition FPN by initializing and preprocessing all sensors simultaneously before they start their readout scan. The internal shift register starts the scan after GBST is clocked in on the falling edge of the clock input (CLK).

During the first 75 clock cycles following a GBST pulse, all the pixels of all the cascaded sensors cycle through their pre-scan initialization process that reduces FPN and reset noise.

A sequence of cascaded sensors has a unique first sensor and identically behaving subsequent sensors. The start input control (SIC) defines whether a sensor will be the first sensor that self-starts the readout of its pixels or will be a subsequent sensor that waits for the SI before starting the readout of its pixels. With its SIC tied high (Vdd), the first sensor self-starts the readout of its pixels after 75 clock cycles of delay. With their SIC tied low (ground), all of the subsequent sensors delay their readout of their pixels until after they receive a SI pulse. Furthermore, the first sensor's SI is left unconnected, while the subsequent sensors all have their SI connected to the end-of-scan (SO) of their respective preceding sensor. Just prior to finishing its readout of its pixels, each sensor will send a SO pulse to its respective subsequent sensor so that its respective subsequent sensor will continue the readout of pixels without a pause or gap in readout. The external module-level start pulse (SP) is connected to all of the sensors' GBST inputs.

For example in the 2400dpi mode, when the first sensor completes its scan, its SO appears on the rising edge of 1442nd clock cycle after the entry of GBST and nine pixels before its last pixel, in order to have a continuous pixel readout between sensors in a module. This SO enters as the SI clock of the second and subsequent sensors; hence all subsequent sensors will start their register scan after each of the preceding sensors completes its scan.

3.4 Power Saving

Each sensor incorporates a power-saving feature when multiple sensors are cascaded together to form a linear imaging array. When a particular sensor is selected to be read out, the SIC on each sensor selects a unique feature of powering up that sensor's output amplifier and powering it down when not selected.

3.5 Common Reference Voltage between Cascaded Sensors

Each sensor has an input/output bias control (VREF), which serves as an offset voltage reference. Each bias control pad is connected to an internal bias source and tied to its own amplifier's reference bias input. In operation, these pads on every sensor are connected together. Each sensor then "shares" the same bias level to maintain a constant bias among all of the sensors.

3.6 Selectable Resolutions of 2400dpi, 1200dpi, 600dpi, 300dpi

The sensor allows for four selectable resolutions; 2400dpi, 1200dpi, 600dpi, and 300dpi, which are controlled by the select resolution 1 and 2 inputs, (SR1, SR2). The following truth details the conditions of the SR1 and SR2 inputs in order to select each resolution, where low represents the input is connected to ground and a high represents the input connected to Vdd.

In the 2400dpi mode, all 1376 pixels are clocked out, whereas in the 1200dpi mode, Pixels 1 and 2 are combined, 3 and 4 are combined and so on up to Pixels 1375 and 1376 being combined. One half of the pixel amplifiers and one half of the scanning registers are then disabled. As a result, sensitivity in the 1200dpi mode will be twice that of the 2400dpi mode and the 1200dpi readout time will be approximately half of the 2400dpi readout time.

Similarly, in the 600dpi mode, Pixels 1-4 are combined, Pixels 5-8 are combined and so on up to Pixels 1373-1376 being combined. Only one quarter of the pixel amplifiers and shift registers are then used. The 600dpi sensitivity will be four times that of the 2400dpi, and the readout time will be one quarter of the 2400dpi readout time.

In the 300dpi mode, Pixels 1-8 are combined, Pixels 9-16 are combined and so on up to Pixels 1369-1376 being combined. Only one eighth of the pixel amplifiers and shift registers are then used. The 300dpi sensitivity will be eight times that of the 2400dpi, and the readout time will be one eighth of the 2400dpi readout time.

Unlike a CCD array, all of the 2400dpi, 1200dpi, 600dpi, and 300dpi arrays can operate with the same clock frequency.

Table 1: Select Resolution Conditions

Resolution	Select Resolution 1 (SR1)	Select Resolution 2 (SR2)
2400dpi	L	L
1200dpi	L	H
600dpi	H	L
300dpi	H	H

4.0 Functional Description

4.1 Input / Output Terminals

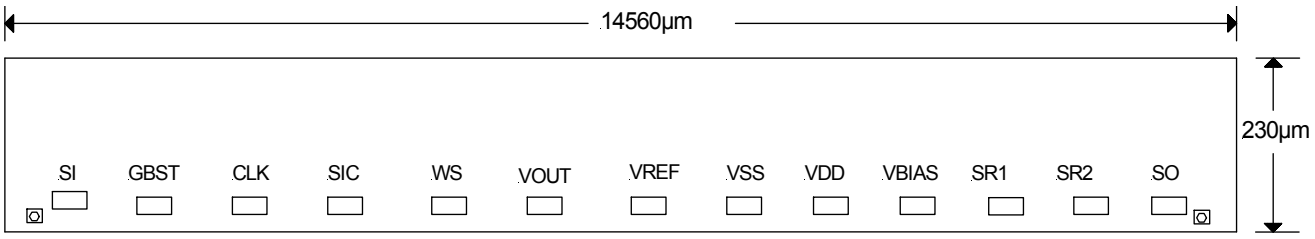
The AMIS-722402 image sensor has 13 pads that become inter-connected when they are cascaded end-to-end on a PCB and packaged in an image sensing module. Their symbols and functions are listed in Table 2.

Table 2: Input and Output Terminals

Signal	I/O	Description
SI	I	Start pulse: Input to start a line scan (see discussion of the sensors unique features for further details)
GBST	I	Global start pulse: Globally initializes the start inputs of all sensors and starts the scanning process of the first sensor (see discussion of the sensors unique features for further details)
CLK	I	Clock: Clock input for the shift register
SIC	I	Start input control: Input to control the Start Pulse to the first sensor (see discussion of the sensors unique features for further details)
WS	I	Waveform select: Selects between two different readout modes, the waveform select input is left unconnected or held high for normal sampling and held low for CDS sampling
VOUT	O	Video output voltage: Output video signal from the chip
VREF	I/O	Reference voltage: Reference input voltage for the amplifier output; sets the output's reset (dark) level
VSS	I	Ground
VDD	I	Power supply
VBIAS	O	Internal bias voltage. This is an internal bias voltage which should be connected via an external decoupling capacitor to Vdd on the modules' PCB for noise reduction. Special care may be required to minimize electro-magnetic interference coupling to this line.
SR1	I	Select resolution 1: Selects the 2400, 1200, 600, or 300dpi modes in conjunction with SR2 (see discussion of the sensors unique features for further details)
SR2	I	Select resolution 2: Selects the 2400, 1200, 600, or 300dpi modes in conjunction with SR1 (see discussion of the sensors unique features for further details)
SO	O	End of scan pulse: Output from the shift register at the end of a scan

4.2 Bonding Pad Layout Diagram

Figure 2 shows the bonding pad locations for the AMIS-722402 sensor.

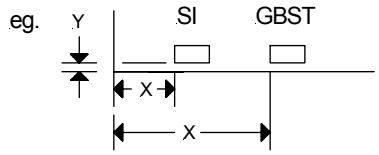


Pad Location Table

Pad	Location	Y	X
SI	Start Pulse	20	2127
GBST	Global Start Pulse	20	2379
CLK	Clock	20	2633
SIC	Start Input Control	20	2890
WS	Waveform Select	20	3826
VOUT	Video Output Voltage	20	4077
VREF	Reference Voltage	20	6084
VSS	Ground	20	6428
VDD	Power Supply	20	7393
VBIAS	Chip Bias Voltage	20	10960
SR1	Select Resolution 1	20	11214
SR2	Select Resolution 2	20	11468
SO	End of Scan Pulse	20	12103

Notes:

1. The drawing is not to scale.
2. The die length and width are given in the above sensor die figure
3. Pad locations are listed in the Pad Location Table



4. Each pad is 100 x 70um
5. All dimensions are in um
6. Die size does not include the scribe line

Figure 2: AMIS-722402 Bonding Pad Layout

4.3 Wafer Scribe Line

Figure 3 outlines the scribe line dimensions surrounding the sensor die on a wafer.

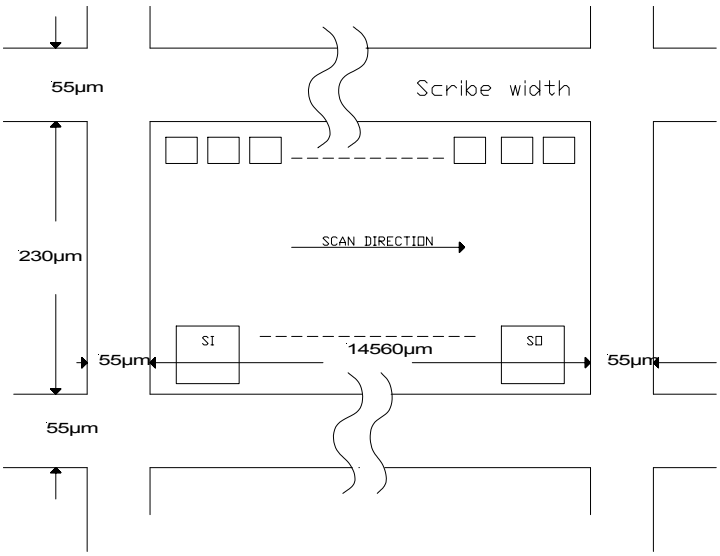


Figure 3: Wafer Scribe Line

5.0 Electro-Optical Specifications

Table 3 lists the electro-optical specifications of the AMIS-722402 sensor at 25°C and Vdd = 3.3V.

Table 3: Electro-Optical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units
Number of pixels [1] @ 2400dpi @ 1200dpi @ 600dpi @ 300dpi		 1376 688 344 172		 1376 688 344 172	
Pixel-to-pixel spacing [1] @ 2400dpi @ 1200dpi @ 600dpi @ 300dpi		 10.58 21.16 42.32 84.64		 10.58 21.16 42.32 84.64	 µm µm µm µm
Dark output voltage level [2]	Vd		0.35		V
Dark output non-uniformity [3]	Ud			80	mV
Photo-response non-uniformity [4]	Up			±15	%
Adjacent photo-response non-uniformity [5]	Upn			±15	%
Sensor-to-sensor photo-response non-uniformity [6]	Usensor			±10	%
Saturation voltage [7]	VSat	0.9	1.2		Volts
Sensitivity [8] @ 300dpi @ 600dpi @ 1200dpi @ 2400dpi	Sv		 2440 1220 610 305		 V/µJ/cm^2 V/µJ/cm^2 V/µJ/cm^2 V/µJ/cm^2
Photo response linearity, between lower and upper end of the linear range (approx range of. 0.1-0.75V) [9]	PRL			2	%
Individual pixel noise (rms) [10] @ 2400dpi @ 1200dpi @ 600dpi @ 300dpi	P_noise		 2.5 3.5 4.5 5.5		 mV mV mV mV
Average pixel noise (rms) [11] @ 2400dpi @ 1200dpi @ 600dpi @ 300dpi	Pavg_noise		 2.5 3.5 4.5 5.5	 3 4 5 6	 mV mV mV mV
Row noise, without external sources (rms) [12] @ 2400dpi @ 1200dpi @ 600dpi @ 300dpi	Row_noise		 0.50 0.50 0.75 1.00		 mV mV mV mV
Wafer thickness		280	300	320	µm

Notes for Table 3 are listed on the next page under “Definitions of Electro-Optical Specifications”.

5.1 Definitions of Electro-optical Specifications

All electrical specifications will be measured at a pixel rate of 3.0MHz, a temperature of 25°C, Vdd = 3.3V, Vref = 0.35V and at an integration time of 0.9ms for 300dpi, 1.8ms for 600dpi, 3.76ms for 1200dpi, and 7.2ms for 2400dpi. The average output voltage Vpavg, which is defined as the voltage difference between the average pixel level in the light and the average pixel level in the dark, will be adjusted to approximately 1.0V, unless stated otherwise. A linear array of uniform green LED's will be used as the light source for measurements requiring illumination, unless stated otherwise. As a guideline, the recommended load on the output should be 1KΩ<RL<10kΩ. All measurements will be taken with a 2kΩ load on the output.

1. Selectable resolutions.
   The sensor allows for four selectable resolutions; 2400dpi, 1200dpi, 600dpi, and 300dpi, which are controlled by the SR1 and SR2 inputs. Table 1 details how each resolution mode is selected. In the 2400dpi mode, all 1376 pixels are clocked out, whereas in the 1200dpi mode, Pixels 1 and 2 are combined, 3 and 4 are combined and so on up to Pixels 1375 and 1376 being combined. One half of the pixel amplifiers and one half of the scanning register are then disabled. As a result, sensitivity in the 1200dpi mode will be twice that of the 2400dpi mode and the 1200dpi readout time will be approximately half of the 2400dpi readout time. Similarly, in the 600dpi mode, Pixels 1-4 are combined, Pixels 5-8 are combined and so on up to Pixels 1373-1376 being combined. Only one quarter of the pixel amplifiers and shift registers are then used. The 600dpi sensitivity will be four times that of the 2400dpi, and the readout time will be one quarter of the 2400dpi readout time. In the 300dpi mode, Pixels 1-8 are combined, Pixels 9-16 are combined and so on up to Pixels 1369-1376 being combined. Only one eighth of the pixel amplifiers and shift registers are then used. The 300dpi sensitivity will be eight times that of the 2400dpi, and the readout time will be one eighth of the 2400dpi readout time.
2. Dark output voltage (Vd).
   Vd is the average dark output level and is essentially the offset level of the video output in the dark. The dark level is set by the voltage on VREF and is recommended to be set externally to a voltage of 0.35V for optimal module operation.
3. Dark output non-uniformity (Ud).
   Ud = Vdmax-Vdmin, where Vdmax is the maximum pixel output voltage in the dark and Vdmin is the minimum pixel output voltage in the dark.
4. Photo-response non-uniformity (Up).
   Up = ((Vpmax-Vpavg)/Vpavg) x 100% or ((Vpavg-Vpmin)/Vpavg) x 100%, whichever is the greater, where Vpmax is the maximum pixel output voltage in the light, Vpmin is the minimum pixel output voltage in the light and Vpavg is average output voltage of all pixels in the light.
5. Adjacent photo-response non-uniformity (Upn).
   Upn = Max ((Vpn, Vpn+1) / Min (Vpn, Vpn+1)) x 100%, where Vpn is the pixel output voltage of pixel n in the light.
6. Sensor-to-sensor photo-response non-uniformity (Usensor).
   Usensor = (Vpavg - Wavg) / Wavg), where Wavg is the average output of all sensors on the same wafer that pass all other specifications.
7. Saturation voltage (VSat) is defined as the maximum video output voltage swing measured from the dark level to the saturation level. It is measured by using the module LED light source with the module imaging a uniform white target. The LED light level is increased until the output voltage no longer increases with an increase in the LED brightness. The dark level is set by the voltage on VREF and is recommended to be set externally to a voltage of 0.35V for optimal module operation.
8. Sensitivity (Sv) is defined as the slope of the Vpavg vs. Exposure curve.
9. Photo-response linearity (PRL).
   Photo-response linearity is defined as the max. deviation of response compared to a best fit line as a percentage of full scale, where full scale is the maximum value of the linearity range of operation; approx 0.75V. Photo-response linearity is specified within the linearity range of operation, approx 0.1-0.75V.
10. Individual pixel noise in rms (P_noise).
    The individual pixel noise in rms is defined as the standard deviation of each pixel in the dark. The maximum of all pixel standard deviations is the maximum individual pixel noise in rms. This can also be thought of as output referred noise as it is measured at the sensor output.
11. Average pixel noise in rms (Pavg_noise).
    The average pixel noise in rms is defined as the average of all pixel standard deviations in the dark. A 2.5mV rms value has a peak-peak equivalent of 15mV. This can also be thought of as output referred noise as it is measured at the sensor output.
12. Row noise in rms (Row_noise)
    Each chip is binned into four equal bins and the row noise in rms is defined as the standard deviation of each bin. The row noise specification does not include any noise due to external sources.

6.0 Recommended Operating Conditions

Table 4 lists the recommended operating conditions @ 25°C.

Table 4: Recommended Operating Conditions @ 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd	3.0	3.3	3.6	V
Clock input voltage high level (1)		2.4	3.3	3.6	V
Clock input voltage low level (1)		0	0	0.8	V
Power supply current	IDD (sensor during readout) IDD (sensor between readouts) IDD (15 chip module)		8 3.0 50	12 4.5 75	mA mA mA
Reference voltage (2)	VREF	0	0.35	0.8	V
Clock frequency (3)		0.5	2.5	3.0	MHz
Pixel rate (4)		0.5	2.5	3.0	MHz
Integration time @ 2400dpi (line scan rate) (5) First die Subsequent die	Tint	 477 459			 µs µs / die
Clock pulse duty cycle (6)			50		%

Notes:

1. Applies to all clocks; GBST, SI and CLK.
2. The dark level is set by the voltage on VREF and is recommended to be set externally to a voltage of 0.35V for optimal module operation.
3. Although the device will operate with a pixel rate of less than 500kHz, it is recommended that the device be operated above 500kHz to maintain performance characteristics. Operating below 500kHz may result in leakage current degradation.
4. One pixel is clocked out for every clock cycle.
5. Tint is the integration time of a single sensor and is the time between two SIs. The minimum integration time is the time it takes to clock out 75 inactive pixels and 1376 active pixels for the 2400dpi mode, 75 inactive pixels and 688 active pixels for the 1200dpi mode, 75 inactive pixels and 344 active pixels for 600dpi mode, 75 inactive pixels and 172 active pixels for 300dpi mode, at a given frequency.

   However, if several sensors are cascaded together in a module then the minimum integration time for the 2400dpi mode is the time it takes to clock out 75 inactive pixels and 1376 active pixels from the first sensor and 1376 pixels from each of all subsequent sensors, at a given frequency.

   For cascaded sensors in the 1200dpi mode, the minimum integration time is the time it takes to clock out 75 inactive pixels and 688 active pixels from the sensor and 688 pixels from each of all subsequent sensors, at a given frequency.

   Similarly, for cascaded sensors in the 300dpi mode, the minimum integration time is the time it takes to clock out 75 inactive pixels and 172 active pixels from the first sensor and 172 pixels from each of all subsequent sensors, at a given frequency.
6. The clock duty cycle is defined as the ration of the positive duration of the clock to its period.

7.0 Absolute Maximum Ratings

Table 5 lists the absolute maximum ratings.

Table 5: Absolute Maximum Ratings

Parameter	Max.	Units
Power supply voltage (Vdd)	5	V
Clock input voltage high level (1)	Vdd + 0.2	V
Clock input voltage low level (1)	-0.5	V
Operating temperature	-10 to +50	°C
Operating humidity	+10 to +85	RH%
Storage temperature	-25 to +75	°C
Storage humidity	+10 to +90	RH%

Note:

1. Applies to all clocks; GBST, SI and CLK.

8.0 Timing Requirements

Table 6 lists the timing requirements for all four resolution modes, and their associated timing diagrams are shown in Figures 4-9.

Table 6: Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock (CLK) period	CLKp	330	400	2000	ns
Clock (CLK) pulse width	CLKpw		200		ns
Clock (CLK) duty cycle			50		%
Data setup time (1)	Tset	20			ns
Data hold time (1)	Thold	25			ns
Clock (CLK) rise time (2)	CLKrt	70			ns
Clock (CLK) fall time (2)	CLKft	70			ns
End-of-scan (SO) rise time (2)	SOrt			50	ns
End-of-scan (SO) fall time (2)	SOft			50	ns
Global start (GBST) rise time (3)	GBSTrt	70			ns
Global start (GBST) fall time (3)	GBSTft	70			ns
Pixel rise time (4,5)	Prt			100	ns
Pixel fall time (4,5)	Pft			30	ns

Notes:

1. The shift register will load on all falling CLK edges, so setup and hold times (Tset, Thold) are needed to prevent the loading of multiple start pulses. This would occur if the GBST remains high during two fallings edges of the CLK signal. See Figure 8.
2. SI starts the register scanning and the first active pixel is read out on the 76th clock of the CLK signal. However, when multiple sensors are sequentially scanned, as in CIS modules, the SO from the predecessor sensor becomes the SI to the subsequent sensor, hence the SI clock = the SO clock.
3. As discussed under the third unique feature, the GBST starts the initialization process and preprocesses all sensors simultaneously in the first 75 clock cycles before the first pixel is scanned onto the video line from the first sensor.
4. The transition between pixels does not always reach the dark offset level as shown in the timing diagrams, see Vout. The timing diagrams show the transition doing so for illustration purposes; however a stable pixel sampling point does exist for every pixel.
5. The pixel rise time is defined as the time from when the CLK's rising edge has reached 50 percent of its maximum amplitude to the point when a pixel has reached 90 percent of its maximum amplitude. The pixel fall time is defined as the time from when the CLK's falling edge has reached 50 percent of its maximum amplitude to the point when a pixel has reached 10 percent of its maximum amplitude.

Figures 4, 5, 6, and 7 show the initialization of the first sensor in relation to its subsequent cascaded sensors for all four resolution modes. The SIC selects the first sensor to operate with 75 clock cycles of delay by connecting it to Vdd on the first sensor and to Ground for all of the subsequent sensors. Hence the first sensor will operate with 75 inactive pixels being clocked out before its first active pixel is clocked out.

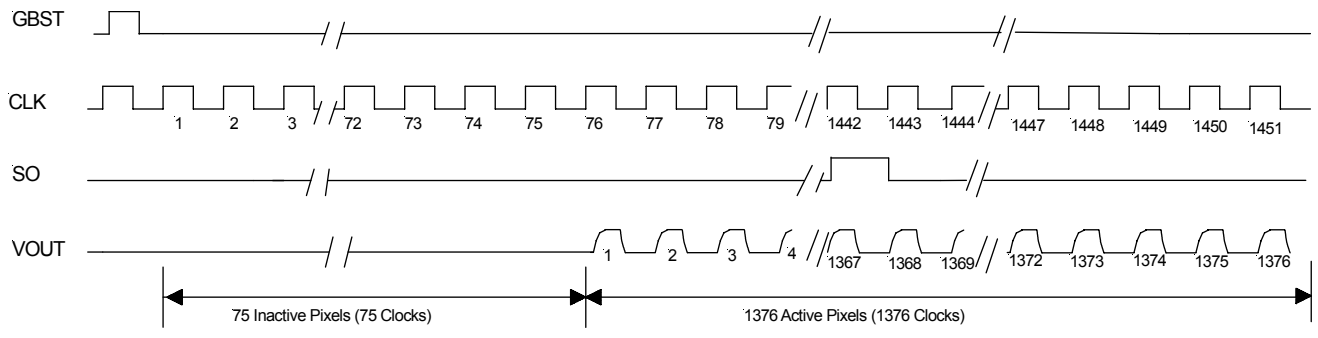


Figure 4: Overall Timing Diagram for the 2400dpi Mode

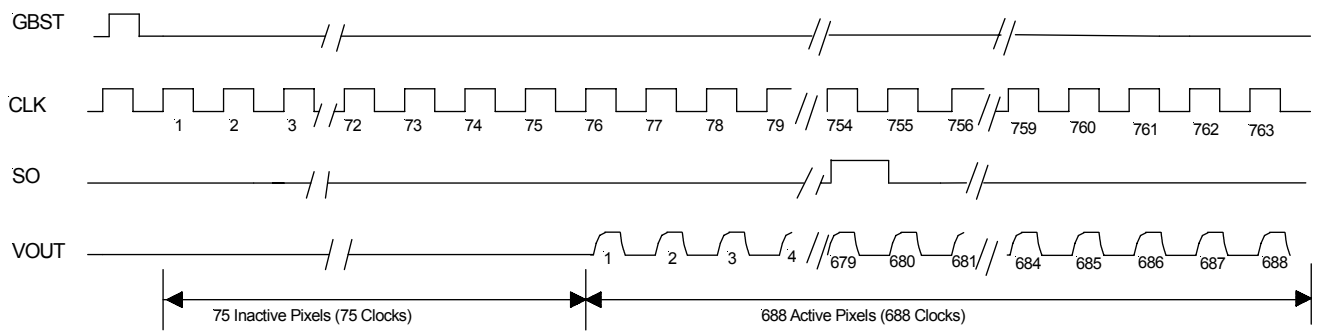


Figure 5: Overall Timing Diagram for the 1200dpi Mode

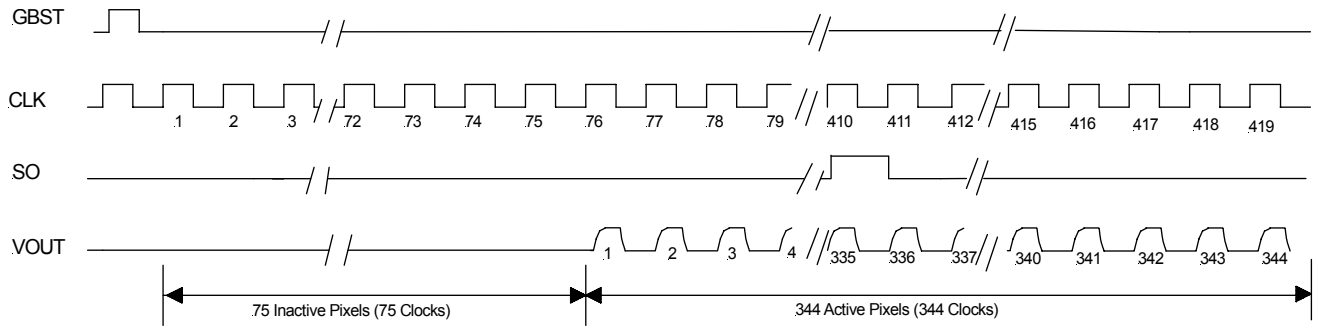


Figure 6: Overall Timing Diagram for the 600dpi Mode

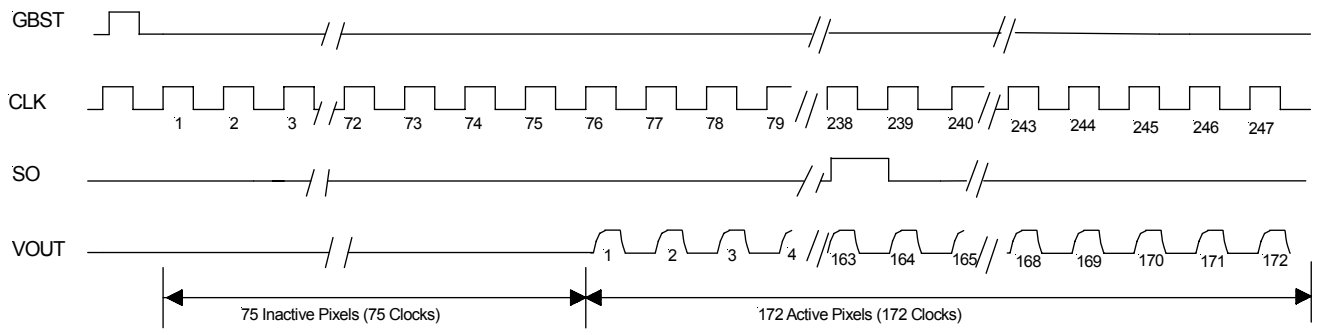


Figure 7: Overall Timing Diagram for the 300dpi Mode

Figures 8 and 9 detail the timing of the CLK, GBST, Vout, and SI/SO signals in further detail, which have the same timing requirements for the 2400, 1200, 600, and 300dpi modes. The rise and fall times are listed in Table 6. In Figure 8, note that Pixel 76 is the first active pixel, as the first 75 pixels are dummy pixels.

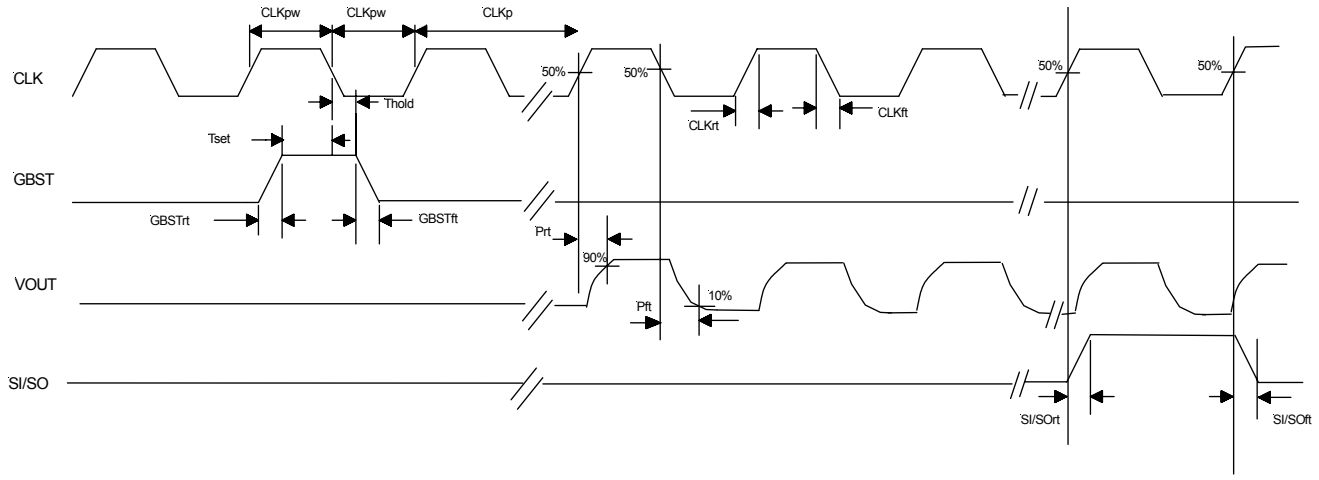


Figure 8: Rise and Fall Times for both the 2400, 1200, 600, 300dpi Modes

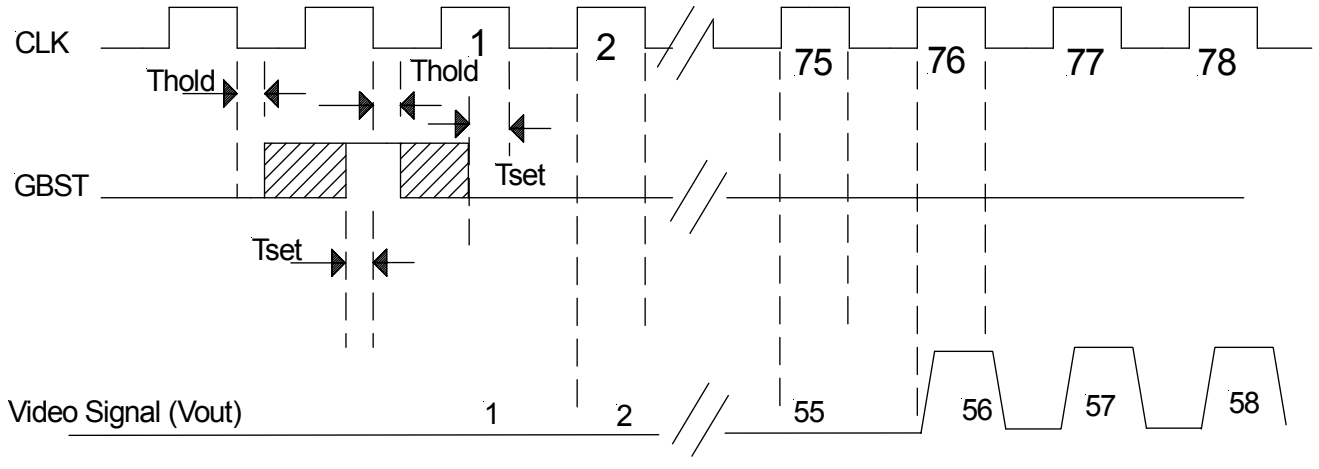


Figure 9: Timing of GBST-to-first Pixel of the First Sensor for 2400, 1200, 600, 300dpi Modes

Figures 10 to 13 show the timing of the SI/SO. At 2400dpi the SI/SO comes out in line with the 1367th pixel, at 1200dpi it comes out in line with the 679th pixel, at 600dpi it comes out in line with the 335th pixel, and at 300dpi it comes out in line with the 163rd pixel.

The SO from the first sensor enters as the SI clock of the second and subsequent sensors; hence all subsequent sensors will start their register scan after each of the preceding sensors completes its scan.

The last active pixel of each sensor is the 1376th pixel for the 2400dpi mode, the 688th pixel for the 1200dpi mode, 344th pixel for the 600dpi mode, and 172nd pixel for the 300dpi mode.

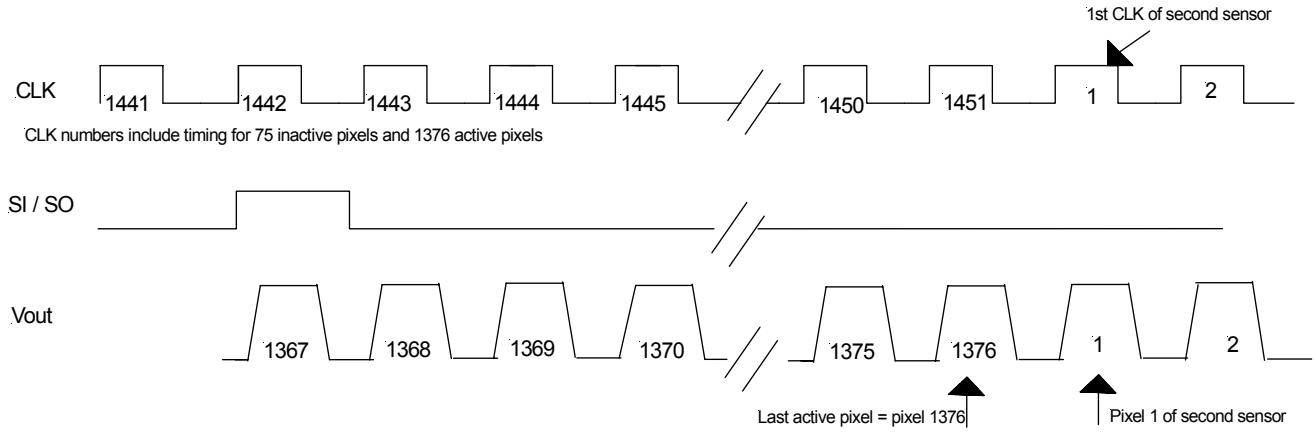


Figure 10: Timing of SI/SO Clock for the 2400dpi Mode

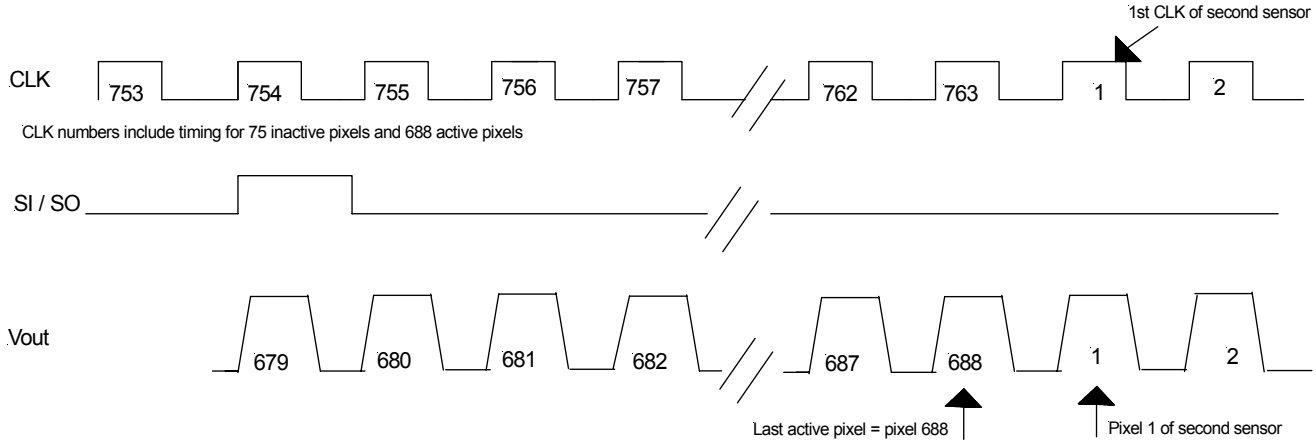


Figure 11: Timing of SI/SO Clock for the 1200dpi Mode

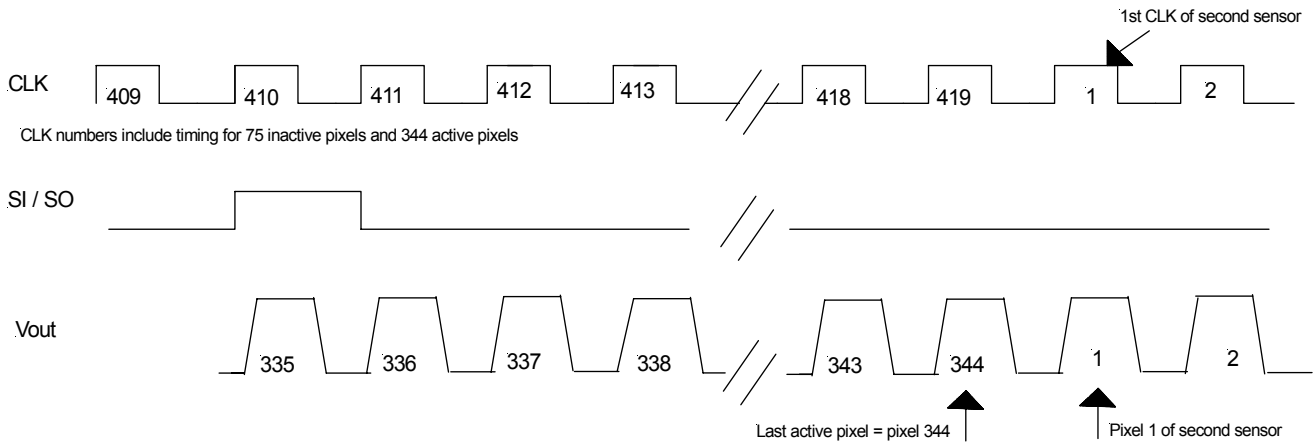


Figure 12: Timing of SI/SO Clock for the 600dpi Mode

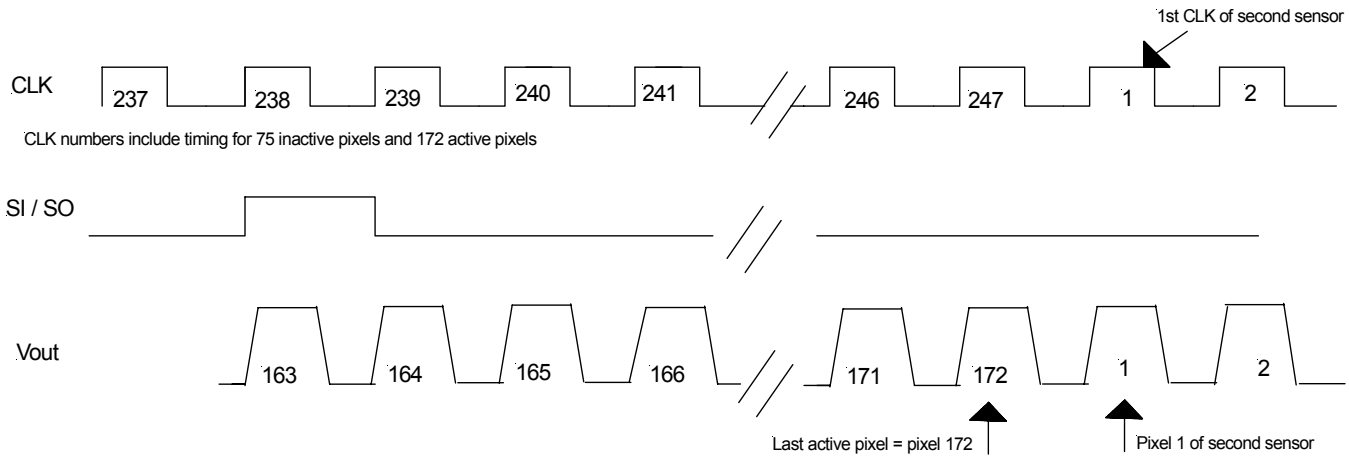


Figure 13: Timing of SI/SO Clock for the 300dpi Mode

9.0 Example of a CIS Module Using Cascaded AMIS-722402 Image Sensors

Figure 14 shows the proposed PCB schematic of the 15 chip CIS module.

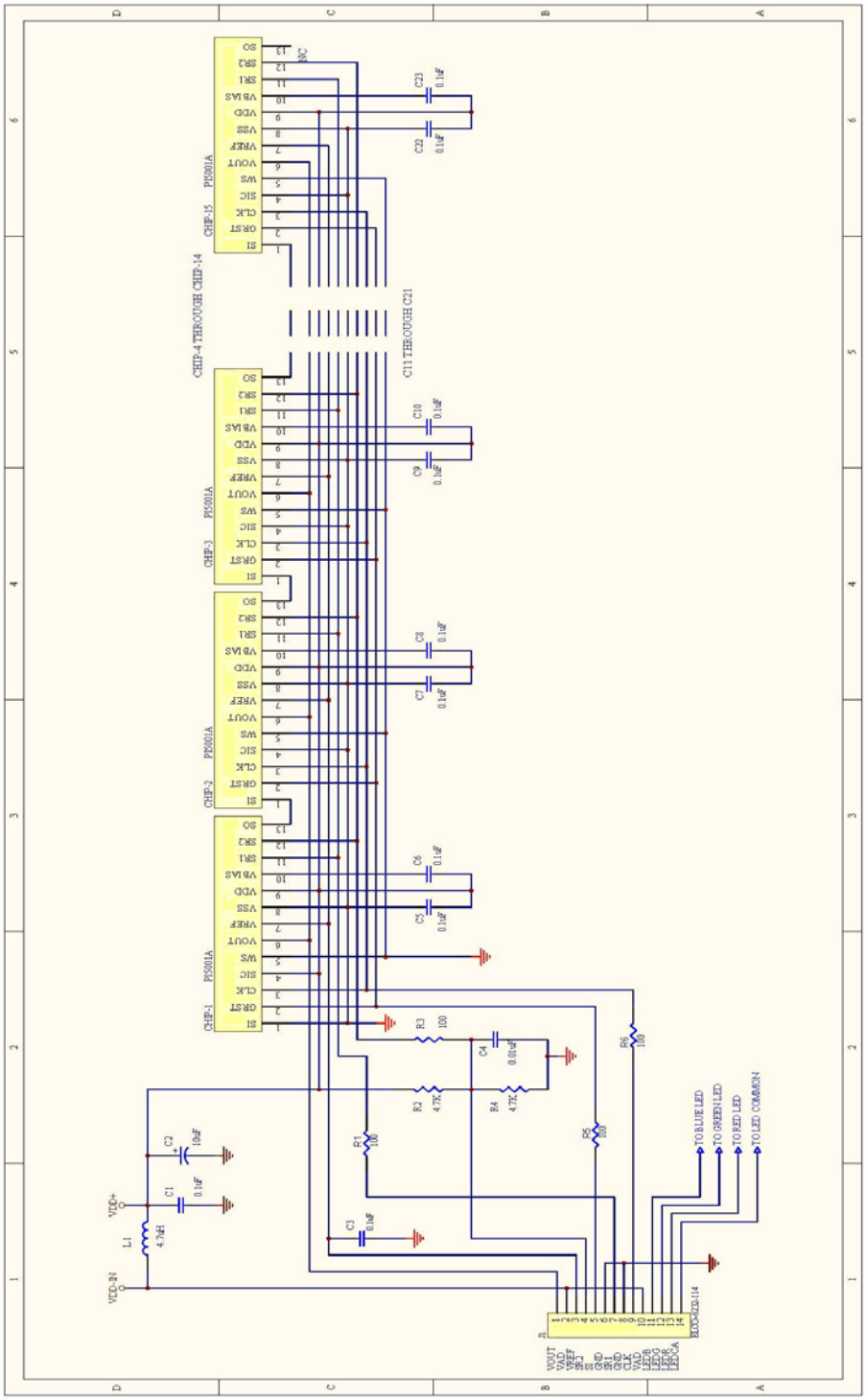


Figure 14: CIS Module with AMIS-722402 Image Sensors

10.0 Company or Product Inquiries

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