1.0 General Description

AMI Semiconductor's AMIS-720649 (PI6049A) contact image sensor (CIS) is a 600 dots per inch (dpi) resolution linear image sensor, which employs AMI Semiconductor's proprietary CMOS image sensing technology. The sensor contains an on-chip output amplifier, power down circuitry and parallel transfer features that are uniquely combined with present-day active-pixel-sensor technology. The image sensors are designed to be cascaded end-to-end on a printed circuit board (PCB) and packaged in an image sensing module. Applications for the sensor array include facsimiles, PC scanners, check readers, and office automation equipment.

Figure 1 is a block diagram of the sensor. Each sensor consists of 344 active pixels, their associated multiplexing switches, buffers and an output amplifier circuit with a power-down feature. The detector's element-to-element spacing is approximately 42.3µm. The size of each sensor without the scribe lines is 14560µm by 380µm.

2.0 Block Diagram

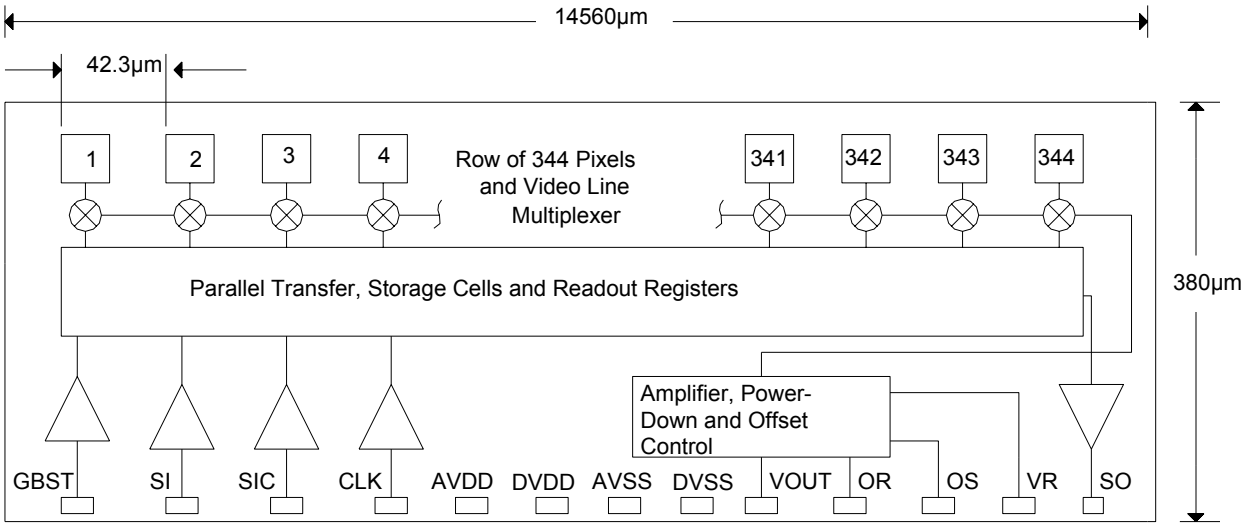


Figure 1: Sensor Block Diagram

3.0 Key Features

- 600dpi
- 344 image sensor elements (pixels)
- 42.3μm pixel center-to-center spacing (23.62dots/mm)
- On-chip amplifier
- Single 5.0V power supply
- 5.0V input clocks
- 2.5MHz maximum pixel rate
- Parallel / integrate and transfer
- Power-down circuit
- High sensitivity
- Low power
- Low noise

4.0 Unique Features

There are five unique features incorporated in the AMIS-720649 which improve the sensor's performance.

4.1 Pixel-to-Pixel Offset Cancellation Circuit

The sensor employs a pixel-to-pixel offset cancellation circuit, which reduces the fix pattern noise (FPN), and amplifier offsets. In addition, this innovative circuit design greatly improves the optical linearity and low noise sensitivity.

4.2 Parallel Integrate, Transfer and Hold

The sensor has a parallel integrate, transfer and hold feature, which allows the sensor to be read out while photon integration is taking place. These features are approached through the use of an integrate and hold cell, located at each pixel site. Each pixel's charge is read from its storage site as the sensor's shift register sequentially transfers each pixel's charge onto a common video line.

4.3 Dual Scan Initiation Inputs, GBST and SI

Each sensor has two scan initiation inputs, the global start pulse (GBST) and the start pulse (SI). These clocks help to reduce the sensor-to-sensor transition fix pattern noise by initializing and preprocessing all sensors simultaneously before they start their readout scan. The internal shift register starts the scan after GBST is clocked in on the falling edge of the clock input (CLK).

The start input control (SIC) selects the first sensor in a sequence of cascaded sensors to operate with 29 clock cycles of delay by connecting it to Vdd on the first sensor, and to ground for all subsequent sensors. Then, only the first sensor clocks out 29 inactive pixels before accessing its first active pixel. During these 29 clock cycles, the first sensor and all of the subsequent cascaded sensors cycle through their pre-scan initialization process. After initialization, only the first sensor starts its read cycle with its first-active pixel appearing on the 30^{th} clock cycle. The second and subsequent sensors await the entry of their SI. Furthermore, the first sensor's SI is left unconnected, while the subsequent sensors all have their SI's connected to the end-of-scan (SO) of their respective preceding sensor. The external scan SI is connected to all of the sensors' GBST inputs.

As the first sensor completes its scan, its SO, appears one pixel before its last pixel. The second and subsequent sensors will then start their registers one clock cycle before the appearance of their respective first pixels, and their SO also appears one pixel before their last pixel.

4.4 Power Saving

Each sensor incorporates a power-saving feature when multiple sensors are cascaded together to form a linear imaging array. The SIC on each sensor selects a unique feature of powering up a particular sensor's output amplifier when it's selected and powering it down when not selected. For the AMIS-720649, only the first sensors' amplifier is used and all subsequent sensors have their amplifiers turned off. The pixels from each sensor are transferred onto a common video line which is connected to the amplifier of the first sensor. The advantage of using only one active amplifier is two-fold; saving on power consumption and reducing sensor-to-sensor FPN.

4.5 Common Reference Voltage Between Cascaded Sensors

Each sensor has an input/output bias control (VR), which serves as an offset voltage reference. Each bias control pad is connected to an internal bias source and tied to its own amplifier's reference bias input. In operation, these pads on every sensor are connected together. Each sensor then "shares" the same bias level to maintain a constant bias among all of the sensors.

5.0 Functional Description

5.1 Input / Output Terminals

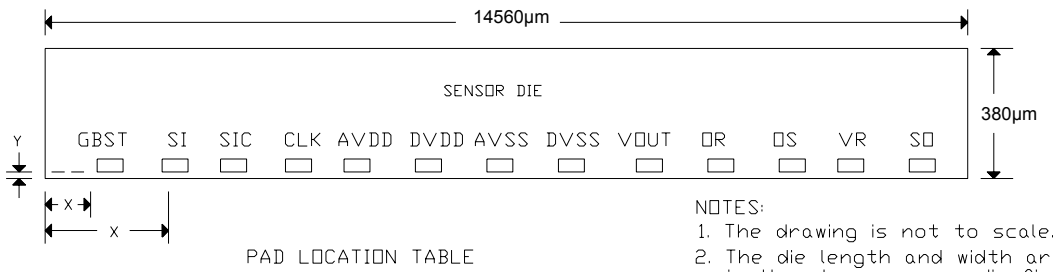
The AMIS-720649 image sensor has 13 input and output (I/O) pads. Their symbols and function descriptions are listed in Table 1.

Table 1: Input and Output Terminals

Symbol	I/O	Description
GBST	I	Global start pulse: Globally initializes the start inputs of all sensors and starts the scanning process of the first sensor. (See discussion of the sensors unique features for further details)
SI	I	Start pulse: Input to start a line scan. (See discussion of the sensors unique features for further details)
SIC	I	Start input control: Input to control the start pulse to the first sensor. (See discussion of the sensors unique features for further details)
CLK	I	Clock: Clock input for the shift register.
AVDD	I	Analog power supply
DVDD	I	Digital power supply
AVSS	I	Analog signal ground
DVSS	I	Digital signal ground
VOUT	O	Video output voltage: Output video signal from the amplifier.
OR	O	Differential reference output
OS	O	Differential video output
VR	I	Reference voltage: Reference input voltage for the amplifier output, sets the output's reset (dark) level.
SO	O	End of scan pulse: Output from the shift register at the end of a scan.

5.2 Bonding Pad Layout Diagram

Figure 2 shows the bonding pad locations for the AMIS-720649 sensor.

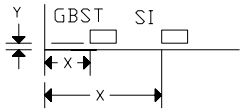


PAD LOCATION TABLE

PAD	FUNCTION	Y	X
GBST	Global Start Pulse	31	499
SI	Start Pulse	31	907
SIC	Start Input Control	31	3746
CLK	Clock	31	4489
AVDD	Analog Power Supply	35	5535
DVDD	Digital Power Supply	39	6432
AVSS	Analog Signal Ground	34	7317
DVSS	Digital Signal Ground	39	7885
VOUT	Video Output Voltage	31	8322
OR	Diff Ref Output	31	9922
OS	Diff Video Output	31	11810
VR	Reference Voltage	31	12207
SO	End of Scan Pulse	32	13970

NOTES:

1. The drawing is not to scale.
2. The die length and width are given in the above sensor die figure
3. Pad locations are listed in the Pad Location Table



4. Each pad is 120 x 80um
5. All dimensions are in um
6. Die size does not include the scribe line

Figure 2: Bonding Pad Locations

5.3 Wafer Scribe Line

Figure 3 outlines the scribe line dimensions surrounding the sensor die on a wafer.

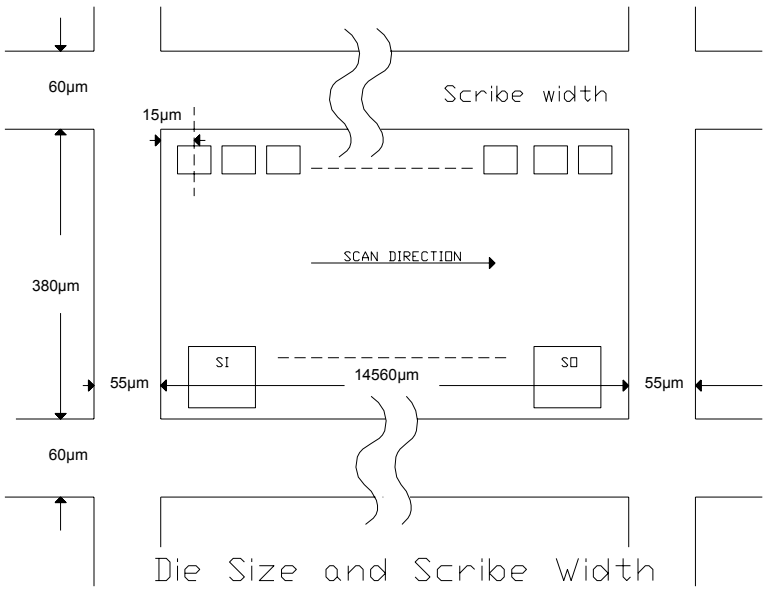


Figure 3: Wafer Scribe Line

6.0 Electro-Optical Specifications

Table 2 lists the electro-optical specifications of the AMIS-720649 sensor at 25°C and Vdd = 5.0V.

Table 2: Electro-Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Units
Number of pixels		344		344	
Pixel-to-pixel spacing		42.3		42.3	µm
Sensitivity (1)	Sv		665		V / µJ / cm^2
Saturation voltage (2)	Vsat		2.0		V
Photo-response non-uniformity (3)	Up			7.5	%
Adjacent photo-response non-uniformity (4)	Upn			7.5	%
Dark output voltage level (5)	Vd		0.7		V
Dark output non-uniformity (6)	Ud			100	mV
Random thermal noise (rms) (7)	Vno		4		mV
Sensor-to-sensor photo-response non-uniformity (8)	Usensor			7.5	%
Photo response linearity (9)	PRL			2.0	%

Notes for Table 2 are listed on the next page under “Definitions of Electro-Optical Specifications”.

6.1 Definitions of Electro-Optical Specifications

All electrical specifications are measured at a pixel rate of 2.0MHz, a temperature of 25°C, Vdd = 5.0V, and at an integration time of 2.2ms. The average output voltage (Vpavg), is adjusted to approximately 1.0V, unless stated otherwise. The modules' internal green LED (525 ± 20nm) was used as the light source for measurements requiring illumination. As a guideline, the recommended load on the output should be 1KΩ<RL<10kΩ. All measurements were taken with a 2kΩ load on the output.

1. Sensitivity (Sv) is defined as the slope of the Vpavg vs. Exposure curve.
2. Saturation voltage (VSat) is defined as the maximum video output voltage swing measured from the dark level to the saturation level. It is measured by using the module LED light source with the module imaging a uniform white target. The LED light level is increased until the output voltage no longer increases with an increase in the LED brightness. The dark level is set by the voltage on VR and in a typical CIS module application, sits at approximately 0.7V.
3. Photo-response non-uniformity (Up): Up = ((Vpmax-Vpavg)/Vpavg) x 100% or ((Vpavg-Vpmin)/Vpavg) x 100%, whichever is the greater, where Vpmax is the maximum pixel output voltage in the light, Vpmin is the minimum pixel output voltage in the light and Vpavg is average output voltage of all pixels in the light.
4. Adjacent photo-response non-uniformity (Upn): Upn = Max ((Vpn – Vpn+1) / Min (Vpn, Vpn+1)) x 100%, where Vpn is the pixel output voltage of pixel n in the light.
5. Dark output voltage (Vd): Vd is the average dark output level and is essentially the offset level of the video output in the dark. The dark level is set by the voltage on VR and in a typical CIS module application, sits at approximately 0.7V.
6. Dark output non-uniformity (Ud): Ud = Vdmax-Vdmin, where Vdmax is the maximum pixel output voltage in the dark and Vdmin is the minimum pixel output voltage in the dark.
7. Random thermal noise (rms), (Vno), is the standard deviation of n pixels in the dark. A sample size n= 64 was used. A 4mV rms value has a peak-peak equivalent of 24mV.
8. Sensor-to-sensor photo-response non-uniformity (Usensor): Usensor = (Vpavg – Wavg) / Wavg), where Wavg is the average output of all sensors on the same wafer that pass all other specifications.
9. Photo-response linearity (PRL): Photo-response linearity is defined as the max deviation of response compared to a best fit line. The data points plotted are those that lie within ten percent of the saturation level and ninety percent of the saturation level. Outside these ranges the module is operating close to non-linearity.

7.0 Recommended Operating Conditions

Table 3 lists the recommended operating conditions @ 25°C.

Table 3: Recommended Operating Conditions @ 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd	4.5	5.0	5.5	V
Clock input voltage high level (1)		2.8	Vdd	Vdd	V
Clock input voltage low level (1)		0	0	0.8	V
Power supply current	IDD (sensor selected) IDD (sensor not selected)		3.2 2.6	5 4	mA mA
Reference voltage (2)	VR	0.6	0.7	1.1	V
Clock frequency (3)		0.5	2.0	2.5	MHz
Pixel rate		0.5	2.0	2.5	MHz
Integration time (line scan rate) (4) First die Subsequent die	Tint	 150 138			 µs µs / die
Clock pulse duty cycle (5)			75		%

Notes:

1. Applies to all clocks; GBST, SIC, SI, and CLK.
2. The dark level is set by the voltage on the VR input pad, which is internally set to a typical value of 0.7V. Alternatively, if the user wishes to use a dark level greater than this, then VR can be supplied externally.
3. Although the device will operate with a pixel rate of less than 500kHz, it is recommended that the device be operated above 500kHz to maintain performance characteristics. Operating below 500kHz may result in a significant integration of dark current.
4. Tint is the integration time of a single sensor and is the time between two start pulses. The minimum integration time is the time it takes to clock out 29 inactive pixels and 344 active pixels. If several sensors are cascaded together in a module then the minimum integration time is the time it takes to clock out 29 inactive pixels and 344 active pixels from the first sensor and 344 pixels from each of all subsequent sensors, at a given frequency.
5. The clock duty cycle is defined as the ratio of the positive duration of the clock to its period.

8.0 Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings.

Table 4: Absolute Maximum Ratings

Parameter	Max.	Units
Power supply voltage (Vdd)	10	V
Clock input voltage high leve l[1]	Vdd + 0.5	V
Clock input voltage low level [1]	-0.5	V
Operating temperature	-10 to +50	°C
Operating humidity	+10 to +85	RH%
Storage temperature	-25 to +75	°C
Storage humidity	+10 to +90	RH%

Notes:

1. Applies to all clocks; GBST, SIC, SI, and CLK.

9.0 Timing Requirements

The timing requirements and their symbols are listed in Table 5 and its accompanying timing diagrams are shown in Figure 4 and Figure 5.

Table 5: Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock (CLK) period	CLKp	400	500	2000	ns
Clock (CLK) pulse width	CLKpw		375		ns
Clock (CLK) duty cycle			75		%
Data setup time [1]	Tset	20			ns
Data hold time [1]	Thold	25			ns
Clock (CLK) rise time [2]	CLKrt	70			ns
Clock (CLK) fall time [2]	CLKft	70			ns
End of scan rise time [2]	SOrt			50	ns
End of scan fall time [2]	SOft			50	ns
Global start rise time [3]	GBSTrt	70			ns
Global start fall time [3]	GBSTft	70			ns
Pixel rise time [4,5]	Prt		115		ns
Pixel fall time [4,5]	Pft		75		ns

Notes:

1. The shift register will load on all falling CLK edges, so setup and hold times (Tset, Thold) are needed to prevent the loading of multiple start pulses. This would occur if the GBST remains high during two fallings edges of the CLK signal.
2. SI starts the register scanning and the first active pixel is read out on the 30th clock cycle of the CLK signal. However, when multiple sensors are sequentially scanned, as in CIS modules, the SO from the predecessor sensor becomes the SI to the subsequent sensor, hence the SI clock = the SO clock.
3. As discussed under the third unique feature, the GBST starts the initialization process and preprocesses all sensors simultaneously in the first 29 clock cycles (29 pixels) before the first pixel is scanned onto the video line from the first sensor.
4. The transition between pixels does not always reach the dark offset level as shown in Figure 4 (Vout). Figure 4 shows the transition doing so for illustration purposes; however a stable pixel sampling point does exist for every pixel.
5. The pixel rise time is defined as the time from when the CLK's rising edge has reached 50 percent of its maximum amplitude to the point when a pixel has reached 90 percent of its maximum amplitude. The pixel fall time is defined as the time from when a pixel's charge begins to decrease from its maximum amplitude to within 10 percent of the lowest point before the next pixel begins to rise.

Figure 4 shows the initialization of the first sensor in relation to its subsequent cascaded sensors. The SIC selects the first sensor to operate with 29 clock cycles of delay by connecting it to Vdd on the first sensor and to ground for all subsequent sensors. Hence the first sensor will operate with 29 inactive pixels being clocked out before its first active pixel is clocked out. The rise and fall times are listed in Table 5. The SO comes out in line with the second last active pixel, and the last active pixel of each sensor is the 344th pixel which coincides with the 344th clock cycle.

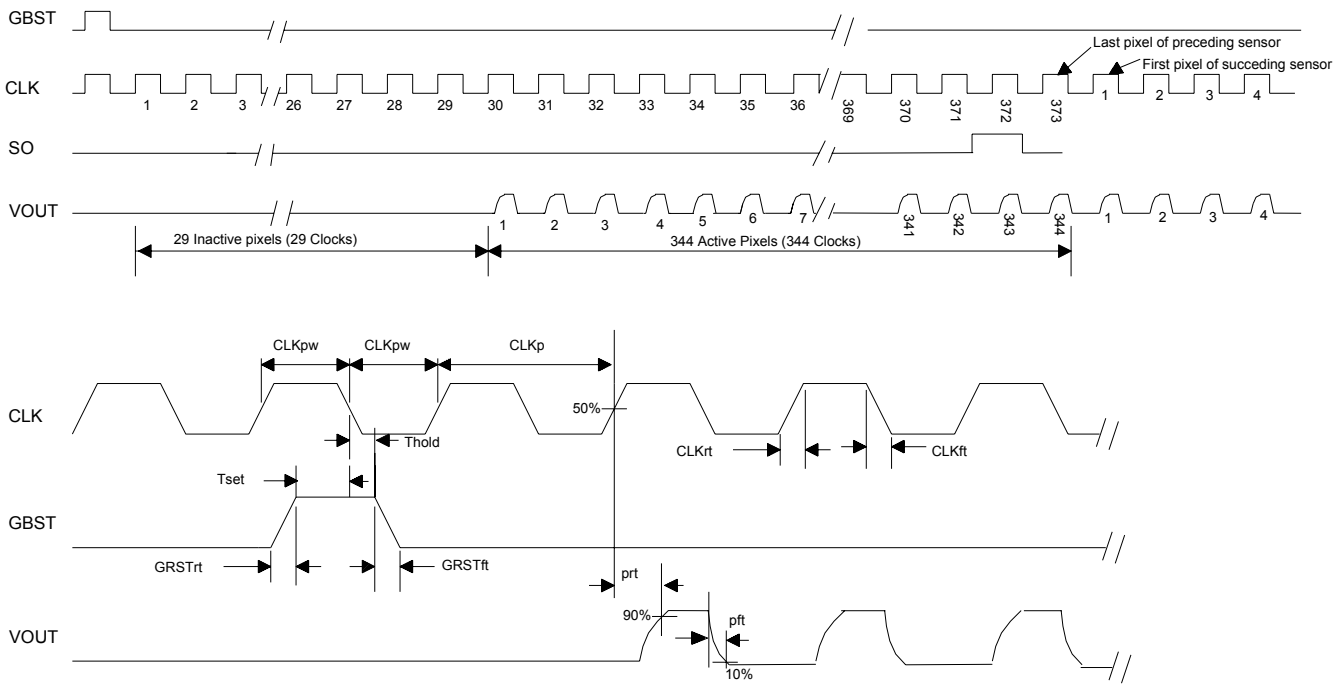


Figure 4: Overall Timing Diagram

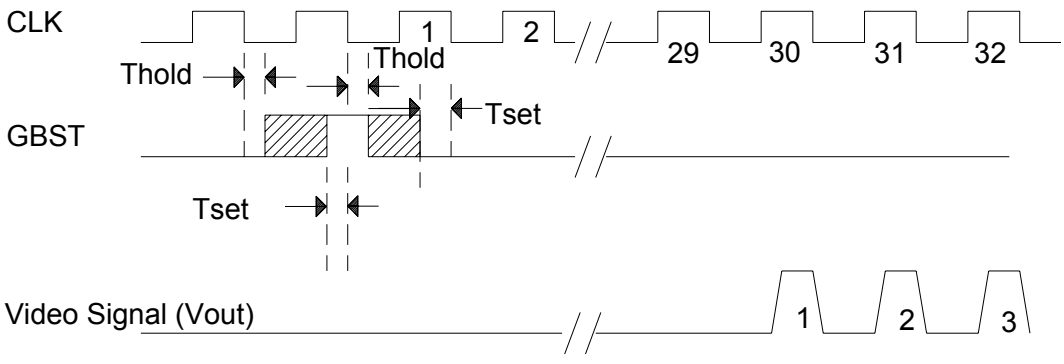


Figure 5: Timing of GBST-to-first Pixel of the First Sensor

10.0 AMIS-720649 Image Sensors in a CIS Module

Figure 6 shows a partial schematic detailing how numerous image sensors are serially concatenated in a CIS module. Since only the first sensor in the series of sensors is connected differently from the remaining sensors, only the first three sensors are shown. Note OS and OR are used as internal monitors and are not connected to the external module connector.

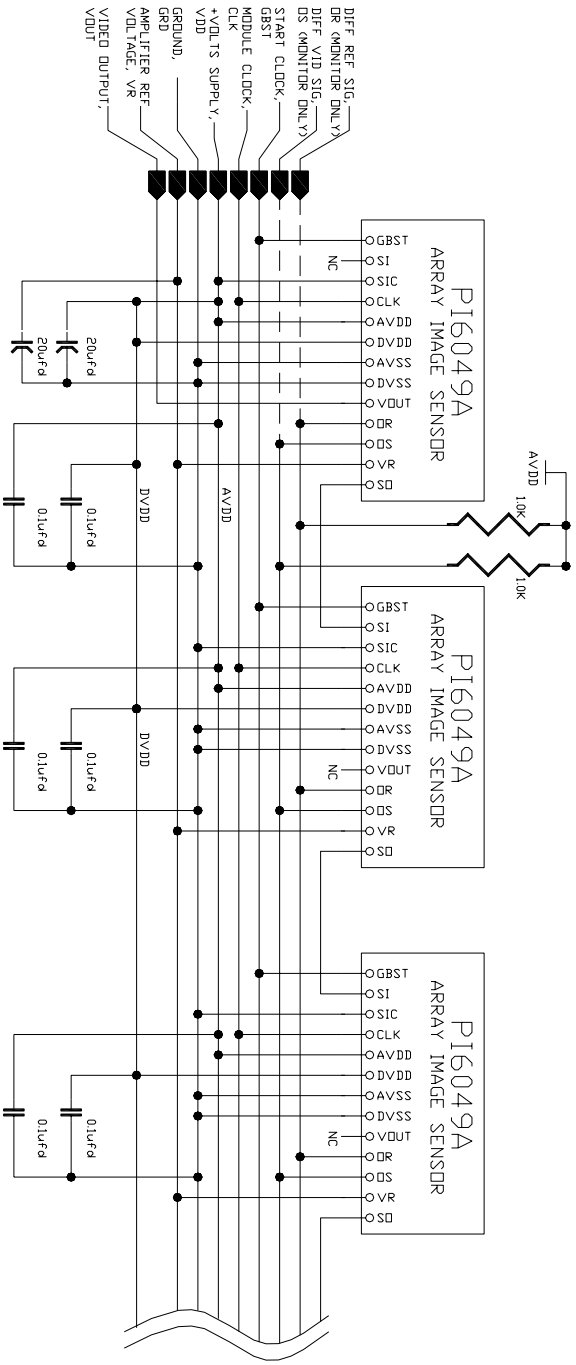


Figure 6: CIS Module with AMIS-720649 Image Sensors

11.0 Company or Product Inquiries

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