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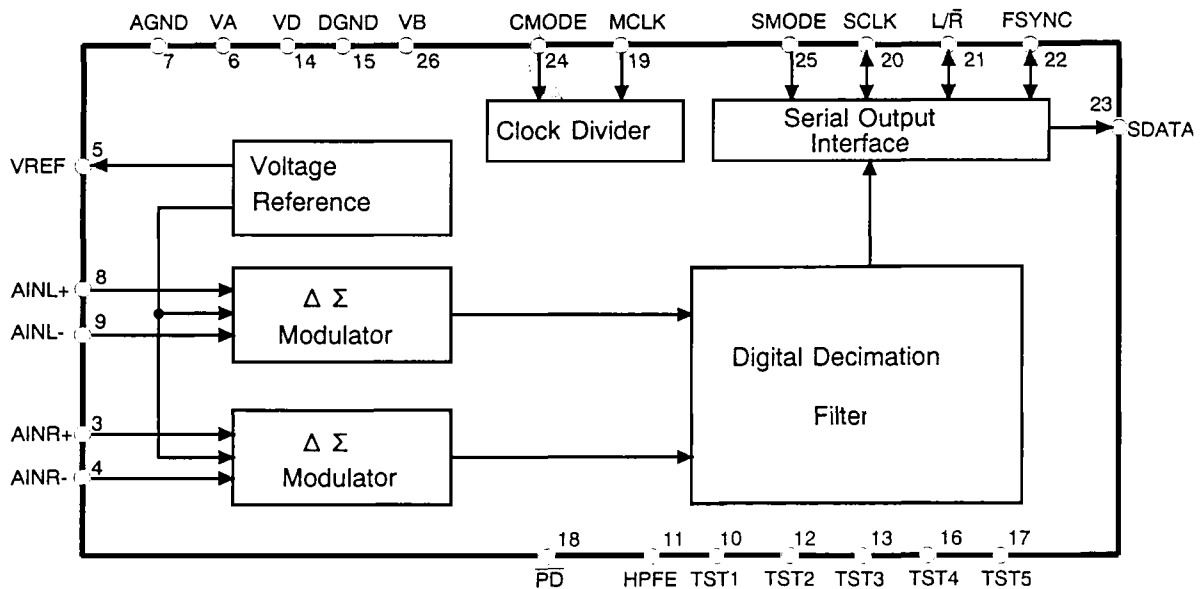
AKM

AK5350

Enhanced Dual bit Δ Σ 20bit A/D Converter

GENERAL DESCRIPTION

The AK5350 is a 20- bit, 64x oversampling rate(64fs) 2- channel A/D converter for stereo digital systems. The Δ Σ modulator in the AK5350 uses the new developed Enhanced Dual bit architecture. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as the conventional Single bit way. The AK5350 performs 100dB dynamic range, so the device is suitable for digital surround and Hi- Fi audio application such as Car- audio, MD, etc. The AK5350 is available in a small 28pin VSOP package which will reduce your system space.
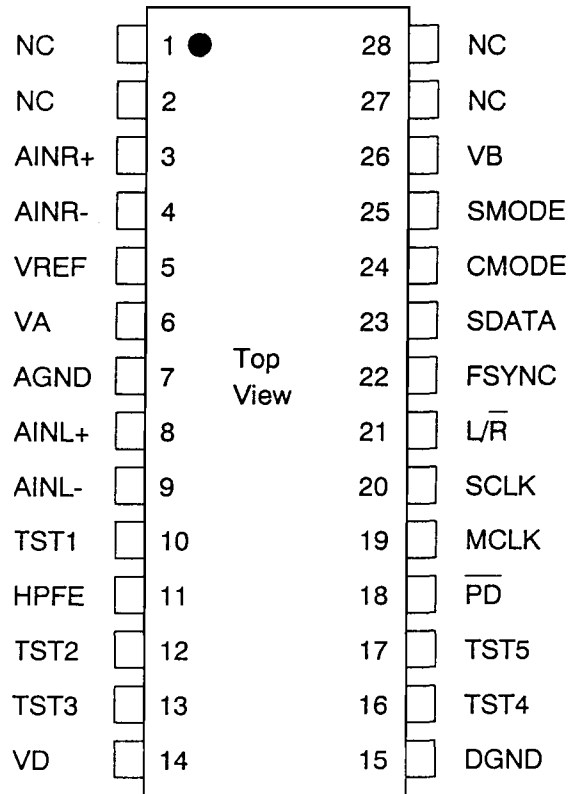
FEATURES

- ☐ Sampling rate: max. 54kHz
- ☐ Full- differential inputs
- ☐ S/(N+D): 94dB
- ☐ DR,S/N: 100dB
- ☐ Linear phase digital filter
    - Pass band: 0 ~ 22kHz (@fs = 48kHz)
    - Pass band ripple: ± 0.005dB
    - Stop band attenuation: 80dB
- ☐ Digital HPF for DC- offset cancel
- ☐ Master clock: 256fs/384fs
- ☐ Power supply: 5V ± 10%
- ☐ Low power consumption: 115mW
- ☐ Small package: 28pin VSOP

■ Ordering Guide

AK5350-VF   -40 ~ 85 ℃   28-pin VSOP
AKD5350   Evaluation Board

■ Pin Layout

NC	1 ●	28	NC
NC	2	27	NC
AINR+	3	26	VB
AINR-	4	25	SMODE
VREF	5	24	CMODE
VA	6	23	SDATA
AGND	7 Top View	22	FSYNC
AINL+	8	21	L/R̄
AINL-	9	20	SCLK
TST1	10	19	MCLK
HPFE	11	18	P̄D̄
TST2	12	17	TST5
TST3	13	16	TST4
VD	14	15	DGND

PIN/FUNCTION			
Pin No.	Pin Name	I/O	Function
3	AINR+	I	Right channel analog positive input pin
4	AINR-	I	Right channel analog negative input pin
5	VREF	O	Voltage Reference output pin (VA - 2.6V) Normally connected to VA with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.
6	VA	—	Analog section Analog Power, +5V
7	AGND	—	Analog section Analog Ground
10 12 13 16 17	TST1 TST2 TST3 TST4 TST5		Test pin (Pull-down pin) Should be left floating.
8	AINL+	I	Left channel analog positive input pin
9	AINL-	I	Left channel analog negative input pin
11	HPFE	I	High Pass Filter Enable pin (Pull-up pin) "H": ON "L": OFF
14	VD	—	Digital Power, +5V
15	DGND	—	Digital Ground
18	$\overline{PD}$	I	Power Down pin "L" brings the device into power-down mode. Must be done once after power-on.
19	MCLK	I	Master Clock Input pin CMODE="H" : 384fs CMODE="L" : 256fs
20	SCLK	I/O	Serial Data Clock pin Data is clocked out at the falling edge of SCLK. Slave mode: 64fs clock is input usually. Master mode: SCLK outputs a 64fs clock. SCLK stays low during the power-down mode($\overline{PD}$="L").

21	L/$\overline{R}$	I/O	Input Channel Selection pin
			Slave mode :
			    An fs clock is fed to this L/$\overline{R}$ pin. On the rising edge, SDATA
			    pin starts outputting the MSB of the left channel data, on the
			    falling, the right.
			Master mode :
			    L/$\overline{R}$ outputs an fs clock. The MSB data bit appears on
			    SDATA pin one SCLK cycle later at every L/$\overline{R}$ transition.
			    L/$\overline{R}$ stays high during the power-down mode($\overline{PD}$="L").

22	FSYNC	I/O	Frame Synchronization Signal pin
			Slave mode :
			    When high, data bits are clocked out on SDATA.
			Master mode :
			    FSYNC outputs 2fs clock.
			    Stays low during the power-down mode($\overline{PD}$="L").

23	SDATA	O	Serial Data Output pin Data are output with MSB first, in 2's complement format. After 20 bits are output it turns to "L". It also remains "L" at a power-down mode($\overline{PD}$="L").
24	CMODE	I	Master Clock Selection pin "L": MCLK=256fs (12.288MHz @fs=48kHz) "H": MCLK=384fs (18.432MHz @fs=48kHz)
25	SMODE	I	Serial Interface Mode Select pin Defines the directions of L/R, SCLK and FSYNC pins. "L": Slave mode (All become inputs) "H": Master mode (All become outputs)
26	VB	—	Substrate Power Supply, +5V

Note: Any other pins except for those listed above are NC pins. NC pins are not bonded internally.

ABSOLUTE MAXIMUM RATINGS

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
DC Power Supply:Analog Power(VA pin)	VA	-0.3	6.0	V
Digital Power (VD pin)(Note 2)	VD	-0.3	6.0/VB+0.3	V
(VB pin)	VB	-0.3	6.0	V
Input Current (Any pin except supplies)	IIN	-	± 10	mA
Analog Input Voltage (Note 2) AINL+,AINL-,AINR+,AINR- pins	VINA	-0.3	6.0/VA+0.3	V
Digital Input Voltage (Note 2)	VIND	-0.3	6.0/VB+0.3	V
Ambient Temperature	Ta	-40	85	℃
Storage Temperature	Tstg	-65	150	℃

Note 1: All voltages with respect to ground.
Note 2: Absolute maximum value is highest voltage in 6.0V, VA+0.3V and VB+0.3V.

WARNING: Operation beyond theses limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
DC Power Supplies: Analog Power	VA	4.5	5.0	5.5	V
Digital Power(VD pin)	VD	4.5	5.0	VB	V
(VB pin) (Note 3)	VB	4.5	5.0	5.5	V

Note 1: All voltages with respect to ground.
Note 3: The VA and VB are connected together through the chip substrate and has several ohms resistors. The VA and VB should be supplied from the same power unit. The VA and VB should be powered at the same time or earlier than VD.

※   AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25 ℃ ; VA,VD,VB=5.0V; fs=48kHz; Input signal frequency=1kHz; 20bit
Measurement Bandwidth=10Hz ～ 20kHz; unless otherwise specified.)

Parameter		min	typ	max	Units
Resolution				20	Bits
Analog Input Characteristics (Analog source impedance: 330 ohms)					
S/(N+D)	(Note 4)	88	94		dB
S/N	(A-Weight)	95	100		dB
Dynamic Range	(A-Weight)(Note 5)	95	100		dB
Interchannel Isolation(f=1kHz)		90	100		dB
Interchannel Gain Mismatch			0.1	0.3	dB
Gain drift		-	± 200	-	ppm/ ℃
Input Voltage Range		± 3.26	± 3.47	± 3.68	Vp-p
Input Impedance		-	180	-	k Ω
Power Supplies					
Power Supply Current (Note 6)					
Normal Operation (PD="H")					
VA+VB			15	22	mA
VD			8	11	mA
Power-Down mode (PD="L")					
VA+VB			20		uA
VD			10		uA
Power Consumption (Note 6)					
Normal Operation			115	165	mW
Power-Down mode			150		uW
Power Supply Rejection Ratio			50		dB

Note 4: The ratio of the rms value of the signal to the sum of all other spectral components up to
    20kHz except for the signal (included harmonic component, excluded DC component, analog
    input signal is -0.5dB). Inversed of THD+N.
Note 5: S/(N+D) with an input signal of 60dB below full-scale.
Note 6: Almost no current is supplied from VB pin.

DIGITAL FILTER CHARACTERISTICS

(Ta=25 ℃ ; VA,VD,VB=5.0V ± 10%; fs=48kHz; HPF=off)

Parameter	Symbol	min	typ	max	Units
Passband (-0.005dB)(Note 7)	PB	0		21.5	kHz
(-0.02dB)				21.768	
(-0.06dB)				22.0	
Stopband (Note 8)	SB	26.5			kHz
Passband Ripple (Note 9)	PR			± 0.005	dB
Stopband Attenuation (Note 8,Note 10)	SR	80			dB
Group Delay Distortion	△ GD			0	us
Group Delay (Note 11)	GD		610		us

Note 7: These frequencies scale with the sampling frequency(fs).

Note 8: Stopband is 26.5kHz to 3.0455MHz at fs=48kHz.

Note 9: Passband is DC to 21.5kHz at fs=48kHz.

Note 10: The analog modulator samples the input at 3.072MHz for a system sampling rate of fs=48kHz. There is no rejection of input signals at those bandwidths which are multiples of the sampling frequency(n x 3.072MHz ± 22kHz ;n=0,1,2,3·····).

Note 11: The calculating delay time occurred by digital filtering. This is the time from the input of analog signal to setting the 20bit data of both channels to the output registers. GD=29.3/fs.

ELECTRICAL CHARACTERISTICS

■ DIGITAL CHARACTERISTICS

(Ta=25 ℃ ; VA,VD,VB=5.0V ± 10%)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	V_{IH}	70%VD	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30%VD	V
High-Level Output Voltage Iout=-20uA	V_{OH}	VD-0.1	-	-	V
Low-Level Output Voltage Iout = 20uA	V_{OL}	-		0.1	V
Input Leakage Current (Note 12)	Iin	-		± 10	uA

Note 12: This is internally pulled down to ground or pulled up to DVDD. (TYP. 50K Ω)

■ SWITCHING CHARACTERISTICS

(Ta=25 ℃ ; VA,VD,VB=5.0V ± 10%; CL = 20pF)

Parameter	Symbol	min	typ	max	Unit
Control Clock Frequency					
Master Clock 256fs:	fCLK	4.096	12.288	13.824	MHz
Pulse width Low	tCLKL	30.0			ns
Pulse width High	tCLKH	30.0			ns
384fs:	fCLK	6.144	18.432	20.736	MHz
Pulse width Low	tCLKL	20.0			ns
Pulse width High	tCLKH	20.0			ns
Serial Data Output Clock	fSLK		3.072	3.456	MHz
Channel Select Clock(Sampling Frequency)	fs	16	48	54	kHz
Duty Cycle		25		75	%
Serial Interface Timing (Note 13)					
Slave Mode(SMODE="L")					
SCLK Period	tSLK	289.4			ns
SCLK Pulse width Low	tSLKL	100			ns
Pulse width High	tSLKH	100			ns
SCLK Falling to L/R Edge (Note 14)	tSLR	-70		70	ns
L/R Edge to SDATA MSB Valid	tDLR			70	ns
SCLK Falling to SDATA Valid	tDSS			70	ns
SCLK Falling to FSYNC Edge	tSF	-70		70	ns
Master Mode(SMODE="H")					
SCLK Frequency	fSLK		64fs		Hz
Duty Cycle			50		%
FSYNC Frequency	fFSYNC		2fs		Hz
Duty Cycle			50		%
SCLK Falling to L/R Edge	tSLR	-20		20	ns
L/R Edge to FSYNC Rising	tLRF		1		tslk
SCLK Falling to SDATA Valid	tDSS			70	ns
SCLK Falling to FSYNC Edge	tSF	-20		20	ns
Power down timing					
PD Pulse width	tPDW	150			ns
PD Rising to SDATA Valid (Note 15)	tPDV		516		1/fs

Note 13: Refer to Serial Data Interface.

Note 14: Specified L/R and FSYNC edges not to coincide with the rising edges of SCLK.

Note 15: The number of L/R rising edges after PD brought high. The value is in master mode.
In slave mode it becomes one L/R clock(1/fs) longer.

■ Timing Chart

SERIAL DATA TIMING (SLAVE MODE, FSYNC = "H")

SERIAL DATA TIMING (SLAVE MODE)

SERIAL DATA TIMING (MASTER MODE)

POWER DOWN TIMING
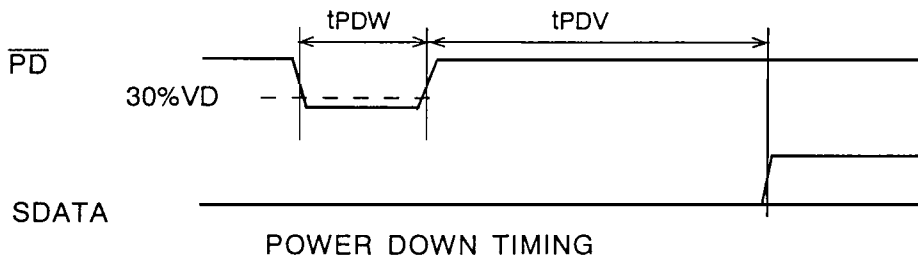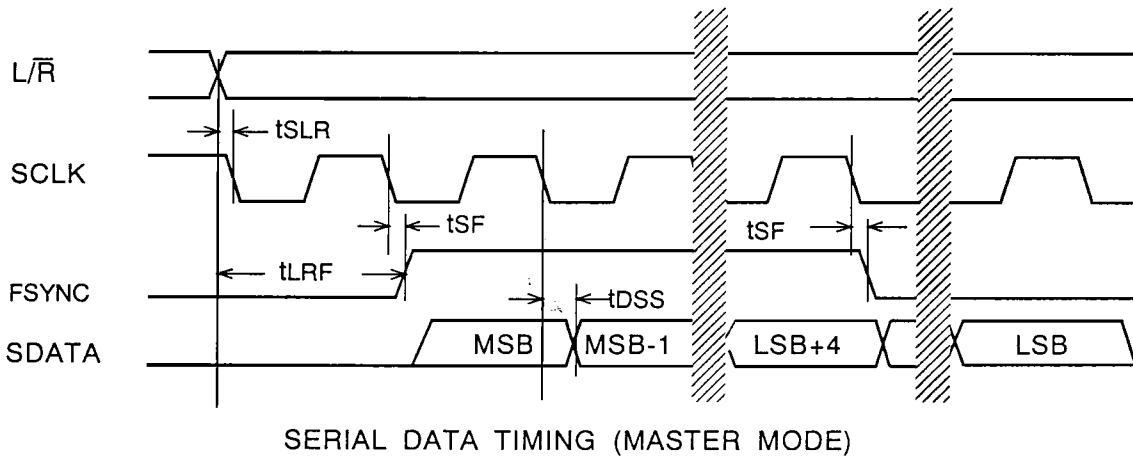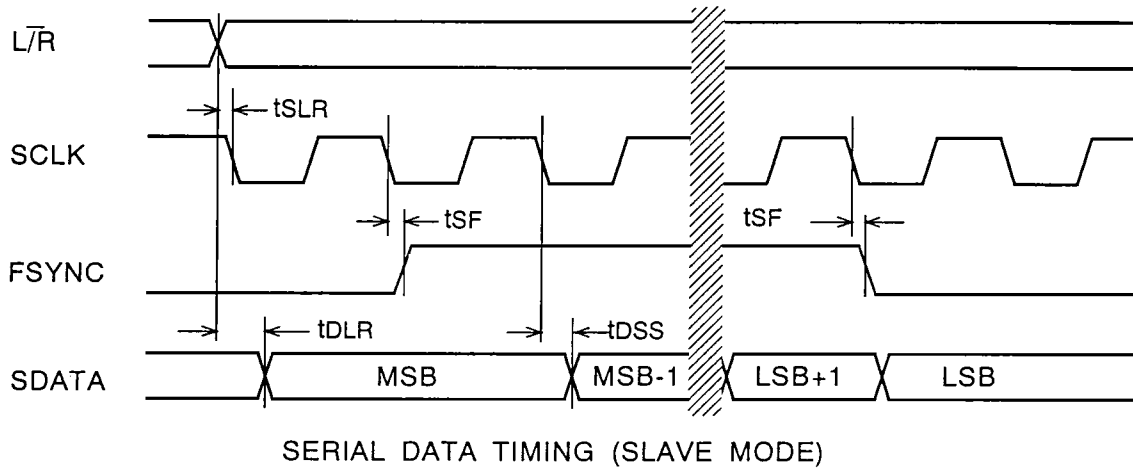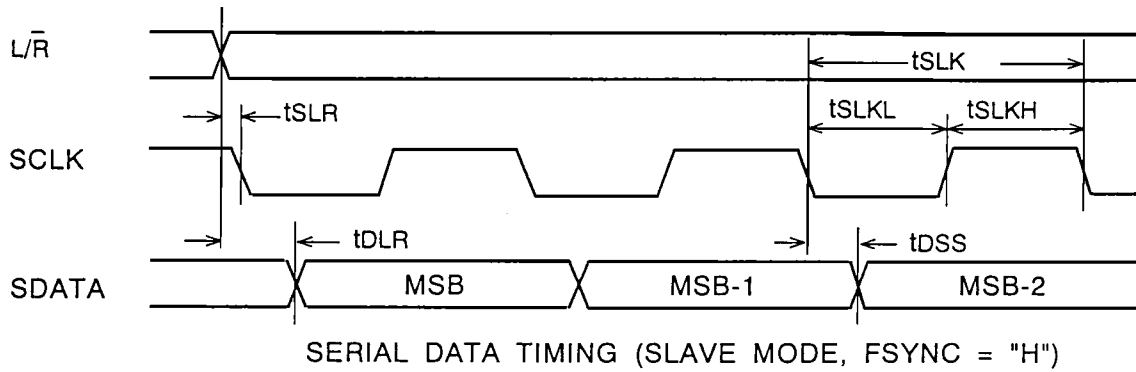
OPERATION OVERVIEW

■ System Clock

In slave mode, MCLK(256fs/384fs), L/R(fs) and SCLK(64fs) are required for AK5350. Use a signal divided from the MCLK for L/R. In master mode, only MCLK is needed. A L/R clock rate meets standard audio rates. (32kHz, 44.1kHz, 48kHz) In slave mode, the MCLK should be synchronized with L/R but the phase is free of care.

The AK5350 includes the phase detect circuit for L/R clock, the AK5350 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not needed except only for power-up.(Please refer to the "Asynchronization-reset"P.12.)

During the operation(PD="H") following external clocks should never be stopped : CLK in master mode and MCLK, SCLK and L/R in slave mode. When the clocks stop there is a possibility that the device comes into a malfunction because of over currents in the dynamic logic. If the external clocks are not present, the AK5350 should be in the power-down mode. (PD="L")

fs	Master Clock(MCLK)		SCLK(64fs)
	256fs	384fs	
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz

Table 1   System Clock

■ Serial Data Interface

SMODE	CMODE	MCLK	L/R, SCLK ,FSYNC	Fig.
L	L	256fs	Input	1
L	H	384fs	Input	1
H	L	256fs	Output	2
H	H	384fs	Output	2

Table 2   Serial Interface

■ Clock Circuit
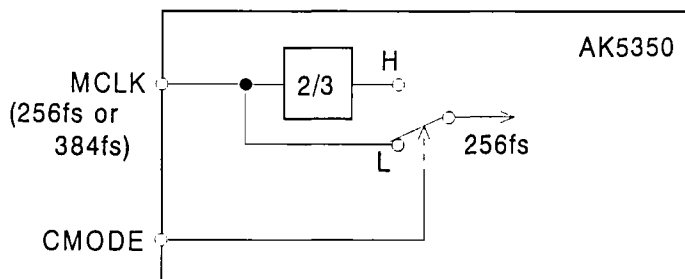
AK5350 has an internal divider as shown in the above figure. The device can interface either or an external MCLK (256fs or384fs) by controlling CMODE pin.

1) SLAVE mode

An output channel is defined by L/R. Both channel data are output in sequence, in order of the Lch first then Rch at the rate of fs. Data bits are clocked out via the SDATA pin at SCLK rate. Figure 1 shows data output timing. Normally SCLK is derived from MCLK by dividing it by four(64fs). FSYNC enables SCLK to start clocking out data. The MSB is clocked out by the L/R edge. SCLK causes the ADC to output succeeding bits when FSYNC is high.
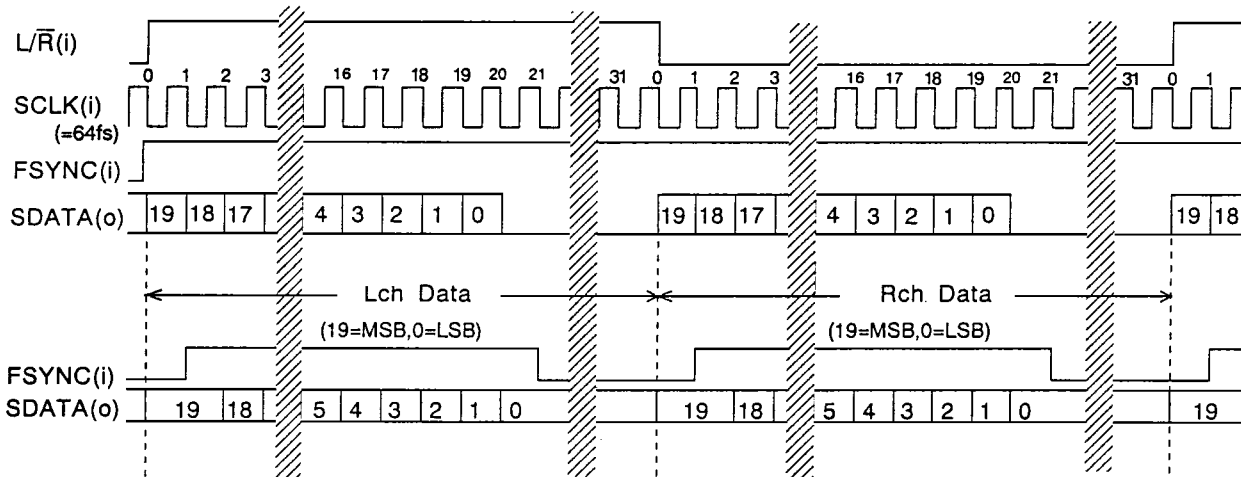
Figure 1. Data Output Timing-SLAVE mode

2) MASTER mode

In MASTER mode, the A/D converter is driven from a master clock(MCLK:256fs/384fs) and outputs all other clocks.(L/R, SCLK) The falling edge of SCLK causes the ADC to output each bit. Figure 2 shows the output timing. 2x fs clock of 50% duty is output via the FSYNC pin. FSYNC rises one SCLK cycle after the transition of L/R edges and stays high during 16 serial clocks($16 * t_{SLK}$). Upper 16 bit data is output during FSYNC "H", lower 4 bit is output after FSYNC "L" transition.
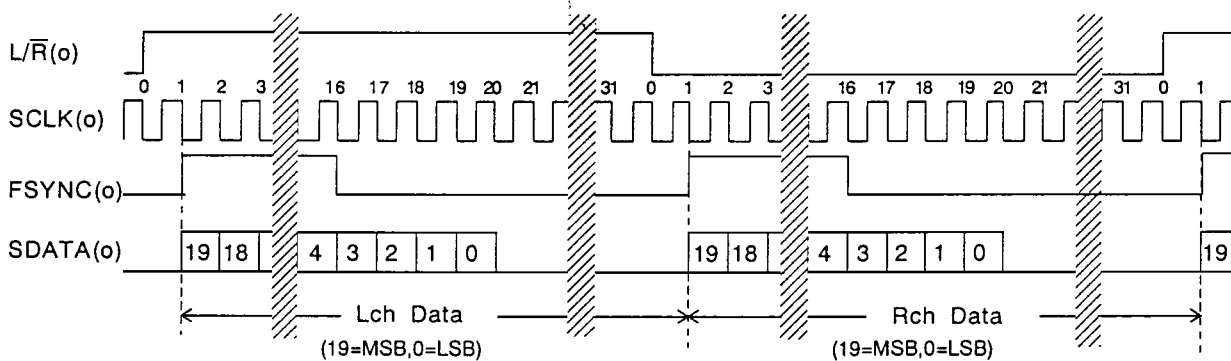
Figure 2. Data Output Timing-MASTER mode

■   Power-down mode

The AK5350 has to be reset once by bringing $\overline{PD}$ "L" upon power-up. All internal registers of the digital filter and so on in the AK5350 are reset by this operation. When exiting the power-down mode(PD="H"), the internal timing starts clocking by first MCLK " ↑ "(rising edge). In master mode internal counter starts at once, in slave mode internal counter starts after synchronizing with the first rising edge of L/R. The serial output data is available after 516 counting clock of L/R cycle.

■   Asynchronization-reset

In slave mode, if the phase difference between L/R and internal control signals is larger than +1/16 ～ -1/16 of word period(1/fs), the synchronization of internal control signals with L/R is done automatically at the first rising edge of L/R.

■   High Pass Filter(HPFE pin)

The AK5350 has a Digital High Pass Filter(HPF) for DC-offset cancel. When HPFE pin goes "H", HPF is enabled. The cut-off frequency of the HPF is 7.5Hz(@fs=48kHz), and the frequency response at 20Hz is -0.5dB. It also scales with the sampling frequency(fs). The HPF can be disabled by bringing HPFE pin "L". In this case, the AK5350 has the DC-offset of a few mV.

SYSTEM DESIGN

Figure 3 shows the system connection diagram and Figure 4 shows the input buffer circuit. An evaluation board[AKD5350] is available which demonstrates the optimum layout, power supply arrangements and measurement results.
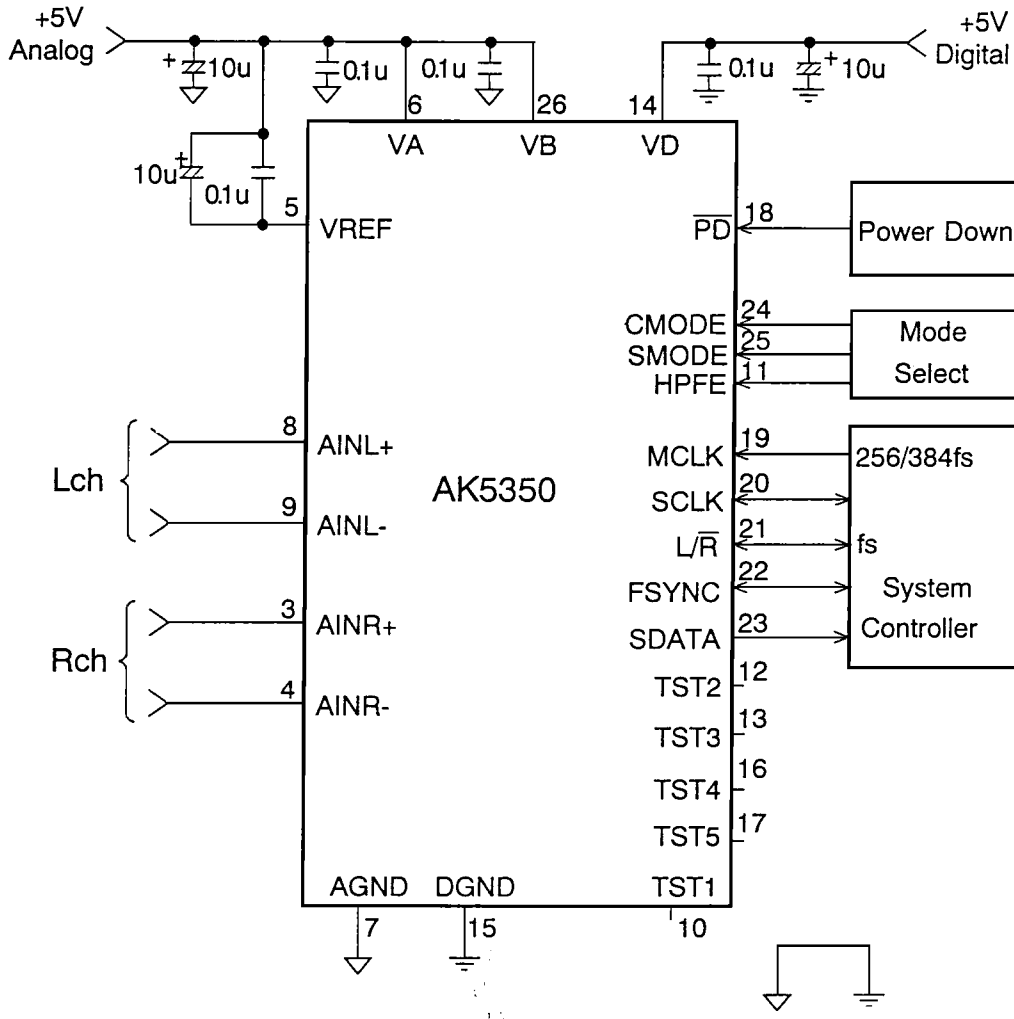
Figure 3.System Connection Diagram Example

NOTE: +5V Analog should be powered the same time or earlier than +5V Digital.
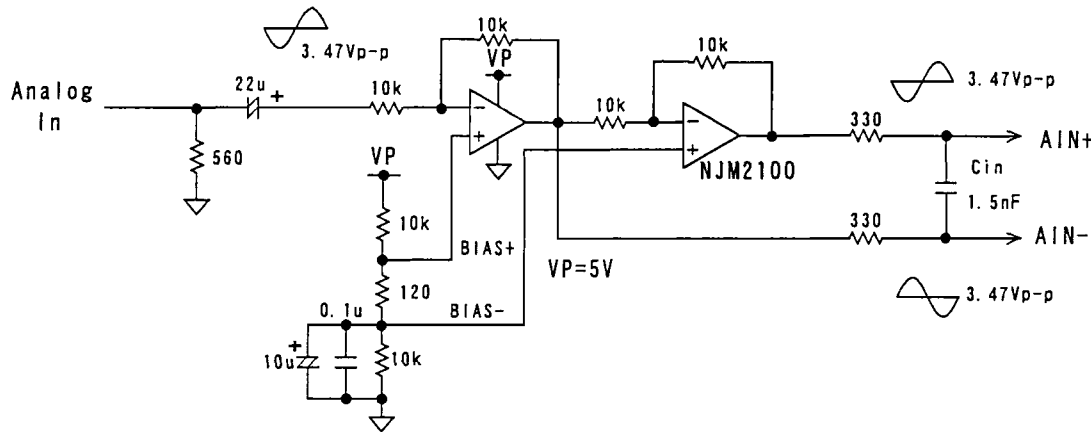
Figure 4. Input Buffer Circuit Example

The resistor of 120 ohms (between BIAS+ and BIAS-) in the input buffer circuit add a slight offset (typ. : -60mV) to A/D input, and it is included to improve the audible noise.

■   Grounding and Power Supply Decoupling

The AK5350 requires careful attention to power supply and grounding arrangements. The VA and VB are connected together through the chip substrate and have several ohm resistance. The power to VB should come up at the same time or faster than the power to VD, when they are fed separately to the device (Figure 3). As to the connections of decoupling capacitors, refer to Figure 3. The 0.1u of decoupling capacitors connected power supply pins should be as near as possible to the power supply pin.

■   Analog connections

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is ± 3.47Vp-p on its reference voltage(VREF). In case that the positive input is more than its full-scale, the AK5350 outputs positive 7FFFFH(Hex, Full-scale). In case that the negative input is more than its full-scale, the AK5350 outputs negative 80000H(Hex, Full- scale).

AK5350 samples the analog inputs at 3.072MHz with fs=48kHz. The digital filter rejects all noise between 26.5kHz and 3.0455MHz. However, the filter will not reject frequencies right around 3.072MHz (and multiples of 3.072MHz). Most audio signals do not have significant noise energy at 3.072MHz. Hence, a simple RC filter shown in figure 5 is sufficient to attenuate any noise energy at 3.072MHz.

The reference voltage for A/D converter is supplied from the VREF pin at VA reference. In order to eliminate the effects of high frequency noise on the VREF pin, a 10 μ F or less electrolytic capacitor and a 0.1 μ F ceramic capacitor should be connected parallel between the VREF and the VA pins. No current should be driven from the VREF pin.

The AK5350 accepts +5V supply voltage. Any voltage which exceeds the upper limit of (VA+)+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AINL ± ,AINR ±) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ± 15V in surrounding analog circuit.
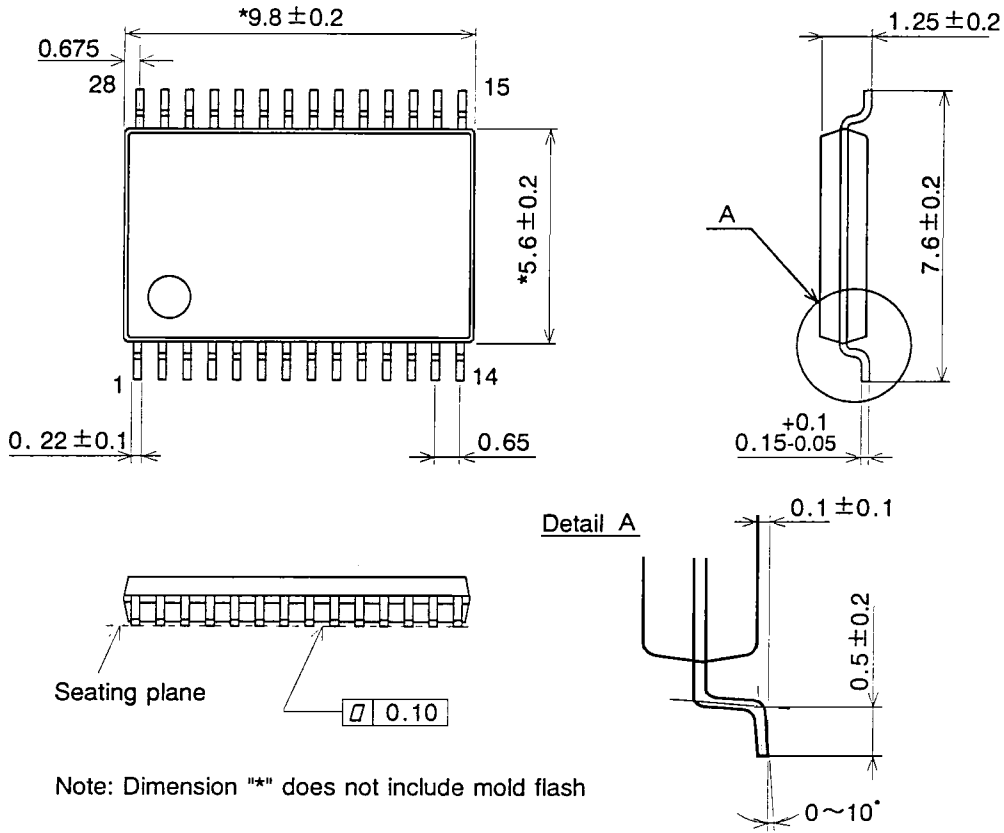
■   Digital Connections

To minimize digital originated noise, connect the ADC digital outputs only to CMOS inputs. Logic families of 4000B, 74HC, 74AC, 74ACT and 74HCT series are suitable.

■   Multiple AK5350

In systems where multiple ADC's are required, care must be taken to insure the internal clocks are synchronized between converters to make simultaneous sampling. In slave mode, synchronous sampling is achieved by supplying the same MCLK and L/R to all converters. In master mode, the same $\overline{PD}$ signal is supplied to each ADC. The $\overline{PD}$ state is released at the first rising edge of MCLK after bringing $\overline{PD}$ into low. Hence, if the falling edge of $\overline{PD}$ and rising edge of MCLK coincides together the sampling difference among the ADC's modulator would occur. The difference could be 1/256fs in the sampling clock(64fs) of the modulator, typically 81ns at fs=48kHz.

PACKAGE

● 28pin VSOP (Unit: mm)

*9.8 ±0.2

0.675

28   15

*5.6 ±0.2

1   14

0. 22 ±0.1   0.65

1.25 ±0.2

A

7.6 ±0.2

+0.1
0.15 -0.05

Detail A

0.1 ±0.1

0.5 ±0.2

0～10°

Seating plane

☐ | 0.10

Note: Dimension "*" does not include mold flash

■ Material & Lead finish

Package: Epoxy
Lead-frame: Copper
Lead-finish: Soldering plate

MARKING

AKM

AK5350-VF
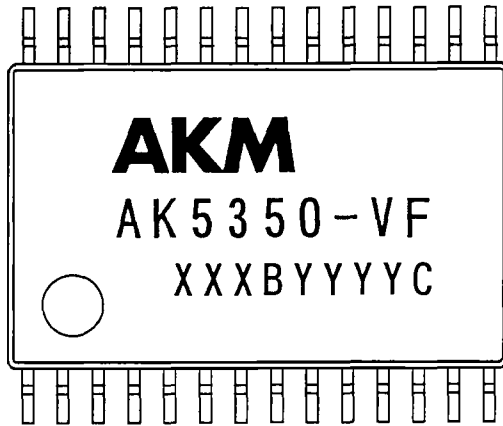
XXXBYYYYC

XXXBYYYYC   data code identifier

XXXB :   Lot number （X : Digit number, B : Alpha character）
YYYYC :   Assembly date （Y : Digit number, C : Alpha character)

IMPORTANT NOTICE