DDR Termination Regulator

FEATURES

- Source and Sink Current Capability
- Suspend To RAM Functionality
- Support DDR Ⅰ (1.25V_{TT}) and DDR Ⅱ (0.9V_{TT}) Requirements
- Low Output Voltage Offset, ±20mV
- High Accuracy Output Voltage at Full-Load
- Low External Component Count
- No external resistor required
- Current Limit protection
- Thermal Protection
- SOP-8 and SOP-8 Exposed Pad (Heat Sink) Package

APPLICATIONS

- Mother board
- Graphic cards
- DDR Ⅰ and DDR Ⅱ termination voltage

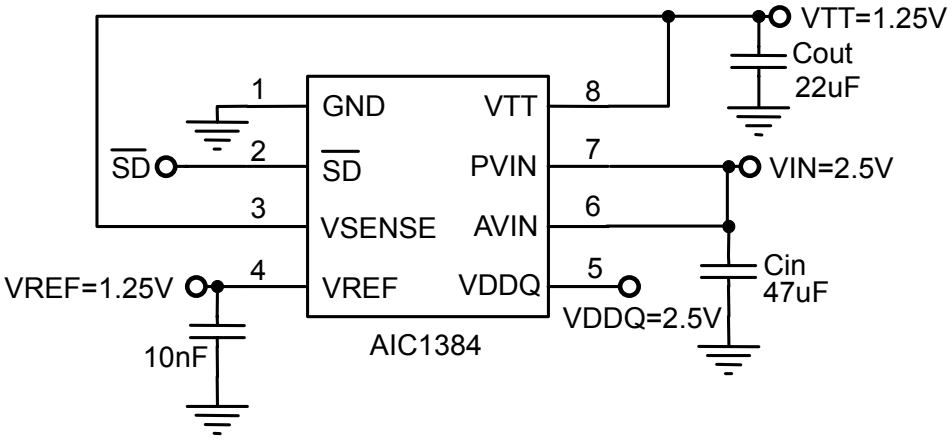
DESCRIPTION

The AIC1384 linear regulator is designed to deliver 1.5A continuous current and up to 3A peak transient currents for termination of DDR-SRAM. The AIC1384 contains a high-speed operational amplifier to supply superior load transient response. It also includes a V_{SENSE} to provide excellent load regulation and V_{REF} output as a reference for the chipset and DIMMs. The AIC1384 supply accurate V_{TT} and V_{REF} without external resistors that save PCB areas.

The AIC1384 also features an active low shutdown pin that provides Suspend To RAM (STR) functionality. The V_{TT} will remain high impedance when in shutdown, but V_{REF} will keep active. The advantage of power saving can be obtained through low 150μA (DDR Ⅰ) quiescent current.

Built in current limiting in source and sink mode, with thermal shutdown provide maximal protection to the AIC1384 against fault conditions.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

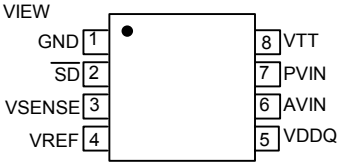
AIC1384XXXX

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  S: SOP-8
  SH: SOP-8 Exposed Pad (Heat Sink)
- P: Lead Free Commercial
  G: Green Package

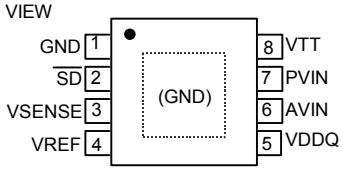
Example: AIC1384PSTR
→ In Lead Free SOP-8 Package & Taping & Reel Packing Type

PIN CONFIGURATION

SOP-8
TOP VIEW



SOP-8 Exposed Pad (Heat Sink)
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

PVIN, AVIN, VDDQ, $\overline{SD}$, V_{SENSE}, V_{REF}, V_{TT}, to GND 6.0V

Operating Temperature Range ..... -40°C ~ 85°C

Junction Temperature ..... 125°C

Storage Temperature Range ..... - 65°C ~ 150°C

Lead Temperature (Soldering. 10 sec) ..... 260°C

Thermal Resistance Junction to Ambient, $R\theta_{JA}$ (Assume no ambient airflow, no heatsink)

SOP-8 ..... 160°C /W

SOP-8 Exposed Pad (Heat Sink) ..... 60°C /W

Thermal Resistance Junction to Case, $R\theta_{JC}$ SOP-8 ..... 40°C /W

SOP-8 Exposed Pad (Heat Sink) ..... 16°C /W

Absolute Maximum Ratings are those values beyond which the life of a device may be Impaired.

TEST CIRCUIT

Refer to TYPICAL APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS

(AVIN=2.5V, PVIN=VDDQ=1.8V / 2.5V, T_A=25°C, unless otherwise specified) (Note 1)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage (DDR1/2)		AVIN	2.2		5.5	V
		PVIN	1.6	2.5/1.8		
Reference Voltage	VDDQ = 1.7V	V_{REF}	0.83	0.85	0.87	V
	VDDQ = 1.8V		0.88	0.90	0.92	
	VDDQ = 1.9V		0.93	0.95	0.97	
	VDDQ = 2.3V	V_{REF}	1.127	1.15	1.177	V
	VDDQ = 2.5V		1.227	1.25	1.277	
	VDDQ = 2.7V		1.327	1.35	1.377	
V_{TT} Output Voltage	I_{OUT} = 0A, +0.9A, -0.9A					
	VDDQ = 1.7V	V_{TT}	0.81	0.85	0.89	V
	VDDQ = 1.8V		0.86	0.90	0.94	
	VDDQ = 1.9V		0.91	0.95	0.99	
	I_{OUT} = 0A, +1.5A, -1.5A					
	VDDQ = 2.3V	V_{TT}	1.116	1.15	1.181	V
	VDDQ = 2.5V		1.216	1.25	1.281	
	VDDQ = 2.7V		1.316	1.35	1.381	
V_{TT} Output Voltage Offset (for DDR I)	I_{OUT} = 0A	V_{OS}	-20		20	mV
	I_{OUT} =+1.5A/ -1.5A		-25		25	
V_{TT} Output Voltage Offset (for DDR II)	I_{OUT} = 0A	V_{OS}	-40		40	mV
	I_{OUT} =+0.9A/ -0.9A		-40		40	
V_{REF} Output Impendence	VDDQ = 2.5V, I_{REF} = -30μA to +30μA	Z_{VREF}		2.5		kΩ
	VDDQ = 1.8V, I_{REF} = -20μA to +20μA			2.5		
Current Limit	PVIN = 2.5V	I_{IL}	3.0			A
	PVIN = 1.8V		1.6			
Quiescent Current	I_{OUT} = 0A	I_{Q-AVIN}		320	500	μA
	$\overline{SD}$ = 0V	$I_{SD-AVIN}$			150	
V_{SENSE} Input Current		I_{SENSE}		13		nA
V_{TT} Leakage Current in Shutdown	$\overline{SD}$ = 0V, V_{TT} = 1.25V	I_{LK-TT}			10	μA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Shutdown Leakage Current	$\overline{SD}$ = 0V	I_{LK-SD}		2	5	μA
Shutdown Threshold	Output ON	V_{IH}	1.9			V
	Output OFF	V_{IL}			0.8	
Thermal Shutdown Temperature		T_{SD}		165		°C
Thermal Shutdown Hysteresis				20		°C

Note1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: V_{OS} is the voltage measurement, which is defined as V_{TT} subtracted $V_{REF.}$

Note 3: Load regulation and Current Limit are measured at constant junction temperature, by using pulse test with a short ON time.

TYPICAL PERFORMANCE CHARACTERISTICS

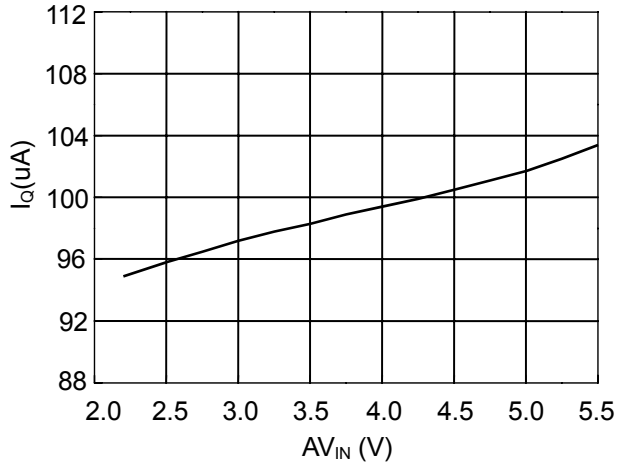


Fig. 1 I_Q vs. AV_{IN} in Shutdown

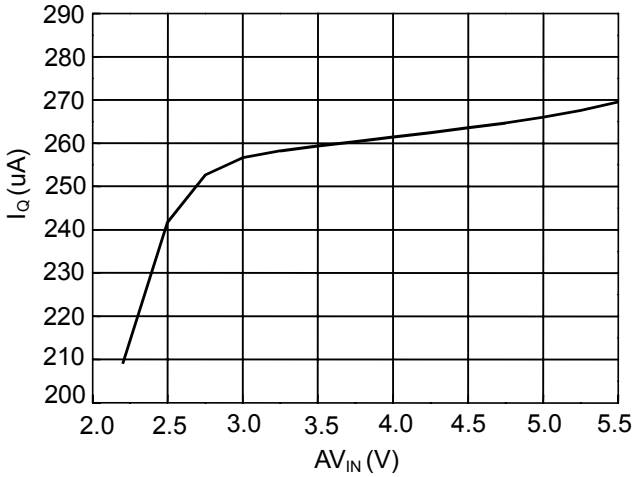


Fig.2 I_Q vs. AV_{IN}

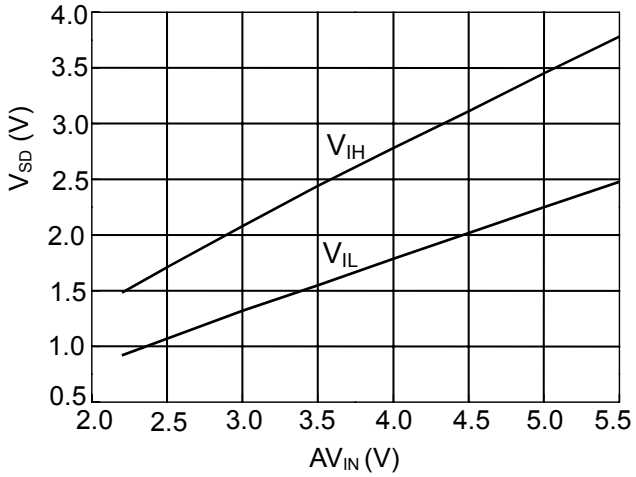


Fig.3 AV_{IN} vs. V_{SD}

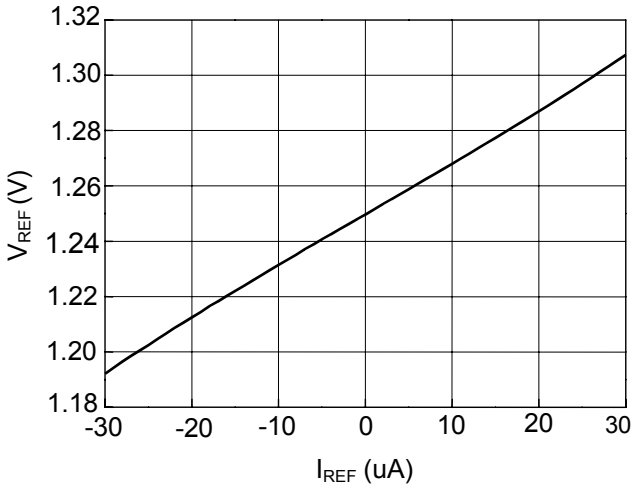


Fig.4 V_{REF} vs. I_{REF}

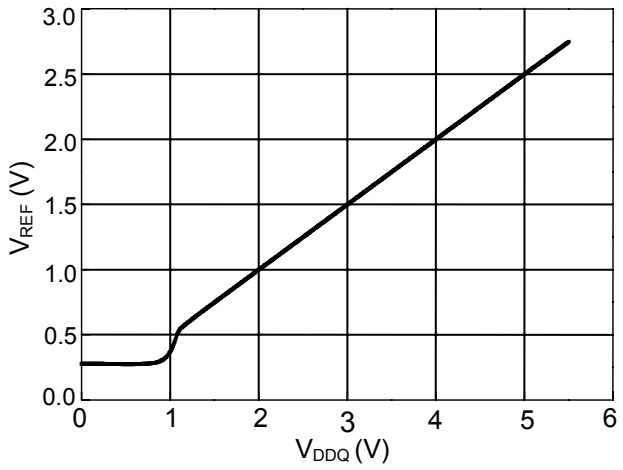


Fig.5 V_{REF} vs. V_{DDQ}

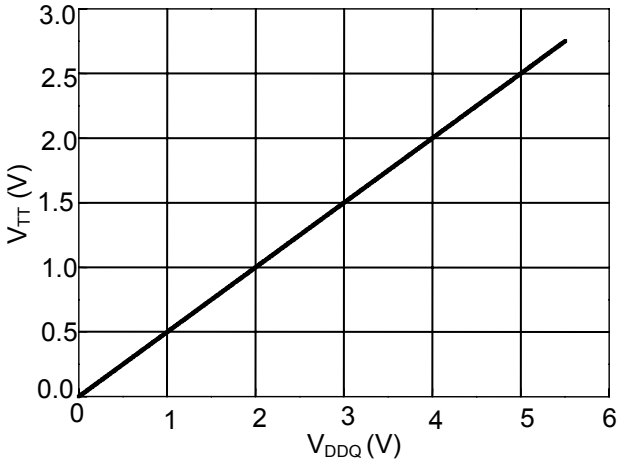


Fig.6 V_{TT} vs. V_{DDQ}

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

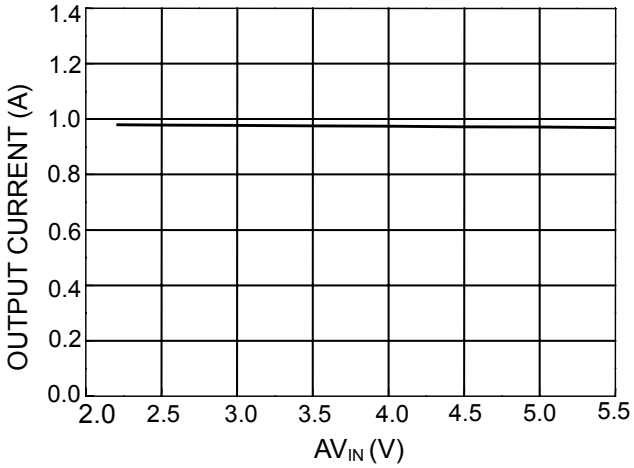


Fig.7 Maximum Sourcing Current vs. AV_{IN}
(V_{DDQ}=2.5V , PV_{IN}=1.8V)

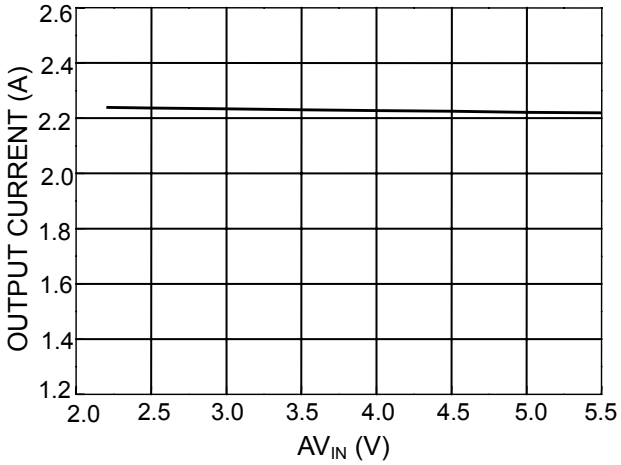


Fig.8 Maximum Sourcing Current vs AV_{IN}
(V_{DDQ}=2.5V , PV_{IN}=2.5V)

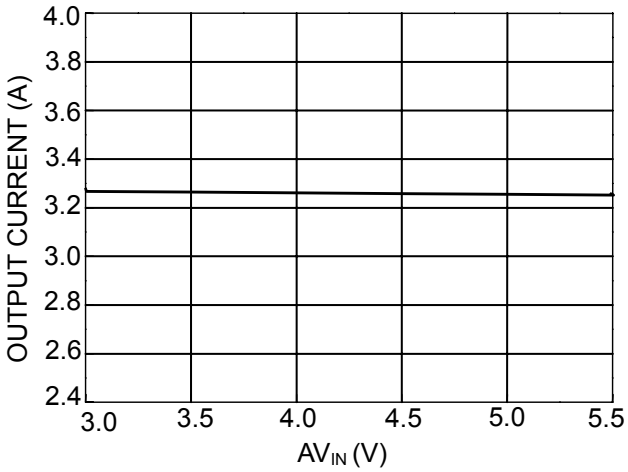


Fig.9 Maximum Sourcing Current vs AV_{IN}
(V_{DDQ}=2.5V , PV_{IN}=3.3V)

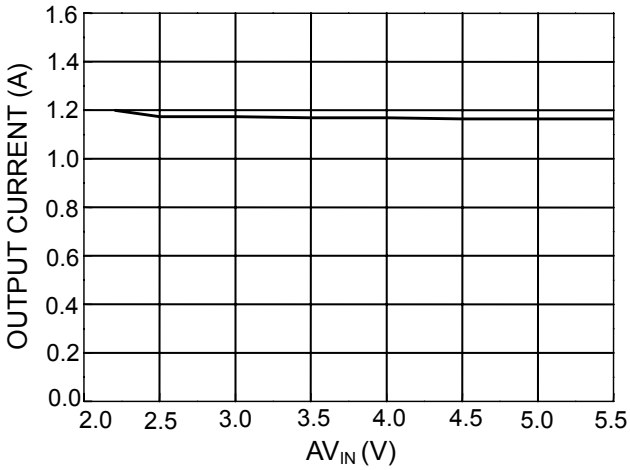


Fig.10 Maximum Sourcing Current vs. AV_{IN}
(V_{DDQ}=1.8V, PV_{IN} =1.8V)

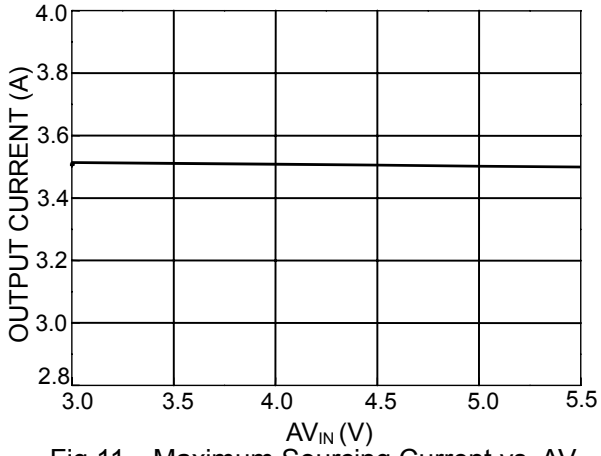


Fig.11 Maximum Sourcing Current vs. AV_{IN}
(V_{DDQ}=1.8V, PV_{IN} =3.3V)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

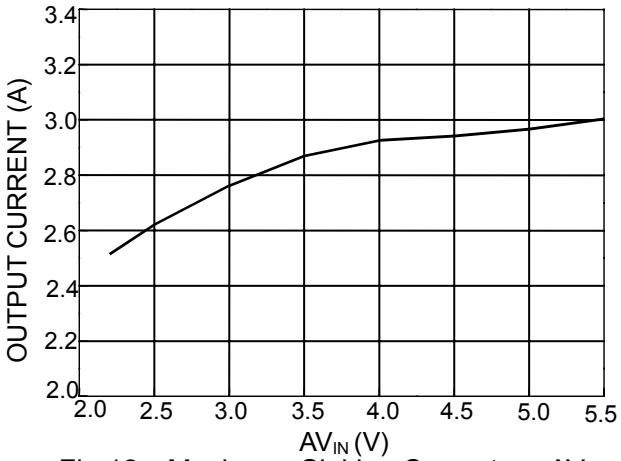


Fig.12 Maximum Sinking Current vs. AV_{IN} (V_{DDQ}=2.5V)

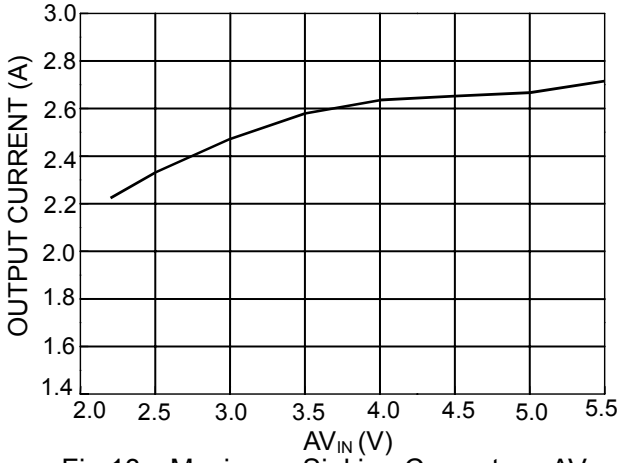


Fig.13 Maximum Sinking Current vs. AV_{IN} (V_{DDQ}=1.8V)

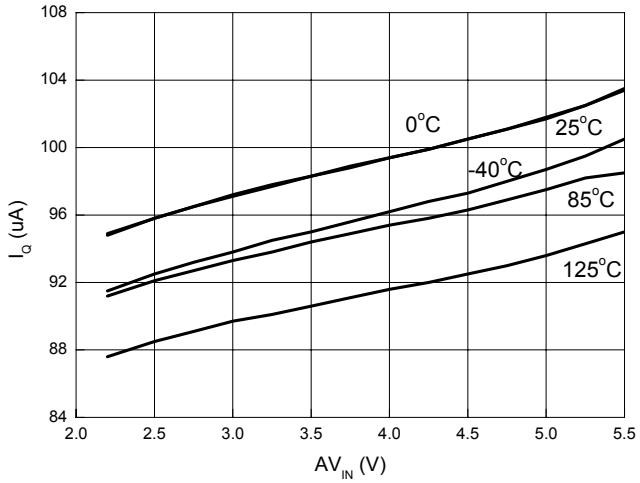


Fig14 I_Q vs. AV_{IN} in Shutdown

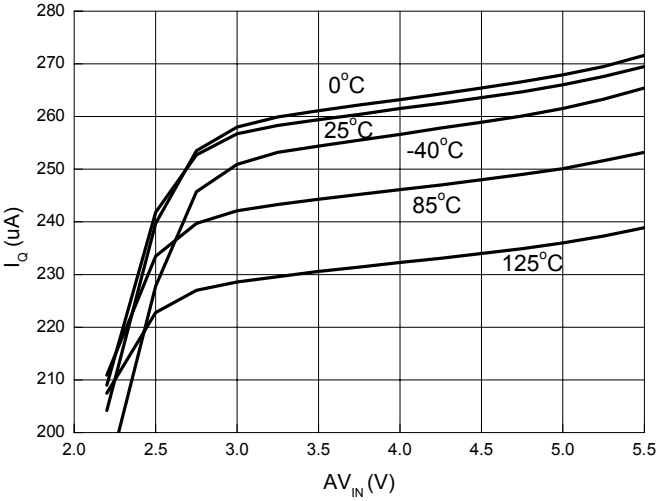


Fig15 I_Q vs. AV_{IN}

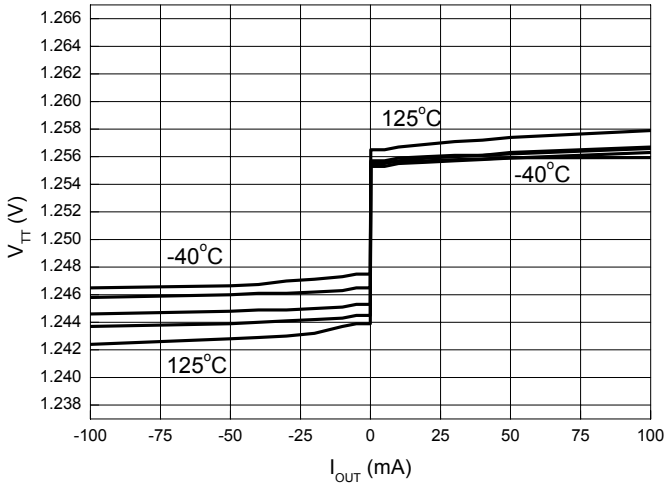


Fig16 V_{TT} vs. I_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

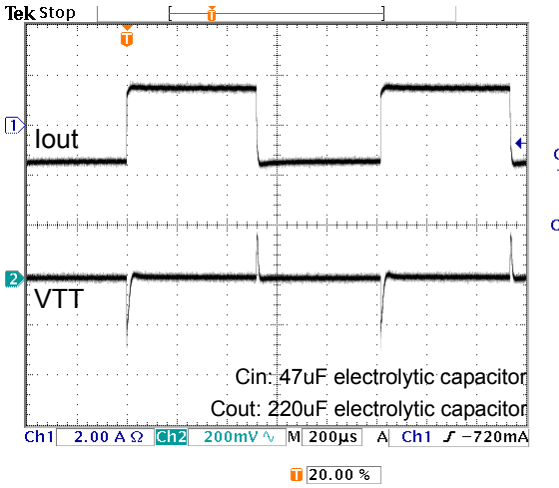


Fig.17 -1.5A to +1.5A load transient

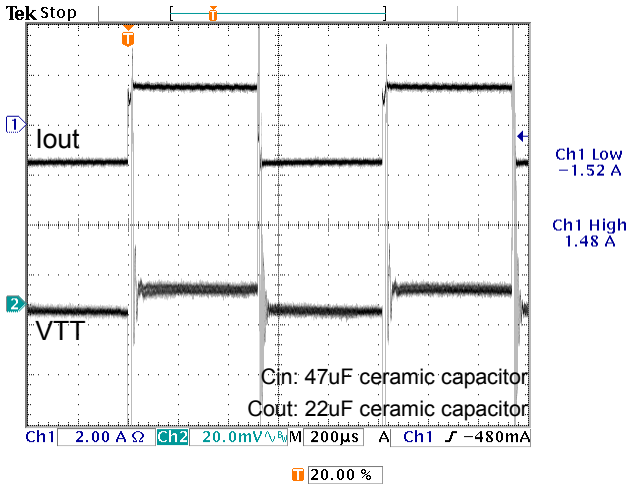


Fig.18 -1.5A to +1.5A load transient

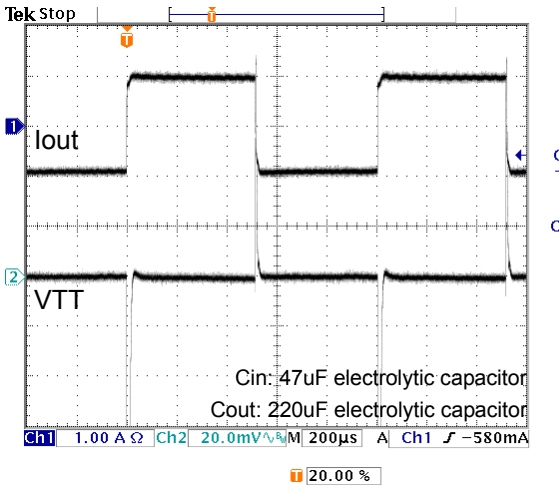


Fig.19 -0.9A to +0.9A load transient

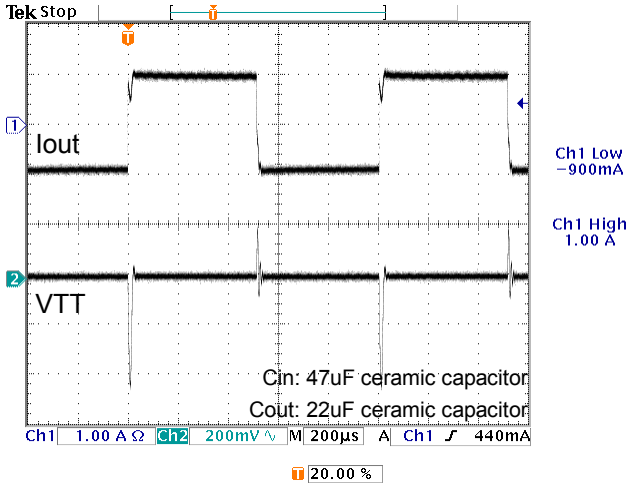
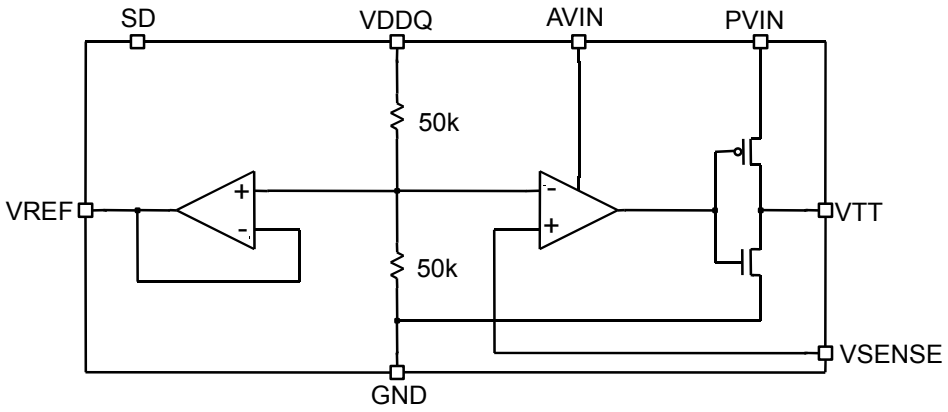


Fig.20 -0.9A to +0.9A load transient

BLOCK DIAGRAM



PIN DESCRIPTION

Pin 1: GND - Ground.

Pin 2: $\overline{SD}$ - Active low shutdown pin.

Pin 3: V_{SENSE} - Sense V_{TT} to improve load regulation.

Pin 4: V_{REF} - Buffered output of internal reference voltage, equal to VDDQ/2.

Pin 5: VDDQ - Input voltage to internal reference voltage for regulating V_{TT}.

Pin 6: AVIN - Analog input voltage to supply internal control circuitry.

Pin 7: PVIN - Power input voltage to supply the rail voltage exclusively for the output stage used to create V_{TT}.

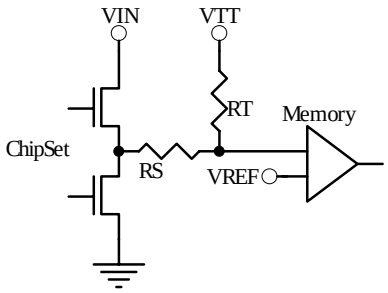
Pin 8: V_{TT} - Regulated output, equal to VDDQ/2.

Heat Sink - Recommended to Connect to GND.

APPLICATION INFORMATION

The AIC1384 linear termination regulator is designed to meet JEDEC requirements of DDR-SDRAM (DDR Ⅰ/Ⅱ). The V_{TT} is able to deliver sinking and sourcing current while regulating the voltage equal to VDDQ/2. The output stage includes a sense function to maintain excellent load regulation to prevent shoot through. The power part has two distinct rails that split the internal analog circuitry from power output stage, which results in reducing internal power disspation.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is necessary to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The achievement of single parallel termination can be seen as below figure.



Between the chipset and memory are one RS series resistor and one RT termination resistor. Both RS and RT are 25 Ohms typically; they can be altered to scale the current requirements from the AIC1384.

AVIN and PVIN

AVIN and PVIN have the ability to work with separate supplies depending on the application. Higher PVIN will increase the maximum continuous output current resulting from output R_{DS-ON} limitations at voltages close to V_{TT}. Oppositely, the internal power dissipation will also increase at high PVIN. Connect AVIN and PVIN together with 2.5V is a good compromise in SSTL-2 applications. This reduces the need for bypassing two supply pins separately. For the safe operation of the system; AVIN must always exceed or equal to PVIN.

VDDQ

VDDQ is used to make internal reference voltage for regulating V_{TT}. And V_{TT} will track VDDQ/2 precisely because of internal resistor divider. For SSTL-2 application, connect VDDQ to the 2.5V rail directly at the DIMM instead of AVIN and PVIN to achieve that reference voltage tracks the DDR memory rails accurately without a voltage drop from power lines.

V_{SENSE}

The sense pin is used to improve remote load regulation. The termination resistors in most motherboards connect to V_{TT} with a long trace that will cause a significant voltage drop. The V_{SENSE} pin can improve that a lower termination voltage at one end of the bus than the other by connecting it to the middle of the bus. If a long V_{SENSE} trace is implemented close to the memory, noise pickup can be a problem in precise regulation of V_{TT}. A small 0.1μF ceramic capacitor can be used for filtering noise. V_{SENSE} pin must still tie to V_{TT} if remote load regulation is not used.

V_{REF}

V_{REF} provides the buffered output of the internal VDDQ/2 reference voltage. It can be used to support the reference voltage for the Northbridge chipset and memory. The V_{REF} remains active during the shutdown state and thermal shutdown for the Suspend to RAM functionality. A bypass capacitor, located close to the V_{REF} pin, can be used to improve performance. Ranging from

0.01μF to 0.1μF of ceramic capacitor is recommended.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistor, which obtains the ability of sinking and sourcing current while regulating the output accurately to VDDQ/2. The AIC1384 is designed to deliver up to ±3A peak transient currents with excellent transient response. The output capacitor should be large enough to prevent an excessive voltage drop if a transient is expected to last above the maximum continuous current rating for a significant amount of time. AIC1384 is able to provide large transient output currents, yet it can't handle for long durations under all conditions that results from the standard packages are not able to dissipate the heat of the internal power loss. If large currents are required for longer durations, ensure that the maximum junction temperature is not exceeded.

Capacitor Selection

The input capacitor of AIC1384 is required for improved performance during large load transients to prevent the input rail from dropping. 47μF aluminum electrolytic capacitors or ceramic capacitor is recommended. If AVIN and PVIN are separated, the 47μF capacitor should be placed as close as possible to the PVIN. And AVIN can bypass a 0.1uF ceramic capacitor to prevent excessive noise.

220μF aluminum electrolytic capacitor is a recommendation for output capacitor to improve load transient response of V_{TT}. And size above 22uF ceramic output capacitor is allowed to general used for obtain small profile. The value of ESR is determined by the acceptable maximum current spike and the output voltage droops.

Thermal Dissipation

The AIC1384 has a thermal-limiting circuitry, which is designed to protect the device against overload condition. For continuous load condition, maximum rating of junction temperature must not be exceeded. It is important to pay more attention in thermal resistance. It includes junction to case, junction to ambient. The maximum power dissipation of AIC1384 depends on the thermal resistance of its case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The thermal resistance is greatly affected by the package used, the number of vias, the speed of airflow and the thickness of copper. When the IC mounting with good thermal conductivity is used, the junction temperature will be low even when large power dissipation applies. So the PCB mounting pad for GND pin of AIC1384 should provide maximum thermal conductivity to maintain low device temperature.

The power dissipation across the device is

$$P = I_{OUT} (V_{IN}-V_{OUT}).$$

The maximum power dissipation is:

$$P_{MAX} = \frac{(T_{J\text{-}max} - T_A)}{R\theta_{JA}}$$

Where $T_{J\text{-}max}$ is the maximum allowable junction temperature (125°C), and T_A is the ambient temperature suitable in application.

Layout Considerations

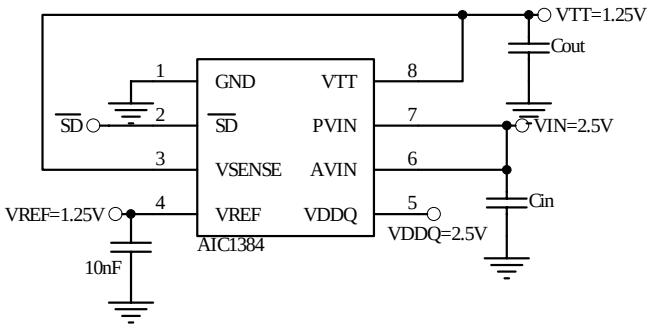
1. Minimize high current ground loops. Place the ground of the device, the input capacitor, and the output capacitor together with short and wide connection.
2. Connect the bottom-side pad (available in SOP-8 Exposed Pad) to a large ground plane. Use as much copper as possible to decrease the thermal resistance of the device.
3. A buried layer may be used as a heat spreader if the large copper around the

device is not available. Use vias to lead the heat into the buried layer.

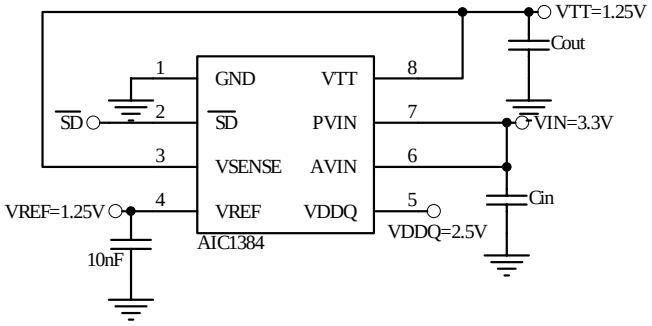
4. The input capacitor should be placed as close as possible to the PVIN pin.
5. A bypass capacitor, located close to the V_{REF} pin, can be used to improve performance. Ranging from 0.01μF to 0.1μF of ceramic capacitor is recommended.
6. If long sense traces is used, the noise of V_{SENSE} trace may occurs which from switching I/O signals. A 0.1uF ceramic capacitor connects to the V_{SENSE} pin can be used to filter high frequency signal.

APPLICATION EXAMPLES

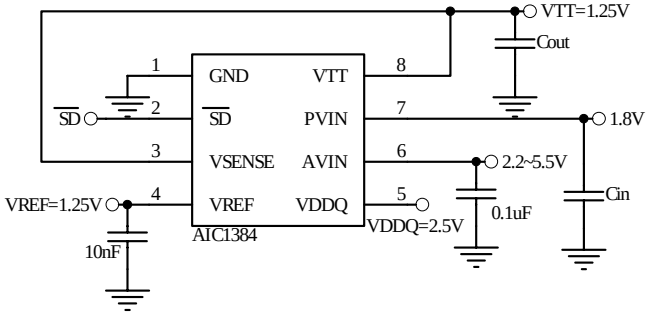
- **DDR Ⅰ Application**



All the input rails connect to 2.5V rail is recommend for the SSTL-2 termination scheme application. The circuitry completes an optimal power dissipation and component count.

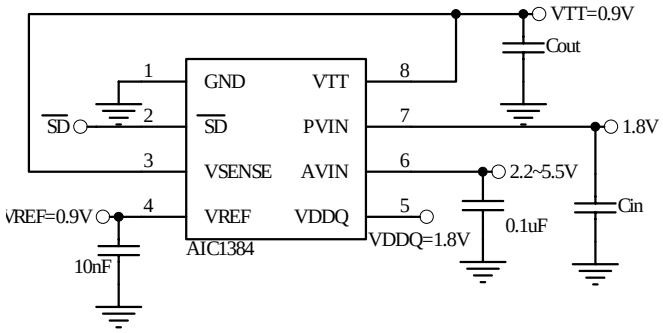


Connect the AIC1384 power rail to 3.3V to provide the maximum continuous output current if 1.8V and 2.5V rail are not available. Beware the junction temperature to exceed the maximum due to large current level. In this configuration AVIN will be limited to operation on the 3.3V or 5V rail results from PVIN can never exceed AVIN.

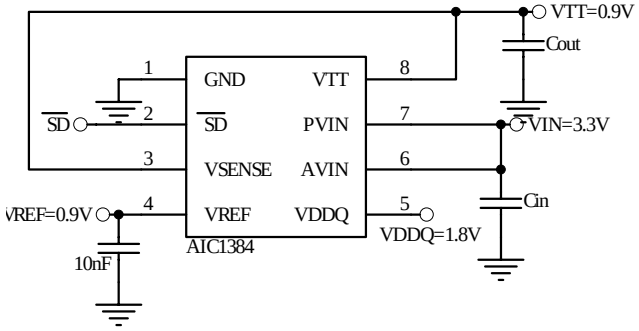


AVIN and PVIN have the ability to work with separate supplies. PVIN can be operated on a lower 1.8V rail and the AVIN can be connected to a higher rail. Although this circuitry can obtain better efficiency, but the maximum continuous current is reduced due to the lower rail voltage. Increasing the output capacitance can also help for large load transients.

- **DDRⅡ Application**

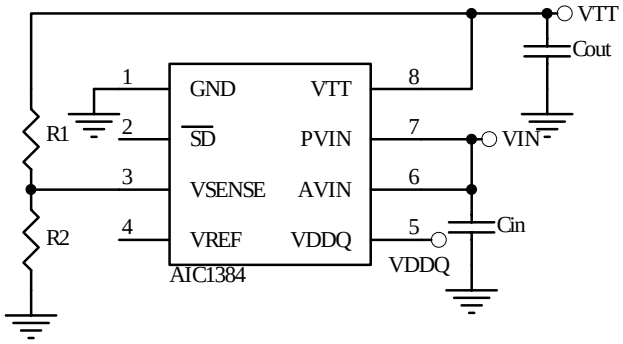


The circuit is recommended for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 3.3V or 5V rail.



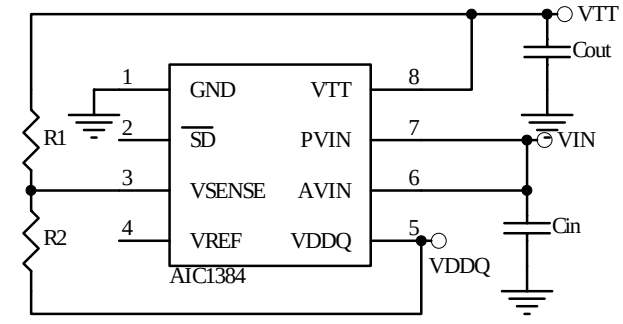
Connect the power rail to 3.3V to provide a higher continuous output current if 1.8V rail is not available. Careful with the junction temperature that may exceed the maximum due to the thermal dissipation increases with lower V_{TT} output voltages. In this configuration PVIN will be limited to operation on the 3.3V rail.

- **Level Shifting Application**



The AIC1384 is available to scale the output to any voltage required. One method is to level shift the output above the internal reference voltage of VDDQ/2 by using two resistors from the V_{TT} to the V_{SENSE}. The correct voltage at VTT is

$$V_{TT} = VDDQ/2\ (1 + R1/R2)$$

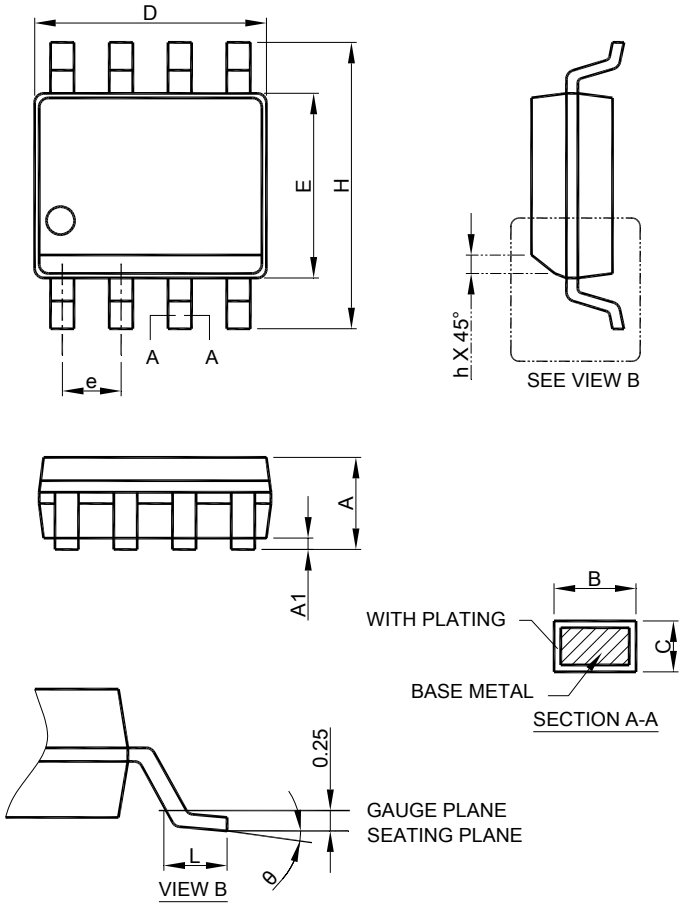


Another method is to level shift the output below the internal reference voltage of VDDQ/2 by using two resistors from the V_{SENSE} and VDDQ. The correct voltage at V_{TT} is

$$V_{TT} = VDDQ/2\ (1 - R1/R2)$$

PHYSICAL DIMENSIONS (unit: mm)

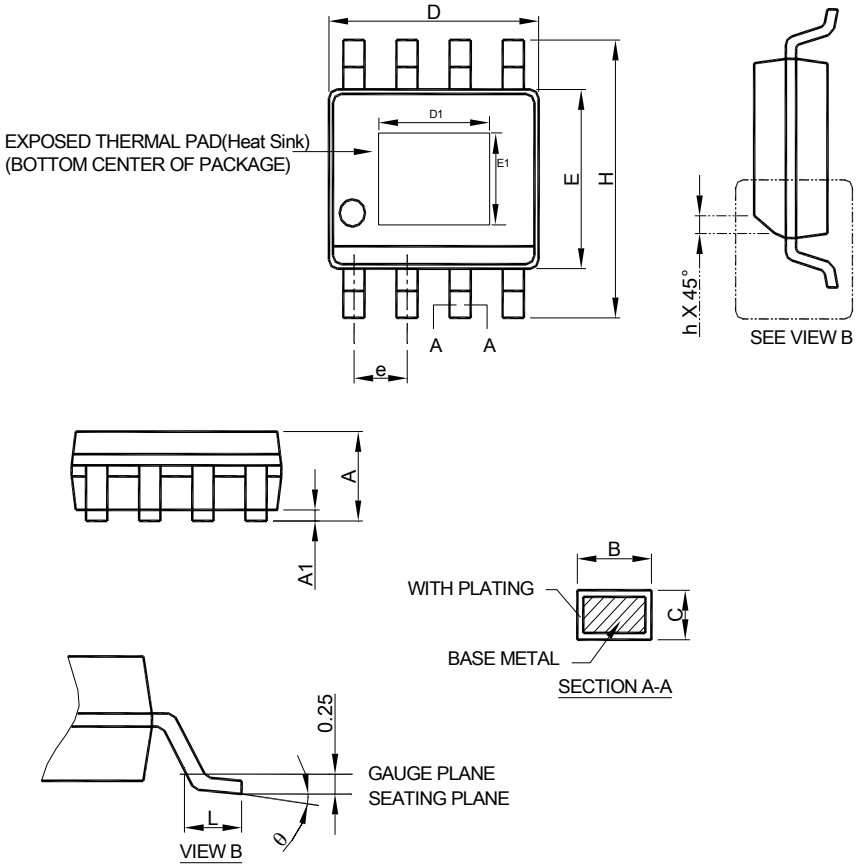
- **SOP- 8**



SYMBOL	SOP-8	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note: 1. Refer to JEDEC MS-012AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

- **SOP- 8 Exposed Pad (Heat Sink)**



SYMBOL	SOP-8 Exposed Pad(Heat Sink)	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
q	0°	8°
D1	1.5	3.5
E1	1.0	2.55

Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.