# Ultra LDO 1A Linear Regulator With Adjustable & Bypass Pin

## FEATURES

- Guaranteed 1A Output Current.
- Fast Response in Line/Load Transient
- Wide Operating Voltage Ranges: 2.3V to 6.0V.
- 0.1μA Shutdown Standby Current
- Low Quiescent Current: < 60μA.
- Fixed: 1.2V, 1.5V, 1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V, 3.5V, 3.7V, 3.8V Output Voltage.
- Adjustable Output Voltage are available from 0.8~4.5V
- Low Dropout：440mV at 1A and 2.8V output voltage.
- High PSRR：70dB at 1KHz.
- Active Low or High Shutdown Control. Current Limit and Thermal Protection.
- Available in ±2% Output Tolerance.
- Available in SOT-223 & TO-220 (3 pin) & SOP-8 Exposed Pad (Heat Sink) and TO-252 &TO-263 (3 & 5 pin) Package.

## APPLICATIONS

- LCD TV, LCD Monitor, DPF
- Networking
- STB
- DVD, HDD Driver
- Portable AV Equipment
- PC Peripherals

## DESCRIPTION

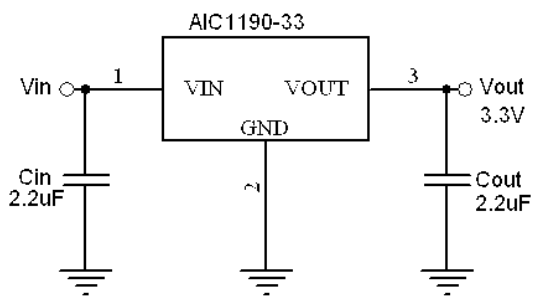
A low noise, high PSRR and ultra low dropout linear regulator AIC1190 is optimized for low ESR ceramic capacitors operation with 1A continuous current.

The AIC1190 offers high precision output voltage of ±2% tolerance. Output voltage can also be adjusted for those other than the preset values.

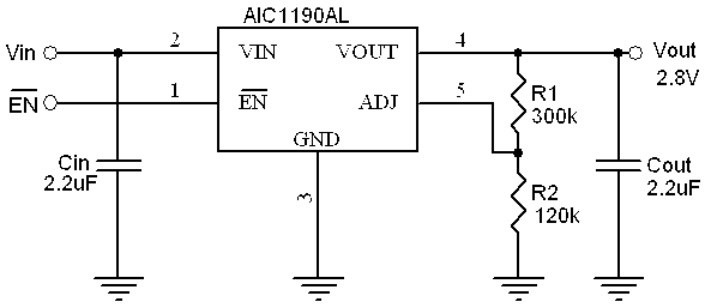
A noise bypass pin is available for further reduction of output noise. The bypass pin could be floating if it's unnecessary. At 1A load current and 2.8V output voltage, a 440mV dropout is performed. The quality of low quiescent current and low dropout voltage makes this device ideal for battery power applications. The high ripple rejection and low noise of the AIC1190 provide enhanced performances for critical applications such as cellular phones, and PDAs.

In addition, a logic-level shutdown input is included, which reduce supply current to less than 0.1μA (typ.) in shutdown mode with fast turn-on time less than 100μs. The AIC1190's current limit and thermal protection provide protection against any overload condition that would create excessive junction temperatures.

## TYPICAL APPLICATION CIRCUIT

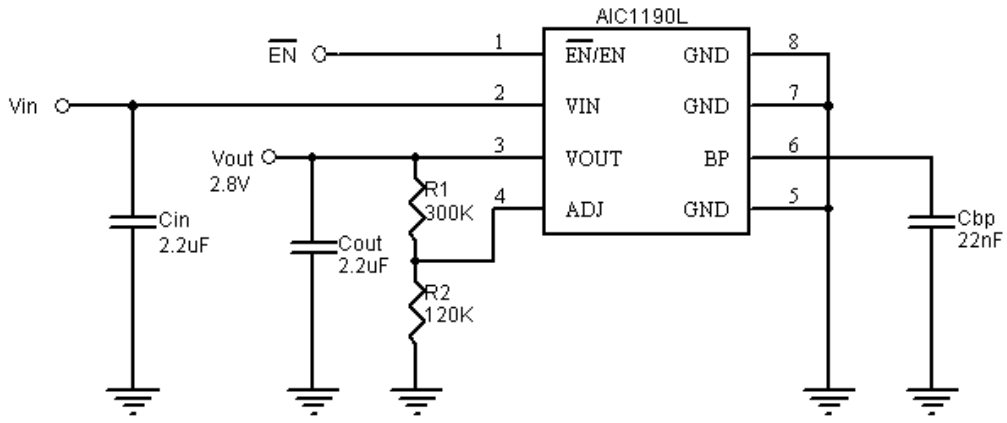



Fixed Linear Regulator




Adjustable Linear Regulator

## TYPICAL APPLICATION CIRCUIT (Continued)




Adjustable Linear Regulator in SOP-8 Exposed Pad Package

## ORDERING INFORMATION

AIC1190-XXXXX XX

PACKING TYPE
TR: TAPE & REEL
TB: TUBE

PACKAGE TYPE
Y3: SOT-223
E3: TO-252
M3: TO-263
T3: TO-220

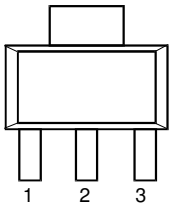
P: Lead Free Commercial
G: Green Package

OUTPUT VOLTAGE
12: 1.2V
15: 1.5V
18: 1.8V
20: 2.0V
25: 2.5V
27: 2.7V
30: 3.0V
33: 3.3V
35: 3.5V
37: 3.7V
38: 3.8V
(Of a unit of 0.1V within 0.8~4.5V, additional voltage versions are available on demand)

3 PIN CONFIGURATION

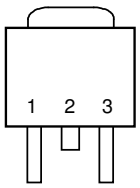
SOT-223 (Y3)
TOP VIEW

1: VIN
2: GND (TAB)
3: VOUT



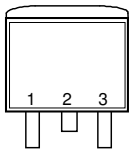

TO-252 (E3)
TOP VIEW

1: VIN
2: GND (TAB)
3: VOUT



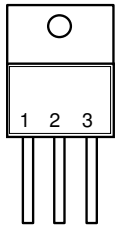

TO-263 (M3)
TOP VIEW

1: VIN
2: GND (TAB)
3: VOUT




TO-220 (T3)
TOP VIEW

1: VIN
2: GND (TAB)
3: VOUT




Example: AIC1190-18PE3TR
→ 1.8V Version, in TO-252 Lead Free Package & Tape & Reel Packing Type

## ■ ORDERING INFORMATION (Continued)

AIC1190XX-XXXXXXX

- PACKING TYPE
  - TR: TAPE & REEL
  - TB: TUBE
- PACKAGE TYPE
  - E5: TO-252-5
  - M5: TO-263-5
- P: Lead Free Commercial
  G: Green Package
- OUTPUT VOLTAGE
  - 12: 1.2V
  - 15: 1.5V
  - 18: 1.8V
  - 20: 2.0V
  - 25: 2.5V
  - 27: 2.7V
  - 30: 3.0V
  - 33: 3.3V
  - 35: 3.5V
  - 37: 3.7V
  - 38: 3.8V

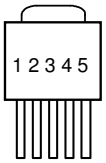
  (Of a unit of 0.1V within 0.8~4.5V, additional voltage versions are available on demand)
- ENABLE TYPE
  - L: Chip Enable Low
  - H: Chip Enable High
- B: Bypass
  A: ADJ

Example: AIC1190BH-18PM5TR

→ With Bypass Pin, Chip Enable High, 1.8V Version, in TO-263-5 Lead Free Package & Tape & Reel Packing Type

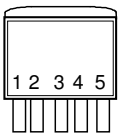
5 PIN CONFIGURATION

TO-252-5 (E5)
TOP VIEW




1: $\overline{EN}$ / EN
2: VIN
3: GND (TAB)
4: VOUT
5: BP/ ADJ

TO-263-5 (M5)
TOP VIEW




1: $\overline{EN}$ / EN
2: VIN
3: GND (TAB)
4: VOUT
5: BP/ ADJ

## ■ ORDERING INFORMATION (Continued)

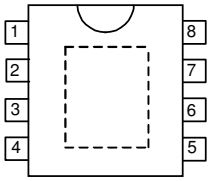
AIC1190X-XXXXXXX

- PACKING TYPE
  - TR: TAPE & REEL
  - TB: TUBE
- PACKAGE TYPE
  - R8: SOP-8
- G: Green Package
- OUTPUT VOLTAGE
  - 12: 1.2V
  - 15: 1.5V
  - 18: 1.8V
  - 20: 2.0V
  - 25: 2.5V
  - 27: 2.7V
  - 30: 3.0V
  - 33: 3.3V
  - 35: 3.5V
  - 37: 3.7V
  - 38: 3.8V

  (Of a unit of 0.1V within 0.8~4.5V, additional voltage versions are available on demand)
- ENABLE TYPE
  - L: Chip Enable Low
  - H: Chip Enable High

8 PIN CONFIGURATION

SOP-8 (R8) Exposed Pad (Heat Sink)
TOP VIEW




1: $\overline{EN}$ / EN
2: VIN
3: VOUT
4: ADJ
5: GND (TAB)
6: BP
7: GND (TAB)
8: GND (TAB)

Example: AIC1190H-18GR8TR

→ Chip Enable High, 1.8V Version, in SOP-8 Green Package & Tape & Reel Packing Type

- **Marking**

| Part No | Marking | Part No | Marking |
|---|---|---|---|
| AIC1190-xxPY3 | HBxxP | AIC1190-xxGY3 | HBxxG |

xx represents output voltage. (08=0.8V, 09=0.9V, ……., 44=4.4V, 45=4.5V)

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Input Voltage | | 7V |
| EN Pin Voltage | | 7V |
| Noise Bypass Terminal Voltage | | 7V |
| Operating Temperature Range | | -40ºC~85ºC |
| Maximum Junction Temperature | | 150ºC |
| Storage Temperature Range | | -65ºC~150ºC |
| Lead Temperature (Soldering, 10 sec) | | 260ºC |
| Thermal Resistance (Junction to Case) | SOT-223 | 15ºC /W |
| | TO-252 | 8ºC /W |
| | TO-263 | 3ºC /W |
| | TO-220 | 3ºC /W |
| | SOP-8 (Exposed Pad*) | 15ºC /W |
| Thermal Resistance (Junction to Ambient) | SOT-223 | 130ºC /W |
| (Assume no ambient airflow, no heat sink) | TO-252 | 100ºC /W |
| | TO-263 | 60ºC /W |
| | TO-220 | 50ºC /W |
| (Assume no ambient airflow) | SOP-8 (Exposed Pad*) | 60ºC /W |

**Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.**

* The package is placed on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

## ELECTRICAL CHARACTERISTICS

**($C_{IN}$ = $C_{out}$ = 2.2μF, $C_{BP}$ = 22nF, $V_{IN}$ = $V_{OUT}$ + 1V, $T_J$=25°C, unless otherwise specified) (Note 1)**

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Input Voltage | | $V_{IN}$ | 2.3 | | 6.0 | V |
| Output Voltage Tolerance | $I_{OUT}$ = 1 mA | $V_{OUT}$ | -2 | | 2 | % |
| Continuous Output Current | | $I_{OUT}$ | 1.0 | | | A |
| Quiescent Current | Chip Enable Low, $V_{EN}$ ≦0.4V, $I_{OUT}$ = 0 mA<br>Chip Enable High, $V_{EN}$ ≧1.6V, $I_{OUT}$ = 0 mA | $I_Q$ | | 60 | 110 | μA |
| GND Pin Current | Chip Enable Low, $V_{EN}$ ≦0.4V, $I_{OUT}$ = 1A<br>Chip Enable High, $V_{EN}$ ≧1.6V, $I_{OUT}$ = 1A | $I_{GND}$ | | 60 | 110 | μA |
| Standby Current | Chip Enable Low, $V_{EN}$ = $V_{IN}$<br>Chip Enable High, $V_{EN}$ = 0 | $I_{STBY}$ | | 0.1 | 0.5 | μA |
| Output Current Limit | $R_{LOAD}$ = 0.1Ω | $I_{IL}$ | 1.1 | 1.6 | | A |
| Dropout Voltage | $I_{OUT}$ = 1A, 0.8V<$V_{OUT}$<2V | $V_{DROP}$ | | | 1500 | mV |
| | $I_{OUT}$ = 1A, 2V<$V_{OUT}$<2.8V | | | 500 | 900 | |
| | $I_{OUT}$ = 1A, $V_{OUT}$>2.8V | | | 440 | 700 | |
| Line Regulation | $V_{IN}$ = $V_{OUT}$ + 1V to 6.0V | $\Delta V_{LIR}$ | | | 10 | mV |
| Load Regulation | $I_{OUT}$ = 1mA to 1A | $\Delta V_{LOR}$ | | 1 | 20 | mV |
| Ripple Rejection (Note 2) | f=1KHz, Ripple=0.5Vp-p, | PSRR | | 70 | | dB |
| Output Noise Voltage | $C_{BP}$ = 22nF, f= 10~100KHz | | | 24 | | μVrms |
| Temperature Coefficient | | TC | | 50 | | ppm/℃ |
| Thermal Shutdown Temperature | $V_{IN}$ = $V_{OUT}$ + 1V | $T_{SD}$ | | 150 | | ℃ |
| Thermal Shutdown Hysteresis | | $\Delta T_{SD}$ | | 20 | | ℃ |
| **ADJ Pin Specifications** | | | | | | |
| ADJ Pin Current | $V_{ADJ}$ = $V_{REF}$ | $I_{ADJ}$ | | 10 | 100 | nA |
| ADJ Pin Threshold | | $VTH_{(ADJ)}$ | 0.05 | 0.1 | 0.2 | V |
| Reference Voltage Tolerance | | $V_{REF}$ | 0.784 | 0.8 | 0.816 | V |

## ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Shutdown Pin Specifications** | | | | | | |
| Shutdown Pin Current | $V_{EN}$ = $V_{IN}$ or GND | $I_{EN}$ | | 0 | 100 | nA |
| Shutdown Exit Delay Time | $I_{OUT}$ = 30mA | $\Delta t$ | | 100 | | µS |
| Max Output Discharge Resistance to GND during Shutdown | | RDSON_CLMP | | 20 | 100 | Ω |
| Shutdown Input Threshold | Chip Enable Low, Output OFF, $V_{IN}$ = 2.3V to 6.0V<br>Chip Enable High, Output ON, $V_{IN}$ = 2.3V to 6.0V | $V_{ENH}$ | 1.6 | | | V |
| | Chip Enable Low, Output ON, $V_{IN}$ = 2.3V to 6.0V<br>Chip Enable High, Output OFF, $V_{IN}$ = 2.3V to 6.0V | $V_{ENL}$ | | | 0.4 | |

Note 1: Specifications are production tested at $T_A$=25℃. Specifications over the -40℃ to 85℃ operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: Connecting a 22nF bypass capacitor to BP pin can improve AIC1190 PSRR in High frequency.

## TYPICAL PERFORMANCE CHARACTERISTICS

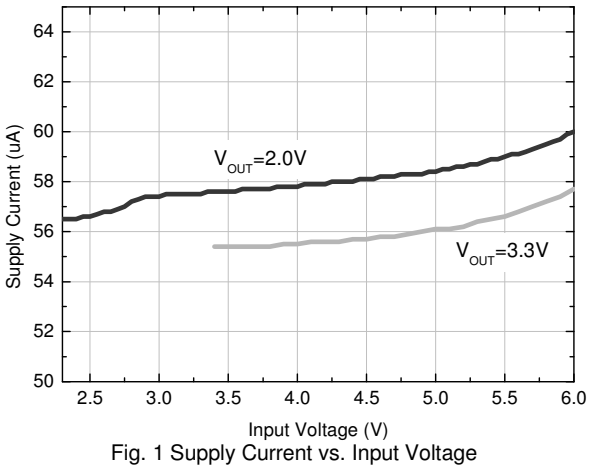



Fig. 1 Supply Current vs. Input Voltage

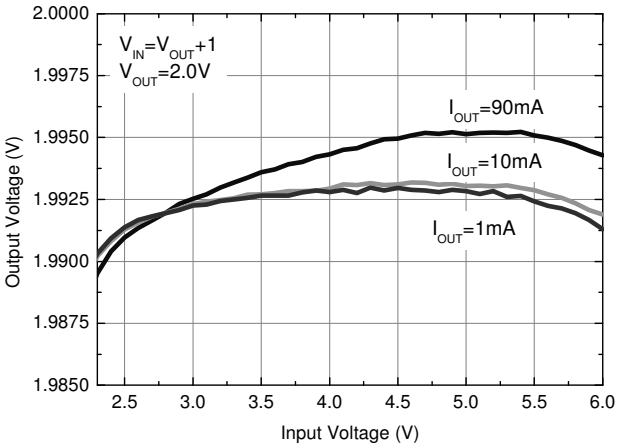



Fig. 2 Output Voltage vs. Input Voltage

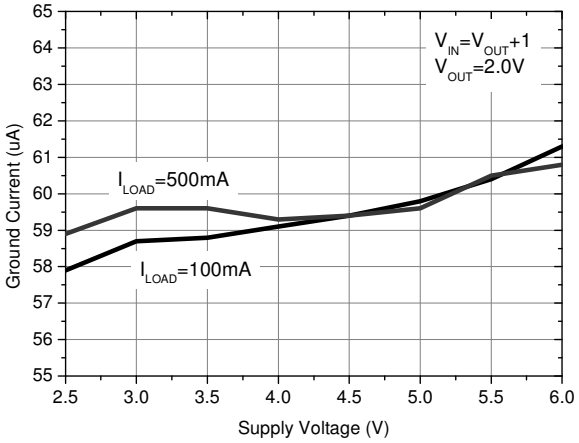



Fig. 3 Ground Current

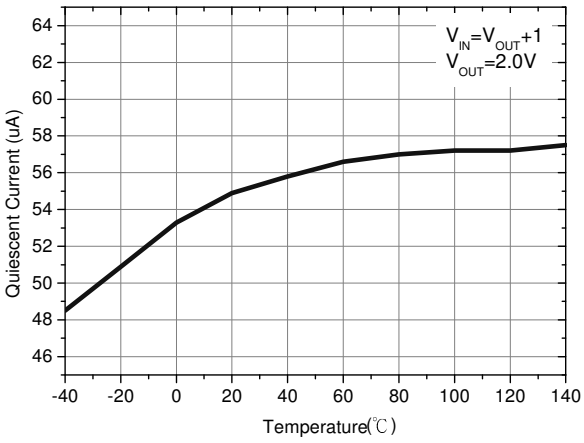



Fig. 4 Quiescent Current vs. Temperature

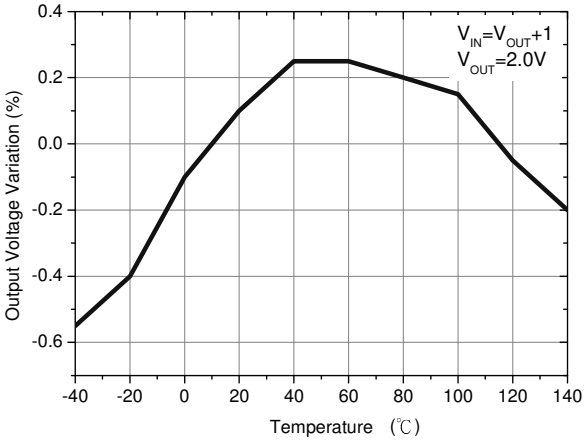



Fig. 5 Output Voltage vs. Temperature

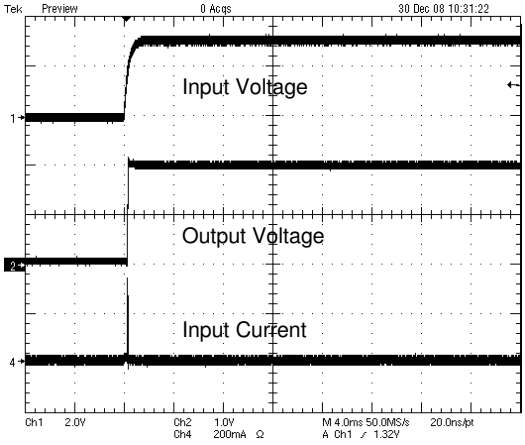



Fig.6 Start-up waveform without bypass capacitance

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

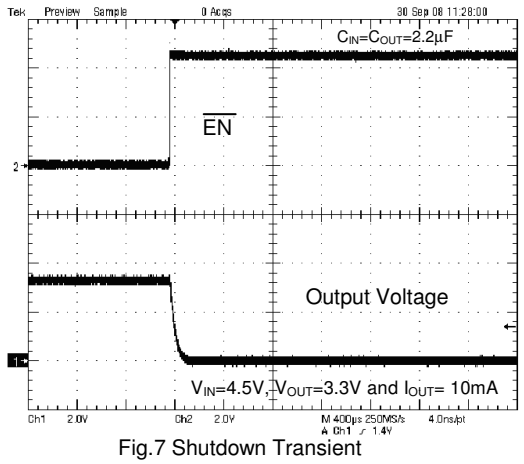



Fig.7 Shutdown Transient

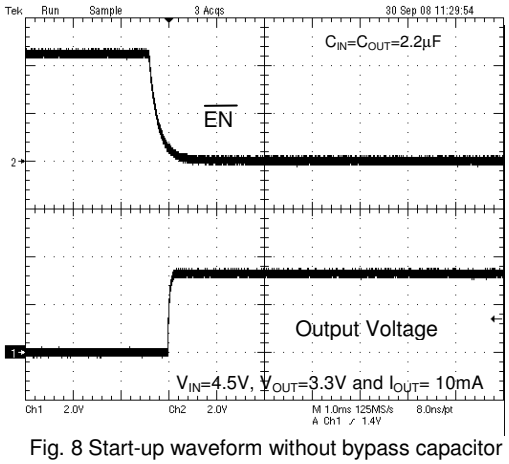



Fig. 8 Start-up waveform without bypass capacitor

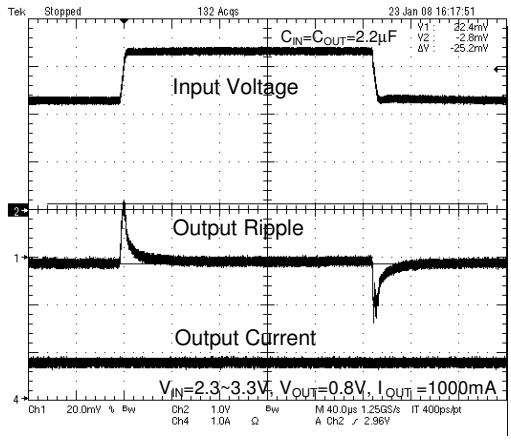



Fig. 9 Line Transient

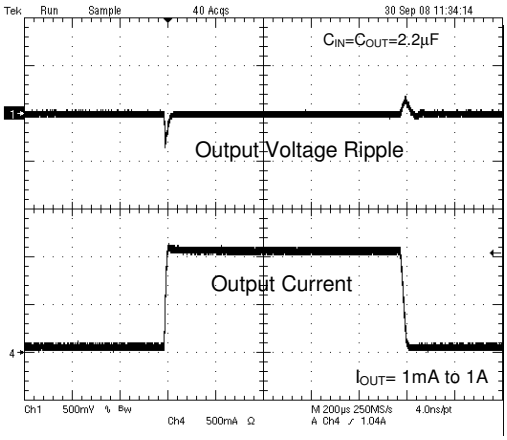



Fig.10 Load Transient Response at $V_{IN}$=4.3V, $V_{OUT}$=3.3V

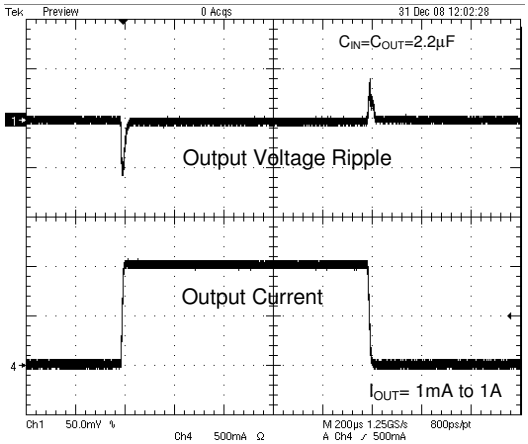



Fig.11 Load Transient Response at $V_{IN}$=2.3V, $V_{OUT}$=0.8V

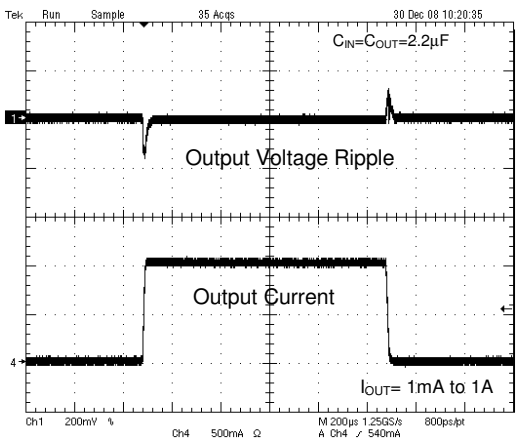



Fig.12 Load Transient Response at $V_{IN}$=3.0V, $V_{OUT}$=2.0V

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

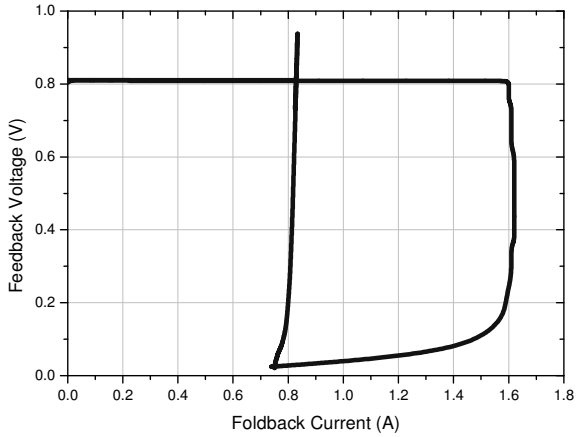



Fig. 13 Current Fold back (Vout<0.2V)

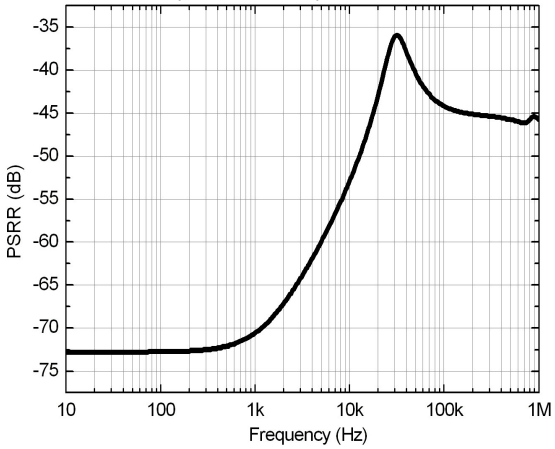
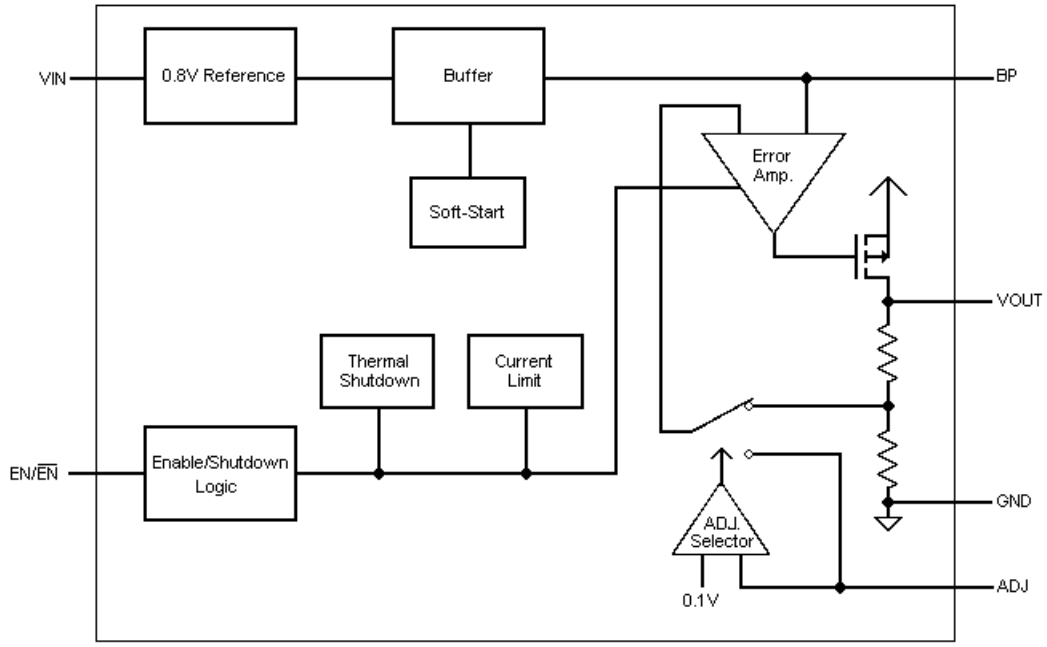



Fig. 14 PSRR Curve

## BLOCK DIAGRAM




## PIN DESCRIPTION

VIN – Power supply input pin. Bypass with a 2.2µF capacitor to GND

GND – Ground.

VOUT – Regulator Output pin. Sources up to 1A.

$\overline{EN}$ (5 Pin and 8 Pin) – Chip Enable (Active Low). This pin isn't allowed to float.

EN (5 Pin and 8 Pin) – Chip Enable (Active High). This pin isn't allowed to float.

BP (5 Pin and 8 Pin) – Bypass pin. It can connect to external 22nF capacitor to GND to reduce output noise. The bypass pin could be floating if it's unnecessary (Keep floating cannot pull low and pull high).

ADJ (5 Pin and 8 Pin) – The output voltage can either be set by the internal feedback resistors when this pin is grounded, or be set by the external feedback resistors when using a resistive divider.

## APPLICATION INFORMATION

The AIC1190 is a high performance linear regulator that provides low-dropout voltage and low quiescent-current. The device is available in an adjustable version and fixed output voltages ranging from 1.2V to 3.8V, and the device can supply loads up to 1A.

**SHUTDOWN**

By connecting $\overline{EN}$(EN) pin to $V_{IN}$(ground), the AIC1190 can be shut down to reduce the supply current to 0.1μA(typ.). At this operation mode, the output voltage of AIC1190 is equal to 0V.

**CURRENT LIMIT**

The AIC1190 includes a current limiter, which monitors and controls the maximum output current. If the output is overloaded or shorted to ground, this can protect the device from being damaged.

**THERMAL PROTECTION**

The AIC1190 includes a thermal-limiting circuit, which is designed to protect the device against overload condition. When the junction temperature exceeds $T_J$=150ºC, the thermal-limiting circuit turns off the pass transistor and allows the IC to cool. For continuous load condition, maximum rating of junction temperature must not be exceeded.

**INPUT-OUTPUT CAPACITORS**

Linear regulators require input and output capacitors to maintain stability. Input capacitor at 2.2μF with a 2.2μF ceramic output capacitor is recommended. To avoid oscillation, it is recommended to follow the figure of "Region of Stable $C_{OUT}$ ESR vs. Load Current" to choose proper capacitor specifications.

When choosing the input and output ceramic capacitors, X5R and X7R types are recommended because they retain their capacitance over wider ranges of voltage and temperature than other types.

**NOISE BYPASS CAPACITOR**

A 22nF bypass capacitor at BP pin can reduce output voltage noise. The bypass pin can be floating if it's unnecessary.

**OUTPUT VOLTAGE PROGRAMMING**

The output voltage of AIC1190 linear regulator can be set by its internal feedback resistors when the ADJ pin is grounded. In addition, the output voltage of AIC1190 linear regulator can be set by the external feedback resistors when connecting a resistive divider $R_1$ and $R_2$. While connecting a resistive divider, $V_{OUT}$ can be calculated as:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider should sit as close to ADJ pin as possible.

**POWER DISSIPATION**

The maximum power dissipation of AIC1190 depends on the thermal resistance of its case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The rate of temperature rise is greatly affected by the mounting pad configuration on the PCB, the board material, and the ambient temperature. When the IC mounting with good thermal conductivity is used, the junction temperature will be low even when large power dissipation applies.

The power dissipation across the device is

$P = I_{OUT} (V_{IN}-V_{OUT})$

The maximum power dissipation is:

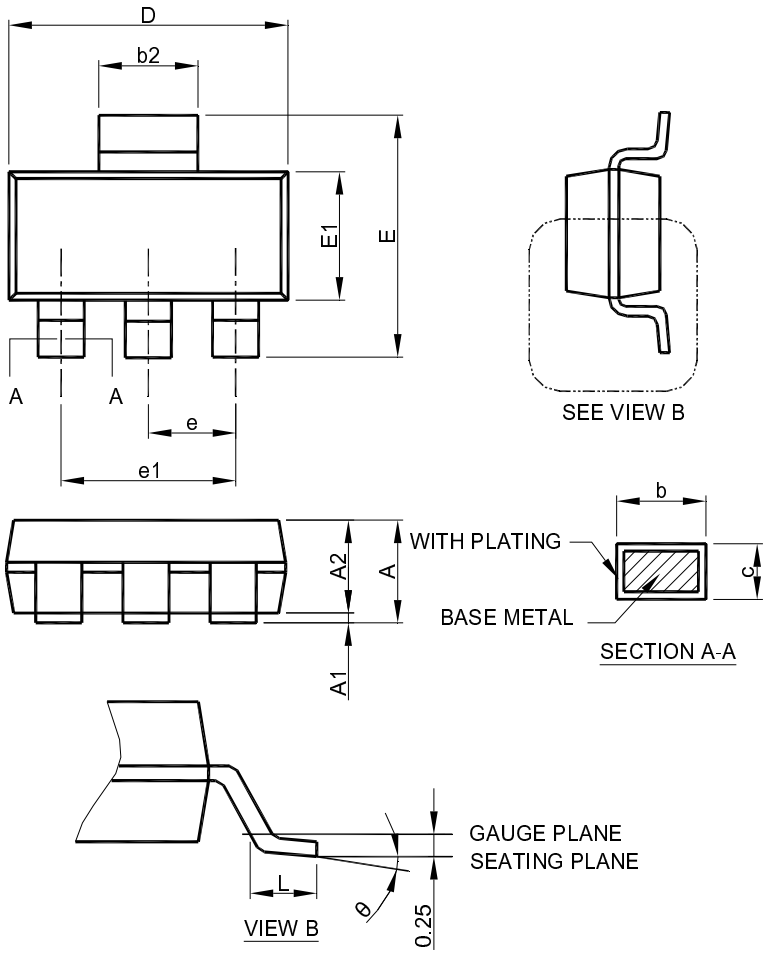
$$P_{MAX} = \frac{(T_{J\text{-}max} - T_A)}{R\theta_{JA}}$$

Where $T_{J\text{-}max}$ is the maximum allowable junction temperature (150°C), and $T_A$ is the ambient temperature suitable in application.

As a general rule, the lower temperature is, the better reliability of the device is. So the PCB mounting pad should provide maximum thermal conductivity to maintain low device temperature.

## PHYSICAL DIMENSIONS

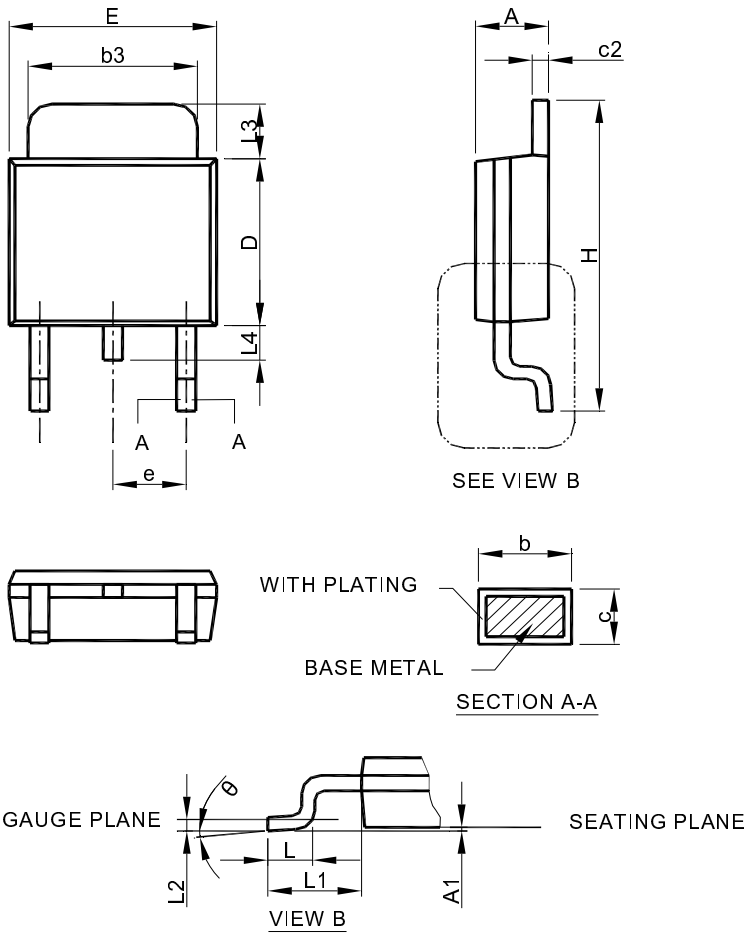
- **SOT-223 PACKAGE OUTLINE DRAWING**




Note: 1. Refer to JEDEC TO-261AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E1" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

| SYMBOL | SOT-223 | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | | 1.80 |
| A1 | 0.02 | 0.10 |
| A2 | 1.55 | 1.65 |
| b | 0.66 | 0.84 |
| b2 | 2.90 | 3.10 |
| c | 0.23 | 0.33 |
| D | 6.30 | 6.70 |
| E | 6.70 | 7.30 |
| E1 | 3.30 | 3.70 |
| e | 2.30 BSC | |
| e1 | 4.60 BSC | |
| L | 0.90 | |
| θ | 0° | 8° |

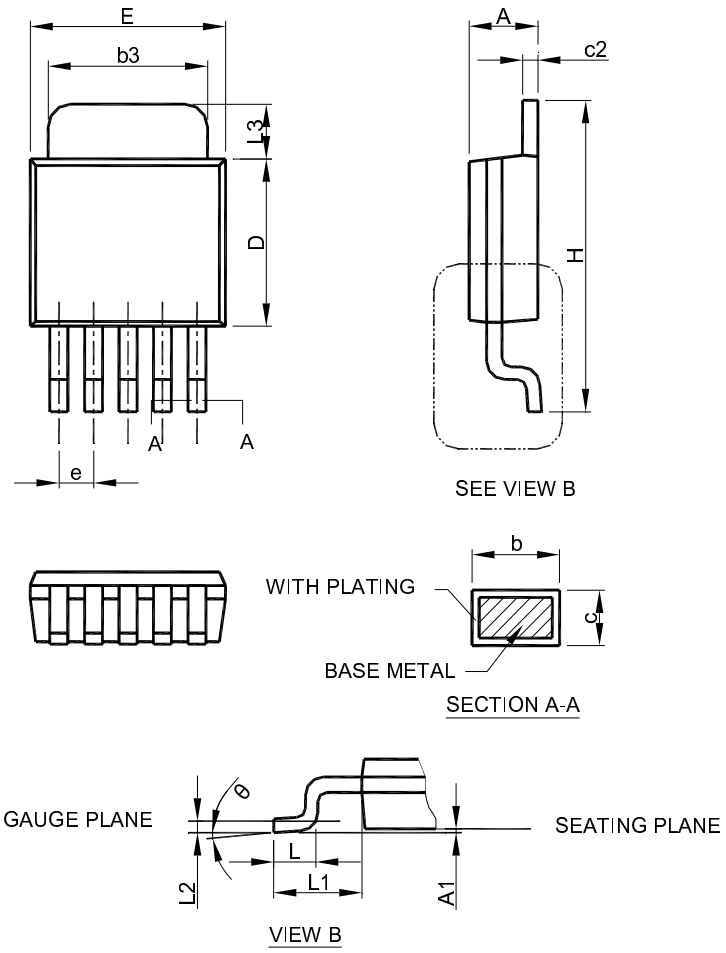
## • TO-252-3L PACKAGE OUTLINE DRAWING




Note: 1. Refer to JEDEC TO-252AA and AB.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

| SYMBOL | TO-252-3L | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.19 | 2.38 |
| A1 | 0.00 | 0.13 |
| b | 0.64 | 0.89 |
| b3 | 4.95 | 5.46 |
| c | 0.46 | 0.61 |
| c2 | 0.46 | 0.89 |
| D | 5.33 | 6.22 |
| E | 6.35 | 6.73 |
| e | 2.28 BSC | |
| H | 9.40 | 10.41 |
| L | 1.40 | 1.78 |
| L1 | 2.67 REF | |
| L2 | 0.51 BSC | |
| L3 | 0.89 | 2.03 |
| L4 | -- | 1.02 |
| θ | 0° | 8° |

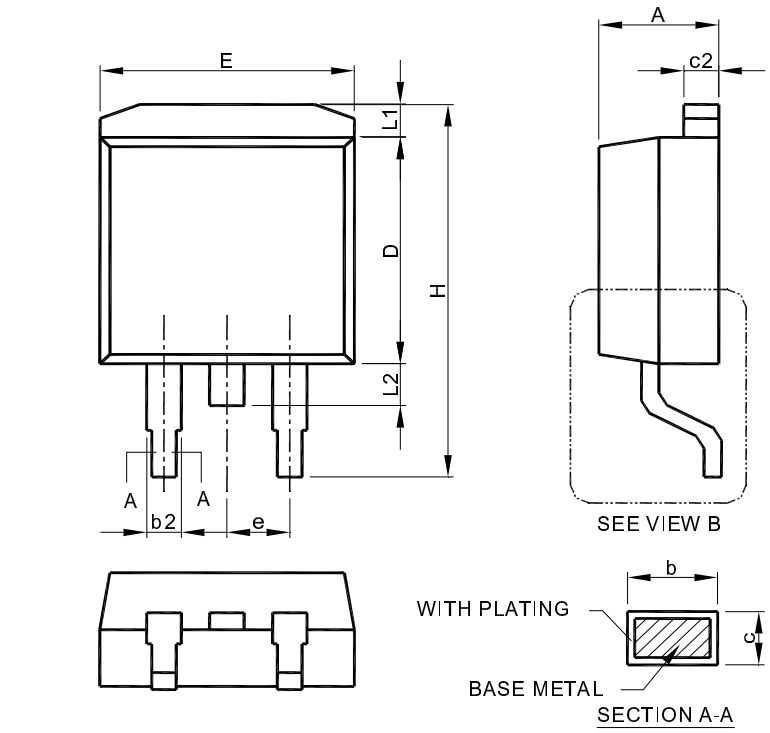
## TO-252-5L PACKAGE OUTLINE DRAWING

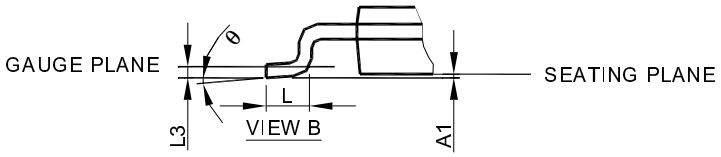



| SYMBOL | TO-252-5L | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.19 | 2.38 |
| A1 | 0.00 | 0.13 |
| b | 0.51 | 0.71 |
| b3 | 4.32 | 5.46 |
| c | 0.46 | 0.61 |
| c2 | 0.46 | 0.89 |
| D | 5.33 | 6.22 |
| E | 6.35 | 6.73 |
| e | 1.27 BSC | |
| H | 9.40 | 10.41 |
| L | 1.40 | 1.78 |
| L1 | 2.67 REF | |
| L2 | 0.51 BSC | |
| L3 | 0.89 | 2.03 |
| q | 0° | 8° |

Note: 1. Refer to JEDEC TO-252AD and AB.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

## ● TO-263-3L PIN PACKAGE OUTLINE DRAWING

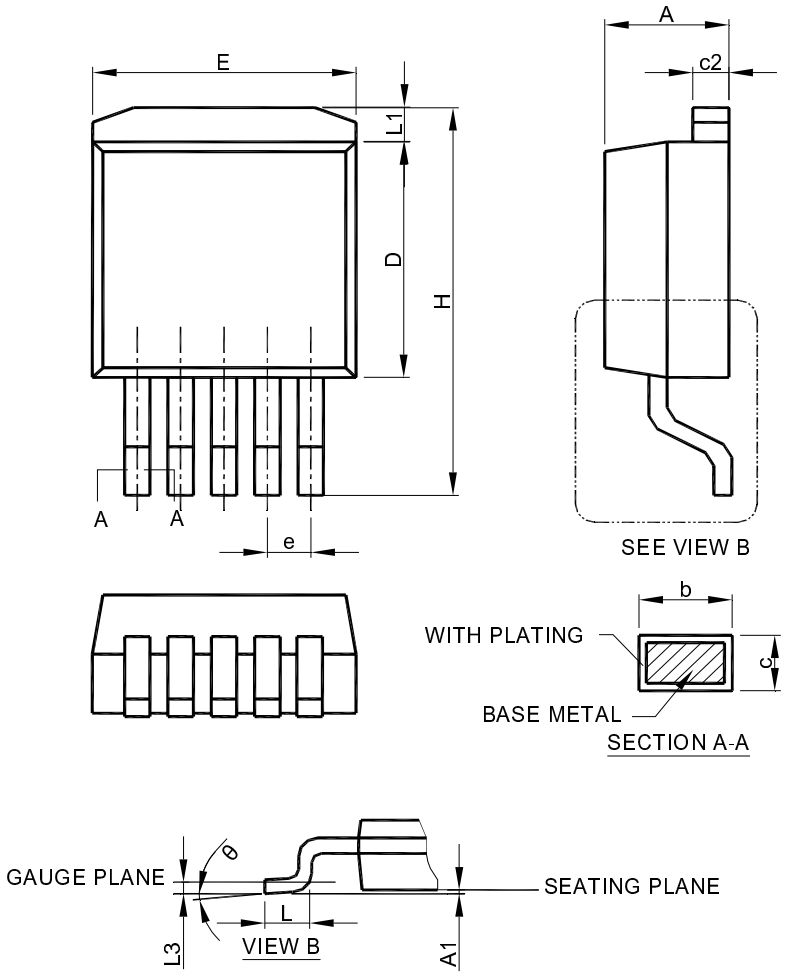



Note: 1. Refer to JEDEC TO-263AB.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

| SYMBOL | TO-263-3L | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 4.06 | 4.83 |
| A1 | 0.00 | 0.25 |
| b | 0.51 | 0.99 |
| b2 | 1.14 | 1.78 |
| c | 0.38 | 0.74 |
| c2 | 1.14 | 1.65 |
| D | 8.38 | 9.65 |
| E | 9.65 | 10.67 |
| e | 2.54 BSC | |
| H | 14.61 | 15.88 |
| L | 1.78 | 2.79 |
| L1 | -- | 1.68 |
| L2 | -- | 1.78 |
| L3 | 0.25 BSC | |
| q | 0° | 8° |

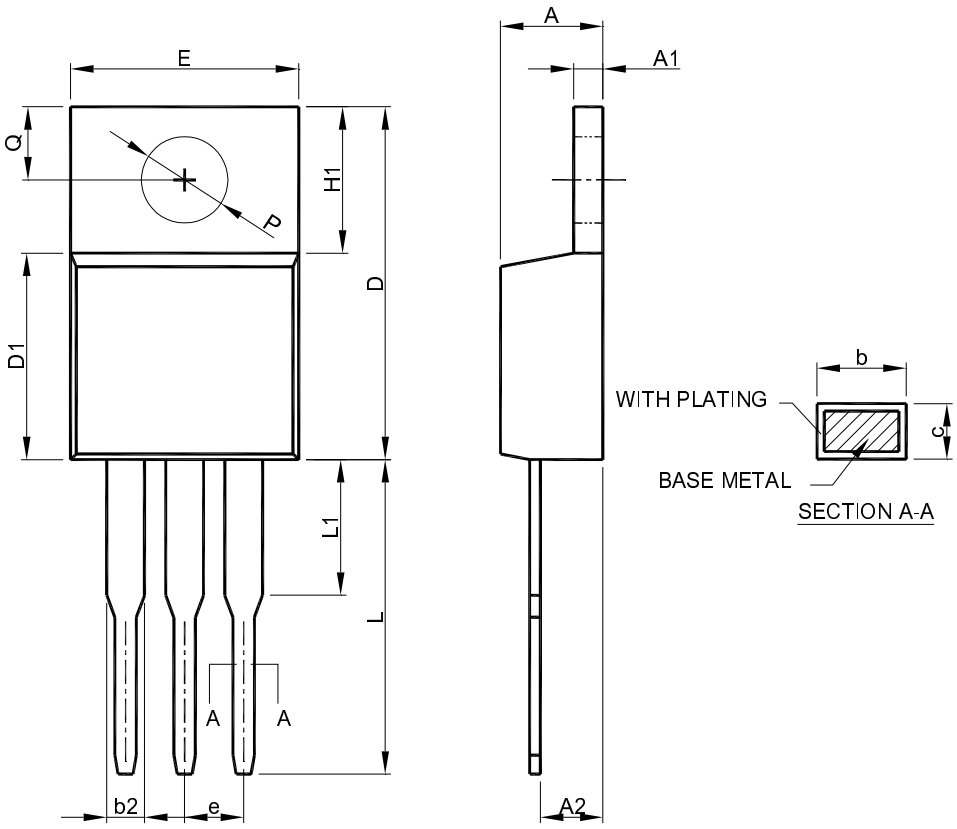
## ● TO-263-5L PACKAGE OUTLINE DRAWING




| SYMBOL | TO-263-5L | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 4.06 | 4.83 |
| A1 | 0.00 | 0.25 |
| b | 0.51 | 0.99 |
| c | 0.38 | 0.74 |
| c2 | 1.14 | 1.65 |
| D | 8.38 | 9.65 |
| E | 9.65 | 10.67 |
| e | 1.70 BSC | |
| H | 14.61 | 15.88 |
| L | 1.78 | 2.79 |
| L1 | -- | 1.68 |
| L3 | 0.25 BSC | |
| q | 0° | 8° |

Note: 1. Refer to JEDEC TO-263BA.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

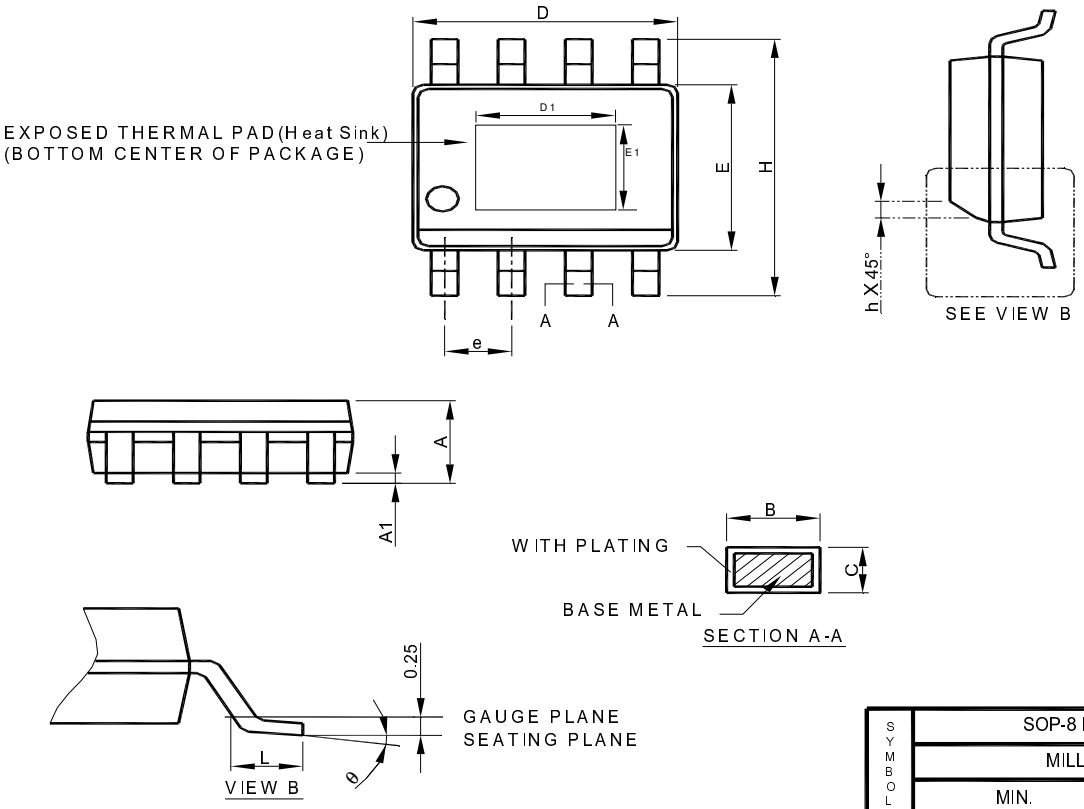
## ● TO-220 PACKAGE OUTLINE DRAWING




| SYMBOL | TO-220 | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 3.56 | 4.82 |
| A1 | 0.51 | 1.39 |
| A2 | 2.04 | 2.92 |
| b | 0.38 | 1.01 |
| b2 | 1.15 | 1.77 |
| c | 0.35 | 0.61 |
| D | 14.23 | 16.51 |
| D1 | 8.38 | 9.02 |
| E | 9.66 | 10.66 |
| e | 2.54 BSC | |
| H1 | 5.85 | 6.85 |
| L | 12.70 | 14.73 |
| L1 | -- | 6.35 |
| P | 3.54 | 4.08 |
| Q | 2.54 | 3.42 |

Note: 1. Refer to JEDEC TO-220AB.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D1" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

- **SOP-8 Exposed Pad PACKAGE OUTLINE DRAWING**




| SYMBOL | SOP-8 Exposed Pad(Heat Sink) | |
|---|---|---|
| | MILLIMETERS | |
| | MIN. | MAX. |
| A | 1.35 | 1.75 |
| A1 | 0.00 | 0.15 |
| B | 0.31 | 0.51 |
| C | 0.17 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| q | 0° | 8° |
| D1 | 1.5 | 3.5 |
| E1 | 1.0 | 2.55 |

Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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