AZ DISPLAYS, INC.

SPECIFICATIONS FOR

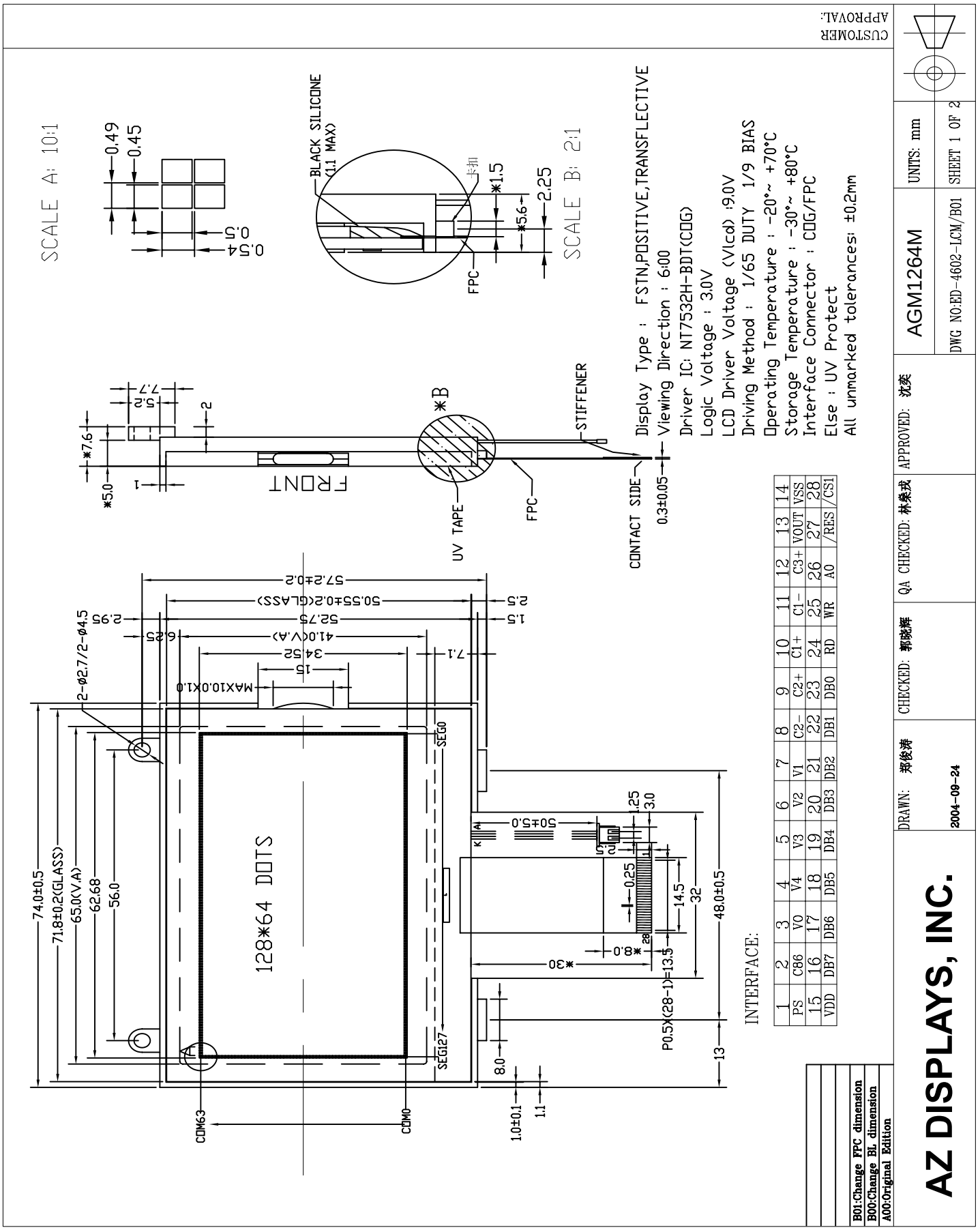
LIQUID CRYSTAL DISPLAY

PART NUMBER:	AGM1264M
DATE:	July 8, 2005

1. General Specifications

Item	☑Standard Value	Unit
Display Pattern	☑Dot-Graphic ☐Character ☐Digits ☐_____ ☐with ICON	Dots
Color	☐Mono. ☑Grayscale ☐_____	
Module Dimension	74.0 X 59.45 X 7.6	mm
Viewing Area	65.0 X 41.0	mm
Active Area	62.68 X 34.52	mm
Character Size		mm
Character Pitch		mm
DOT Size	0.45 X 0.50	mm
DOT Pitch	0.49 X 0.54	mm
LCD Type	☐TN, Positive ☐TN, Negative ☐HTN, Positive ☐HTN, Negative ☐STN, Yellow-Green ☐STN, Gray ☐STN, Blue ☑FSTN, Positive ☐FSTN, Negative ☐Color STN ☐FM LCD	
Polarizer Type	☑Transflective ☐Transmissive ☐Reflective ☐Anti-Glare	
View Direction	☑6H ☐12H ☐____	
LCD Controller & Driver	NT7532H-BDT	
LCD Driving Method	1/65duty, 1/9bias	
Interface Type	☐I^2C ☐4-wire Serial ☐3-wire Serial ☐6800 ☐8080 ☐4-bit ☑ Change by hardware	
Backlight Type	☑LED ☐Bottom ☐Single Side ☐Dual Side ☐EL ☐CCFL ☐____	
Backlight Color	☑Yellow-Green ☐White ☐Amber ☐Blue ☐Red ☐_____	
EL/CCFL Driver type	☐Build-in ☐External	
DC-DC Converter	☑Build-in ☐External	
Operation Temperature (°C)	-20-70 (T_{OPL} T_{OPH}) deg.	
Storage Temperature (°C)	-30-80 (T_{STL} -- T_{STH}) deg.	

2. Mechanical Diagram

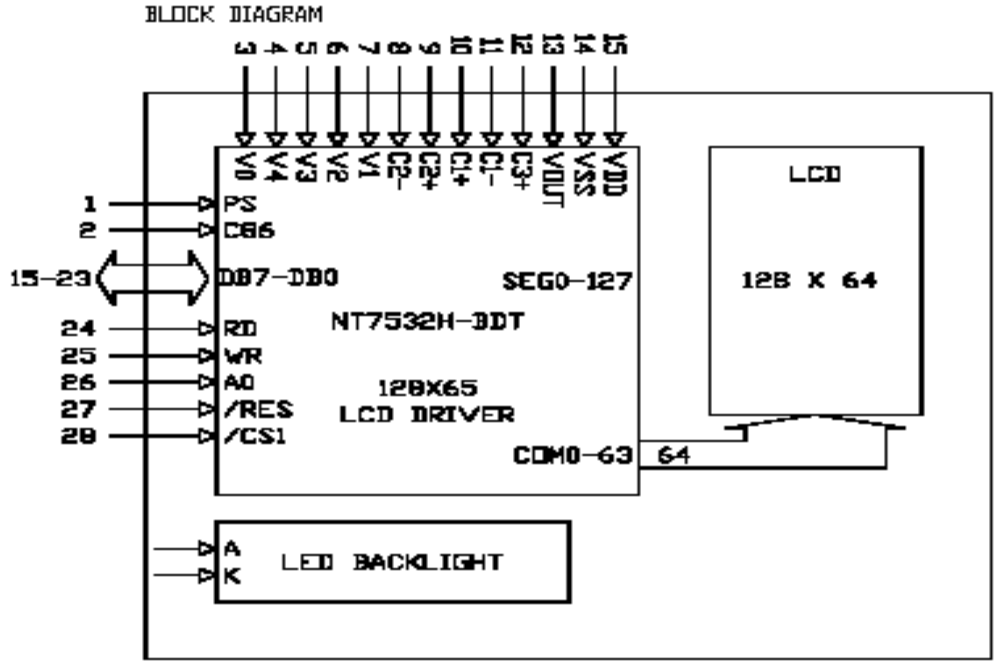


3. I/O Terminals

3.1 Pin Description

Pin NO.	Symbol	Function Description
1	PS	Parallel or Serial data input select
2	C86	MPU Interface select(6800 or 8080)
3	V0	LCD driver supply voltage
4	V4	LCD driver supply voltage
5	V3	LCD driver supply voltage
6	V2	LCD driver supply voltage
7	V1	LCD driver supply voltage
8	C2-	For internal DC/DC voltage converter
9	C2+	For internal DC/DC voltage converter
10	C1+	For internal DC/DC voltage converter
11	C1-	For internal DC/DC voltage converter
12	C3+	For internal DC/DC voltage converter
13	VOUT	DC/DC voltage converter output
14	VSS	Logic Ground.
15	VDD	Logic supply voltage.
16-23	DB7-DB0	Quasi-Bidirectional I/O Data Bus. Three state I/O common terminal. DB0 (LSB) ... DB7 (MSB)
24	/RD(E)	When connected to an 8080 MPU, it is active LOW. This pad is connected to the RD signal of the 8080MPU, and the NT7532 data bus is in an output status when this signal is "L" When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
25	/WR(R/W	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When W R/ = "H": Read When W R/ = "L": Write
26	A0	Data or Instruction. A0 = H DB<0:7>: Display RAM data A0 = L DB<0:7>: Instruction data
27	/RES	14 16 RES I When RES is set to "L", the settings are initialized. The reset operation is performed by the RES signal level
28	/CS1	This is the chip select signal. When CS1="L", then the chip select becomes active, and data/command I/O is enabled.

3.2 Block Diagram



4. Electro-optical Specifications

4.1 Absolute Maximum Ratings

No	Item	Symbol	Min.	Max.	Unit
1	Supply Voltage For Logic	V_{DD} -V_{SS}	-0.3	3.6	V
2	Supply Voltage For Lcd Driver	V_{LCD}	-0.3	13.5	V
3	Input Voltage	V_I	-0.3	V_{DD}+0.3	V

Note: Operating Temperature and Storage Temperature can be found in *1.General Specifications.*

4.2 Optical Characteristics(1)

No	Item		Symbol	Condition	Min.	Typ.	Max.	Unit
1	Contrast Ratio		Cr	Ta=23±3°C V_{LCD} = Typ. (2)	-	4.03	-	-
2	Response time		T_{ON}	Ta=23±3°C	-	110		ms
3	Response time		T_{OFF}	Ta=23±3 °C	-	170		ms
4	Viewing Angle	3H	Θ1	Cr = 2 Ta=23±3 °C		48	-	Deg.
5		9H	Θ2			50	-	Deg.
6		6H	Θ3			28	-	Deg.
7		12H	Θ4		-	55	-	Deg.

Note:

(1) See Appendix 1 Definition of Optical Characteristics for detail.

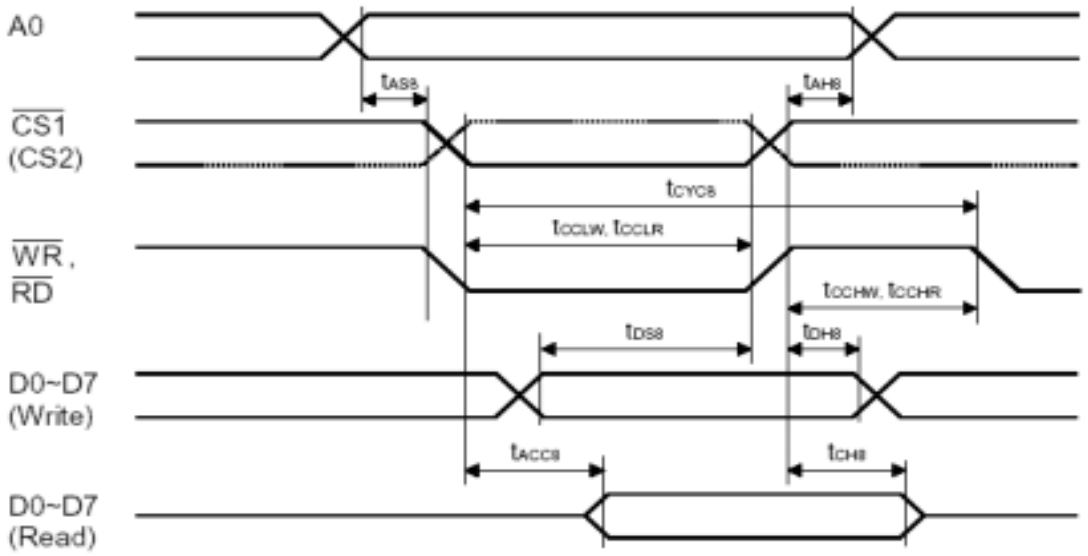
(2) V_{LCD} can be found in 4.2 Electrical Characteristics *Supply Voltage for LCD Driver*

4.3 Electrical Characteristics

No	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Supply Voltage for Logic	V_{DD}-V_{SS}		2.4	/	3.5	V
2	Supply Voltage for LCD Driver	V_O-V_{SS} (V_{LCD})	Ta=23±3 °C	9.5	9.6	9.7	V
3	Supply Current for Logic	I_{DD}		-	0.4	1.5	mA
4	Oscillation Frequency	F_{osc}	Ta=23±3 °C	27	33	39	KHz
5	Input High Voltage	V_{IH}	-	0.7 V_{DD}		V_{DD}	V
6	Input Low Voltage	V_{IL}	-	-0.3	-	0.4	V
7	Output High Voltage	V_{OH}	-	2.0	-	-	V
8	Output Low Voltage	V_{OL}	-	-	-	0.4	V
9	Supply Current for LED Backlight	I_{LED}	V_{LED} = Typ. Ta=23±3 °C	-	50	-	mA
10	Supply Voltage for LED Backlight	V_{LED}	I_{LED} = Typ. Ta=23±3 °C	-	42	-	V

4.4 Timming Characteristics

1. System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

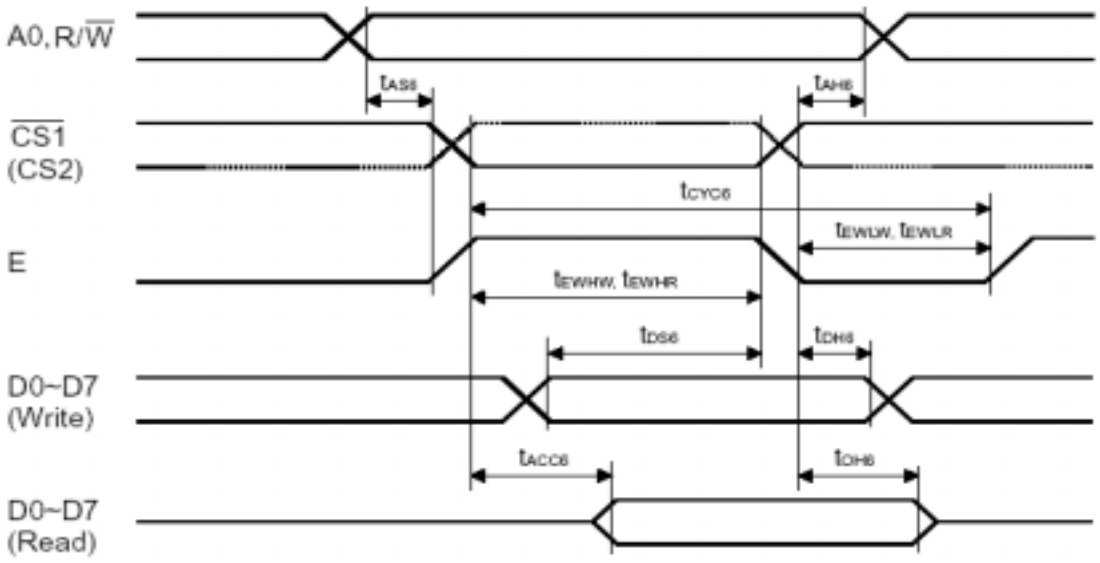
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	300	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	$\overline{WR}$
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	$\overline{RD}$
t_{CCHW}	Control high pulse width (write)	120	-	-	ns	$\overline{WR}$
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	$\overline{RD}$
t_{DS6}	Data setup time	40	-	-	ns	D0~D7
t_{DH6}	Data hold time	15	-	-	ns	
t_{ACC6}	$\overline{RD}$ access time	-	-	140	ns	D0~D7, CL = 100pF
t_{OH6}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < (t_{CYC6} - t_{CCLW} - t_{CCHW}) for write, ($t_r + t_f$) < (t_{CYC6} - t_{CCLR} - t_{CCHR}) for read.

*2. All timing is specified using 20% and 80% of VDD as the reference.

*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and $\overline{WR}$ or $\overline{RD}$ is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)

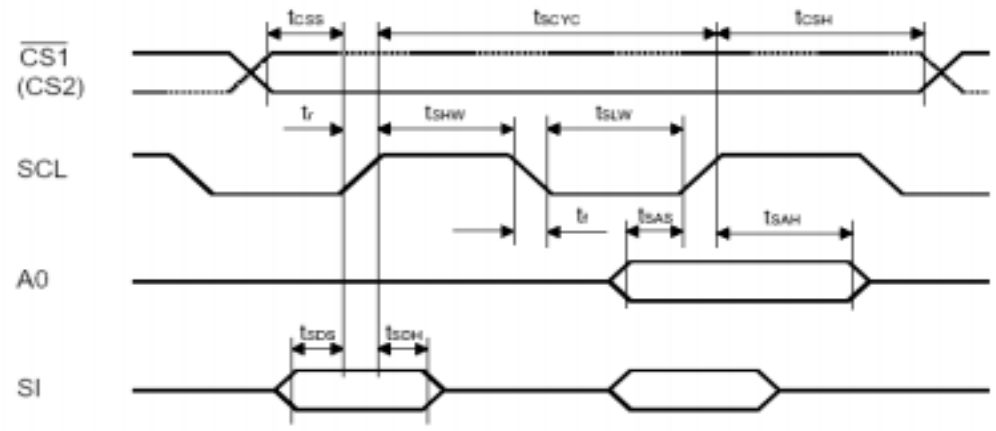


(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	300	-	-	ns	
t_{EWHW}	Control low pulse width (write)	90	-	-	ns	$\overline{WR}$
t_{EWHR}	Control low pulse width (read)	120	-	-	ns	$\overline{RD}$
t_{EWLW}	Control high pulse width (write)	120	-	-	ns	$\overline{WR}$
t_{EWLR}	Control high pulse width (read)	60	-	-	ns	$\overline{RD}$
t_{DS6}	Data setup time	40	-	-	ns	D0~D7
t_{DH6}	Data hold time	15	-	-	ns	
t_{ACC6}	$\overline{RD}$ access time	-	-	140	ns	D0~D7, CL = 100pF
t_{OH6}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for write, ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{EWLW} and t_{EWLR} are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and E is high.

3. Serial Interface Timing



(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	100	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	100	-	-	ns	SCL
t_{SAS}	Address setup time	150	-	-	ns	D/I
t_{SAH}	Address hold time	150	-	-	ns	D/I
t_{SDS}	Data setup time	100	-	-	ns	SDI
t_{SDH}	Data hold time	100	-	-	ns	SDI
t_{CSS}	Chip select setup time	150	-	-	ns	$\overline{CS1}$, CS2
t_{CSH}	Chip select hold time	150	-	-	ns	$\overline{CS1}$, CS2

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
*2. All timing is specified using 20% and 80% of VDD as the standard.

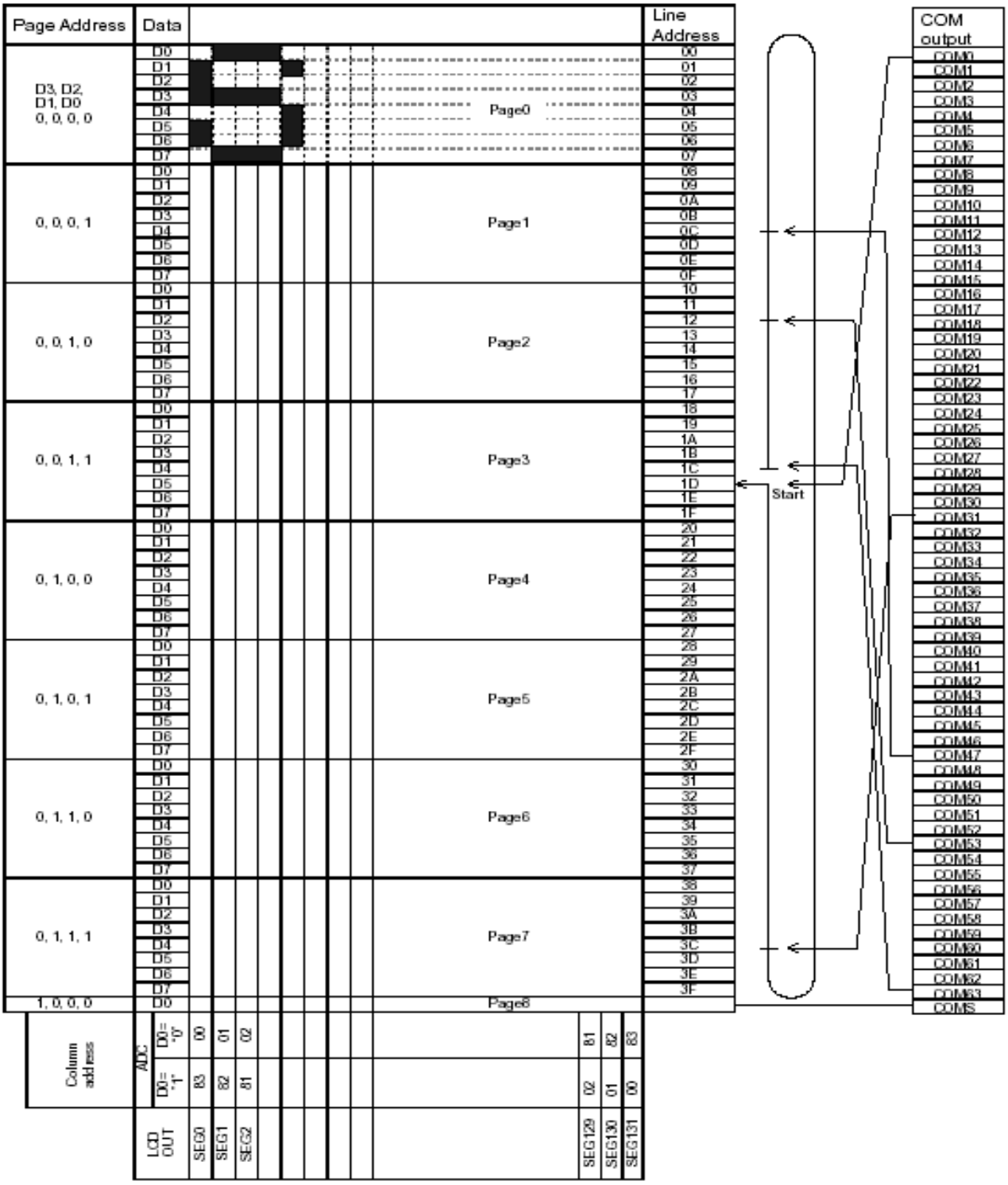
5. Programming

5.1 Instruction Table

Command	A0	RD	WR	Code D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when goes high, and turn off when goes low
(2) Set Display Start Line	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Set Page Address	0	1	0	1	0	1	1	Page Address				B0h to BFh	Set the display data RAM page in Page Address register
(4) Set Column Address	0	1	0	0	0	0	1	Higher Column Address				00h to 1Fh	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Selects normal display (0) or entire display on
(11)Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Selects COM output scan direction *: invalid data
(16)Set Power Control	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Selects the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Selects internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	0	0	1	0	1	0	1	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(23)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

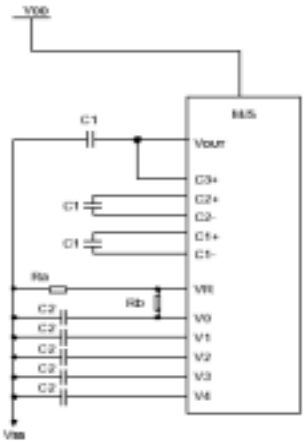
Note: Do not use any other command, or system malfunction may result.

5.2 Display Data RAM

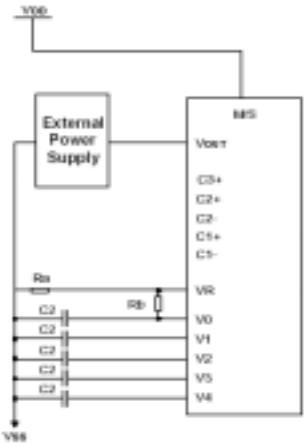


6. Power Supply

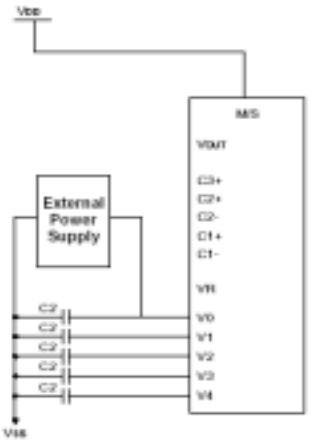
-When using all LCD power circuits
(Voltage converter regulator and follower)
(In case of 3X boosting circuit)



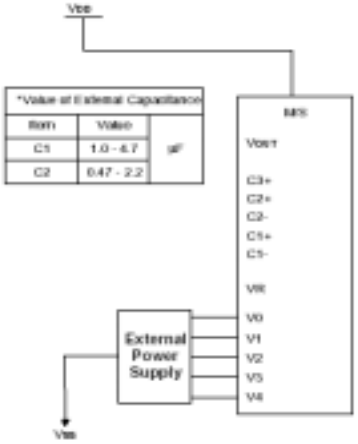
-When not using voltage booster circuits



-When only using voltage follower



-When not using internal LCD power supply circuits



$V0 = (1+Rb/Ra)*V_{EV} = (1+Rb/Ra)* (1-(63-\alpha)/162)*VREG$

Appendix 1

1. Optical Definitions

Note 1: Contrast Ratio Test

A. Contrast ratio is calculated by the following formula when the output voltage (Fig.2-a, positive type; Fig 2-b,negative type) is obtained from the next electro-optical test system (Fig.1)
B. Conditions of Testing: Accord to the LCD s driving method and operating voltage (Vop)
C. The formula:

$$\text{Contrast ratio} = \frac{\text{Photometer output voltage when non-select waveform is applying}}{\text{Photometer output voltage when select waveform is applying}} \quad \text{(positive type)}$$

$$\text{Contrast ratio} = \frac{\text{Photometer output voltage when select waveform is applying}}{\text{Photometer output voltage when non-select waveform is applying}} \quad \text{(negative type)}$$

D. Test system:

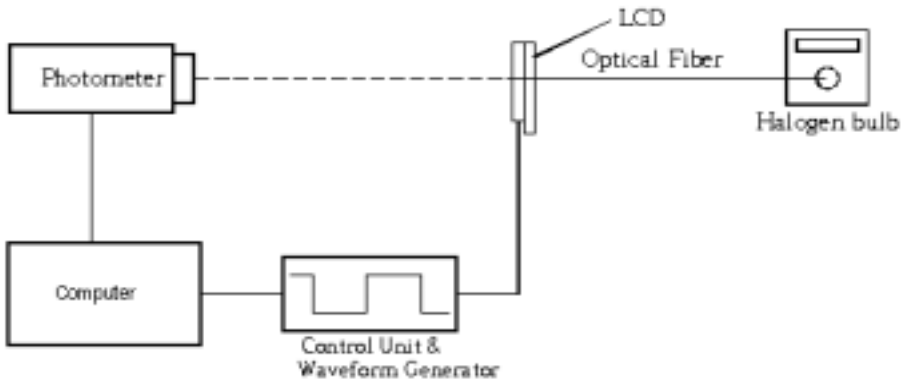


Fig. 1

Note 2: Response time

A. Rise time is defined as the time required for the transmission to change from 90% to 10%.
B. Fall time is defined as the time required for the transmission to change from 10% to 90%.
C. On time is defined as the time required for the transmission to change from 100% to 10%.
D. Off time is defined as the time required for the transmission to change from 10% to 100%.

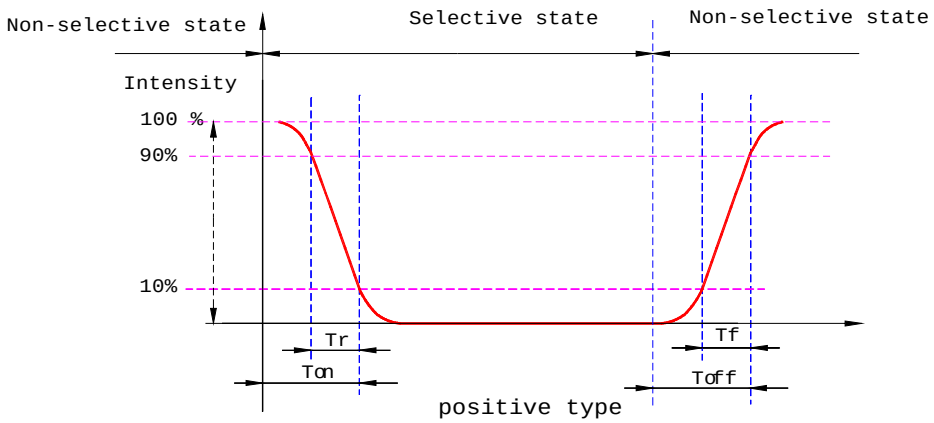


Fig.2-a

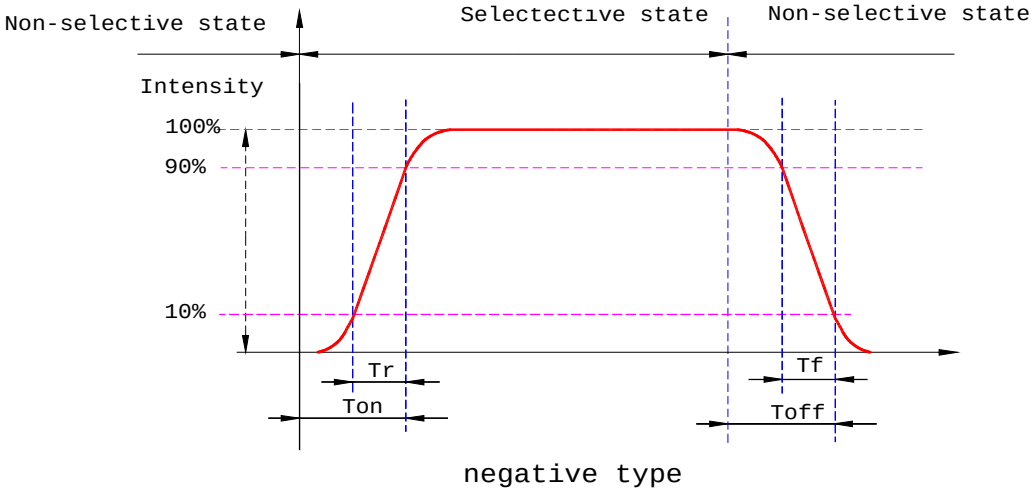


Fig.2-b

Note 3: Viewing Angle

A. The viewing angle is defined as shown below. (See Fig.3)

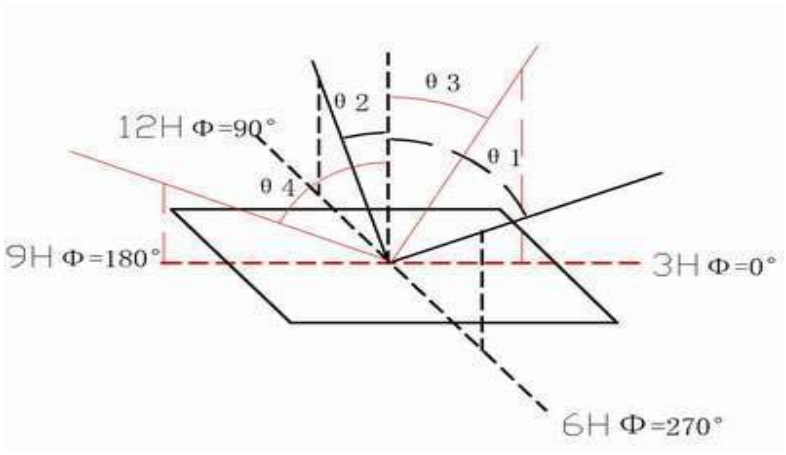


Fig.3

B. The system block diagram (See Fig.4)