ADNS-5030

Low Power Optical Mouse Sensor

Data Sheet

Description

The Avago Technologies ADNS-5030 is a low power, small form factor optical mouse sensor. It has a new low-power architecture and automatic power management modes, making it ideal for battery, power-sensitive applications – such as cordless input devices.

The ADNS-5030 is capable of high-speed motion detection – up to 14 ips and 2G. In addition, it has an on-chip oscillator and LED driver to minimize external components.

The ADNS-5030 along with the ADNS-5100/ADNS-5100-001 lens, ADNS-5200 clip, and HLMP-ED80 LED form a complete and compact mouse tracking system. There are no moving parts, which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through a four-wire serial port. It is housed in an 8-pin staggered dual in-line package (DIP).

Theory of Operation

The ADNS-5030 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-5030 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC.

Features

- Low power architecture
- Small form factor
- Self-adjusting power-saving modes for prolonging battery life
- High speed motion detection up to 14 ips and 2 G
- Self-adjusting frame rate for optimum performance
- Internal oscillator – no clock input needed
- Selectable 500 and 1000 cpi resolution
- Operating voltage: 3.3 V nominal
- Four wire serial port interface
- Minimal number of passive components

Applications

- Optical mice and optical trackballs
- Integrated input devices
- Battery-powered input devices

Pinout of ADNS-5030 Optical Mouse Sensor

Pin	Name	Description
1	MISO	Serial Data Output (Master In/Slave Out)
2	XY_LED	LED Control
3	NRESET	Reset Pin (active low input)
4	NCS	Chip Select (active low input)
5	SCLK	Serial Clock Input
6	GND	Ground
7	VDD3	Supply Voltage
8	MOSI	Serial Data Input (Master Out/Slave In)

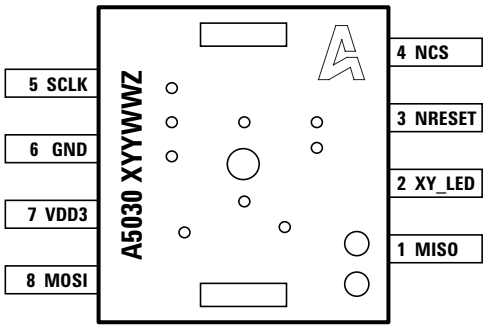
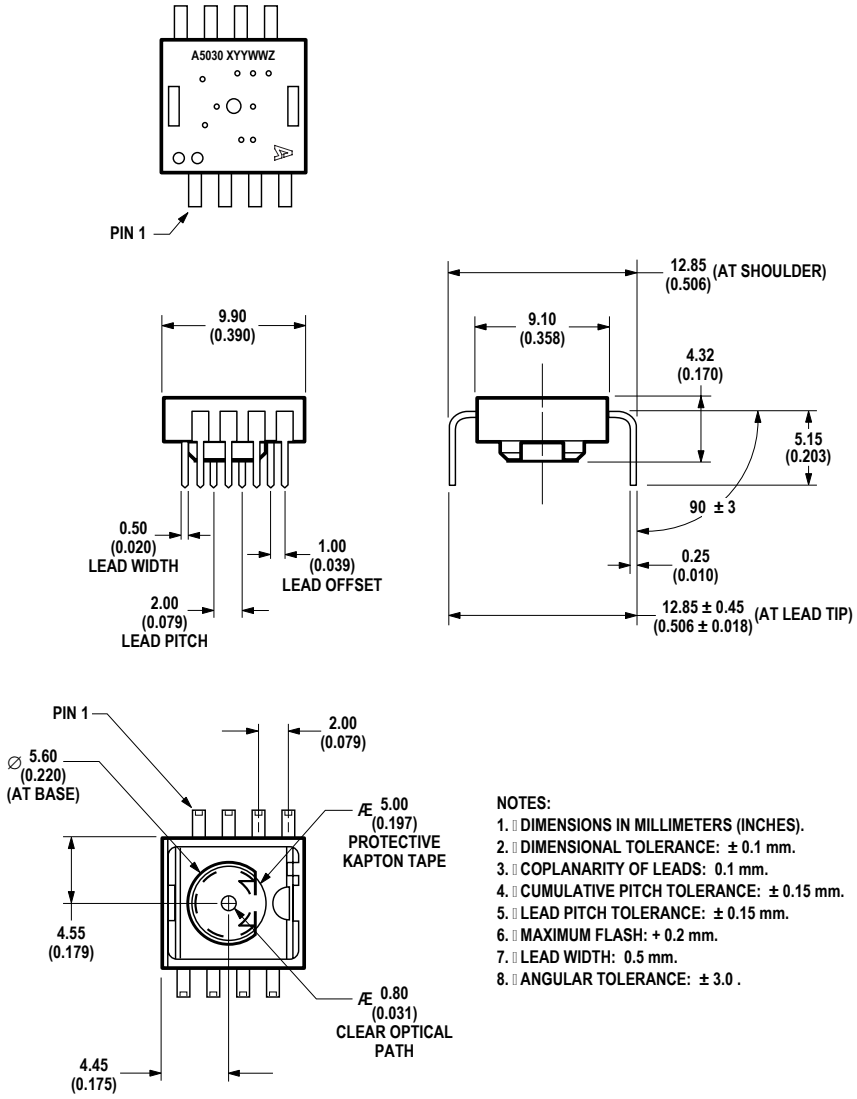


Figure 1. Package outline drawing (top view).



NOTES:
1. DIMENSIONS IN MILLIMETERS (INCHES).
2. DIMENSIONAL TOLERANCE: ± 0.1 mm.
3. COPLANARITY OF LEADS: 0.1 mm.
4. CUMULATIVE PITCH TOLERANCE: ± 0.15 mm.
5. LEAD PITCH TOLERANCE: ± 0.15 mm.
6. MAXIMUM FLASH: + 0.2 mm.
7. LEAD WIDTH: 0.5 mm.
8. ANGULAR TOLERANCE: ± 3.0 .

Figure 2. Package outline drawing.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The ADNS-5030 sensor is designed for mounting on a through-hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNS-5100/5100-001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED.

The ADNS-5200 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB.

The HLMP-ED80 LED is recommended for illumination.

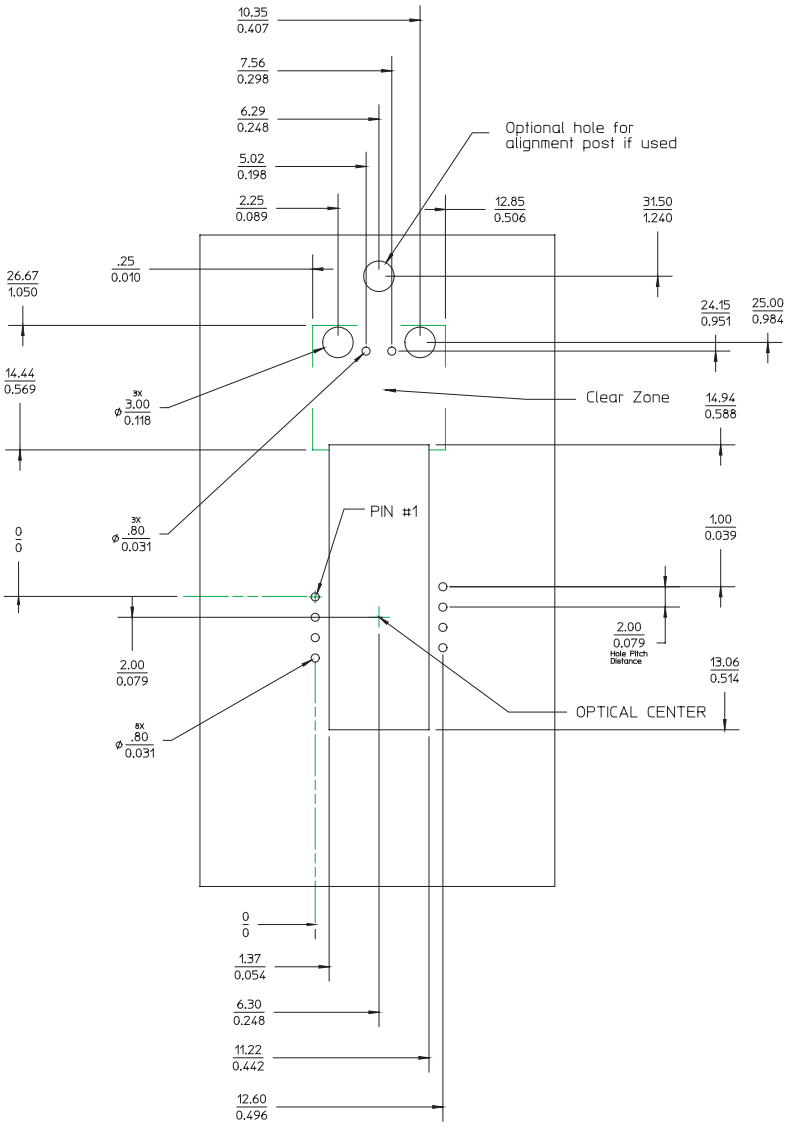


Figure 3. Recommended PCB mechanical cutouts and spacing.

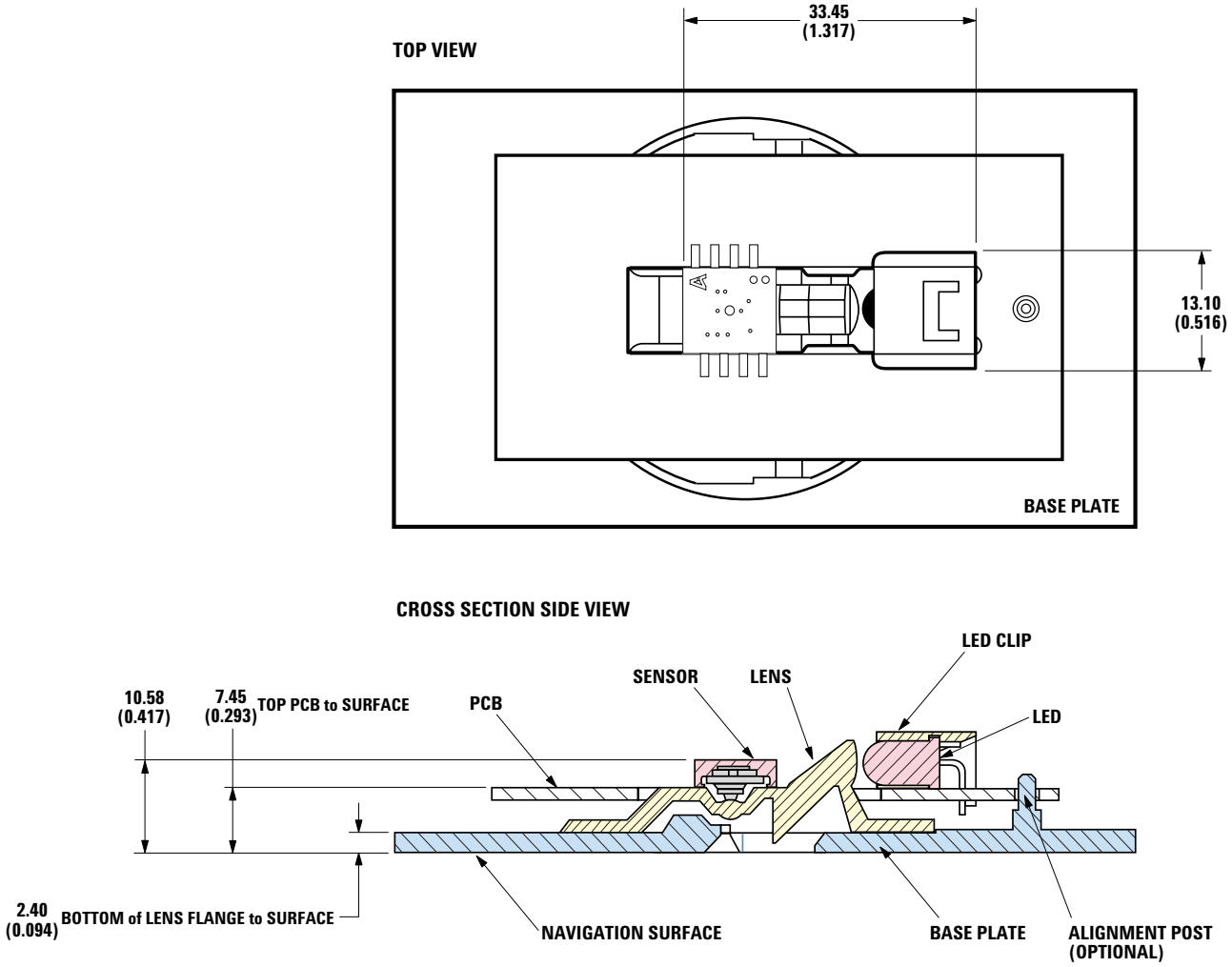


Figure 4. 2D Assembly drawing of ADNS-5030 (top and side view).

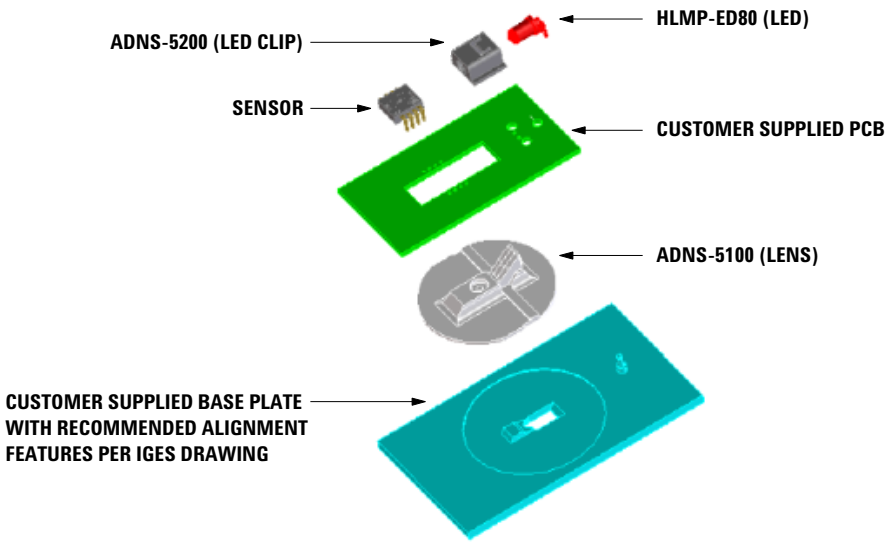


Figure 5. Exploded view drawing.

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED clip assembly into PCB.
4. Wave solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There MUST be a feature in the top case to press down onto the PCB assembly to ensure all components are interlocked to the correct vertical height.

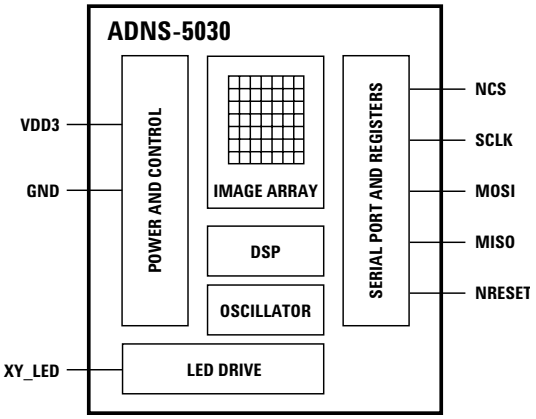


Figure 6. Block diagram of ADNS-5030 optical mouse sensor.

Design Considerations for Improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied IGES file and ADNS-5100/5100-001 lens.

Typical Distance	Millimeters
Creepage	16.0
Clearance	2.1

Note that the lens material is polycarbonate or polystyrene HH30, therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

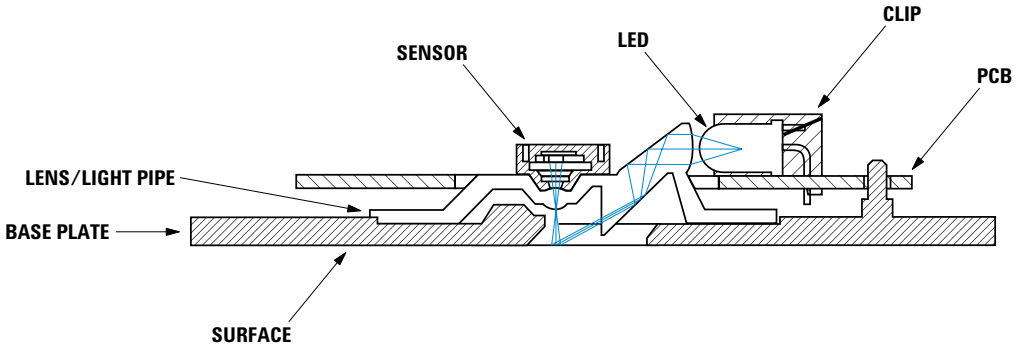


Figure 7. Sectional view of PCB assembly highlighting optical mouse components.

Recommended Typical Application (Receiver Side)

Recommended Typical Application (Transmitter Side)

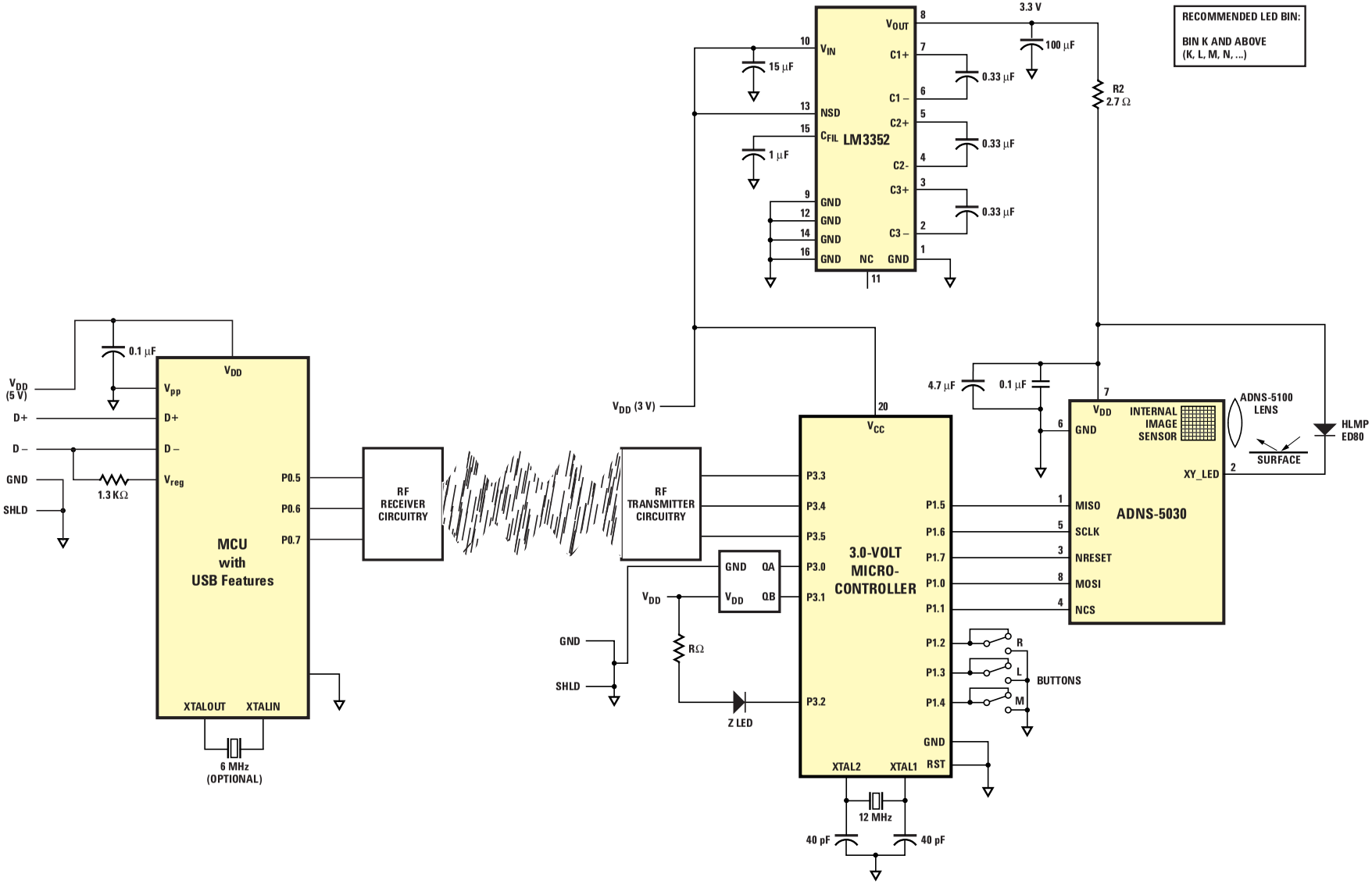


Figure 8. Schematic diagram for interface between ADNS-5030 and microcontroller (cordless application).

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15 kV when assembled into a mouse using ADNS-5100 round lens according to usage instructions above.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature			260	°C	
Supply Voltage	V_{DD}	-0.5	3.7	V	
ESD			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	All I/O pins
Output Current	Iout		7	mA	MISO pin

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply	V_{DD}	3.0	3.3	3.6	V	
Power Supply Rise Time	V_{RT}	0.005		100	ms	0 to V_{DD} min
Supply Noise (Sinusoidal)	V_{NA}			100	mVp-p	10 kHz - 50 MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface (Z)	Z	2.3	2.4	2.5	mm	
Speed	S	0		14	ips	
Acceleration	a			2	G	
Load Capacitance	C_{out}			100	pF	MISO

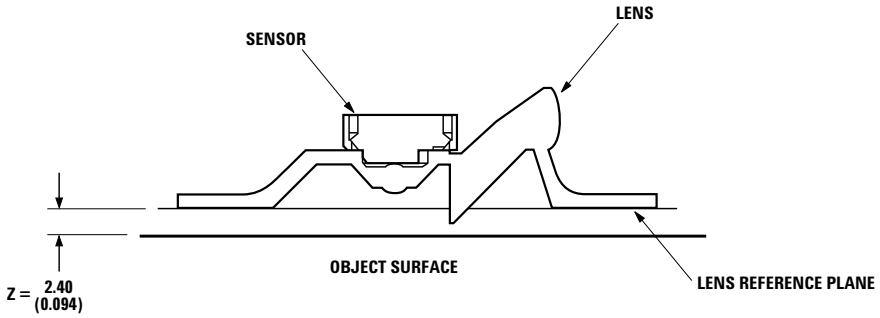


Figure 9. Distance from lens reference plane to tracking surface (Z).

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD} = 3.3 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Reset Pulse Width	t_{RESET}	250			ns	Active low
Motion Delay after Reset	$t_{MOT-RST}$			50	ms	From NRESET pull high to valid motion, assuming V_{DD} and motion is present
Forced Rest Enable	$t_{REST-EN}$			1	s	From Rest Mode(RM) bits set to target rest mode
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From Rest Mode(RM) bits cleared to valid motion
Power Down	t_{PD}			50	ms	From PD (when bit 1 of register 0x0d is set) to low current
Wake from Power Down	t_{WAKEUP}	50		55	ms	From PD inactive (when NRESET pin is asserted low to high or write 0x5a to register 0x3a) to valid motion
MISO Rise Time	t_{r-MISO}		40	200	ns	C_L = 100 pF
MISO Fall Time	t_{f-MISO}		40	200	ns	C_L = 100 pF
MISO Delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	0.5		$1/f_{SCLK}$	µs	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time between Write Commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte
SPI Time between Write and Read Commands	t_{SWR}	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte
SPI Time between Read and Subsequent Commands	t_{SRW} t_{SRR}	250			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the next address
SPI Read Address-Data Delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read
NCS Inactive after Motion Burst	t_{BEXIT}	250			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK Active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge
SCLK to NCS Inactive (for Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS Inactive (for Write Operation)	$t_{SCLK-NCS}$	20			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS-MISO}$			250	ns	From NCS rising edge to MISO high-Z state
Transient Supply Current	I_{DDT}			60	mA	Max supply current during a V_{DD} ramp from 0 to V_{DD}

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current in Various Mode	$I_{DD\_AVG\_HIGH}$		15.2	17	mA	Average current, including LED current, at max frame rate. No load on MISO. Bit 0 of register 0x40 set to "0"
	$I_{DD\_AVG\_LOW}$		11.3	13.1	mA	Average current, including LED current, at max frame rate. No load on MISO. Bit 0 of register 0x40 set to "1"
	I_{DD_REST1}		0.34	0.54	mA	
	I_{DD_REST2}		0.09	0.16	mA	
	I_{DD_REST3}		0.03	0.06	mA	
Power Down			2		uA	
Input Low Voltage	V_{IL}			0.5	V	SCLK, MOSI, NCS, NRESET
Input High Voltage	V_{IH}	V_{DD} – 0.5			V	SCLK, MOSI, NCS, NRESET
Input hysteresis	V_{I_HYS}		200		mV	SCLK, MOSI, NCS, NRESET
Input leakage current	I_{leak}		±1	±10	mA	Vin=VDD-0.6V, SCLK, MOSI, NCS, NRESET
Output Low Voltage	V_{OL}			0.7	V	Iout=1mA, MISO
Output High Voltage	V_{OH}	VDD -0.7			V	Iout=-1mA, MISO
Input Capacitance	C_{in}		50		pF	MOSI, NCS, SCLK, NRESET

Typical Performance Characteristics (Bit 0 of register 0x40 set to "0")

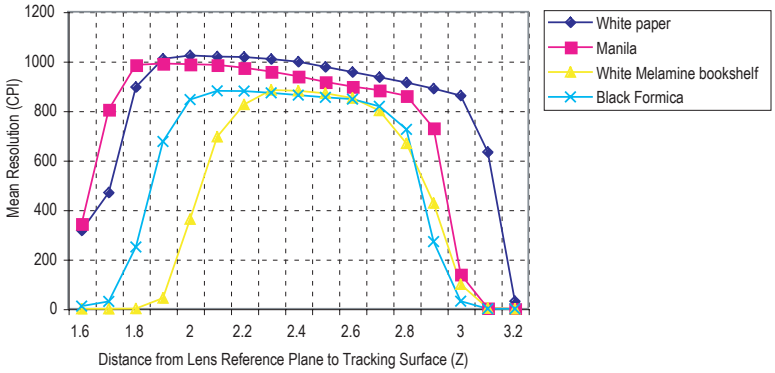


Figure 10. Mean resolution vs. distance from lens reference plane to surface.

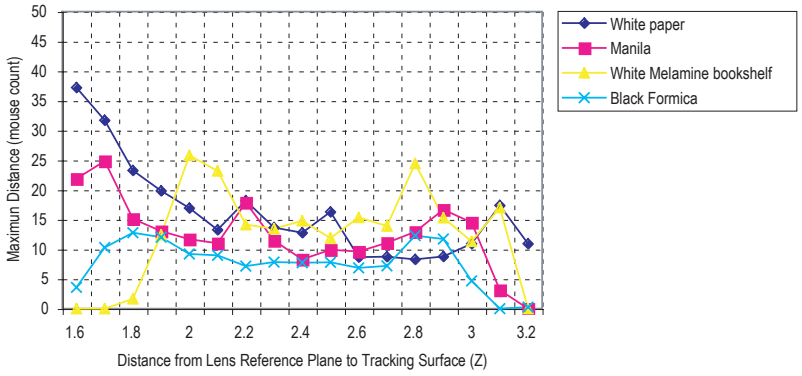


Figure 11. Typical path deviation.

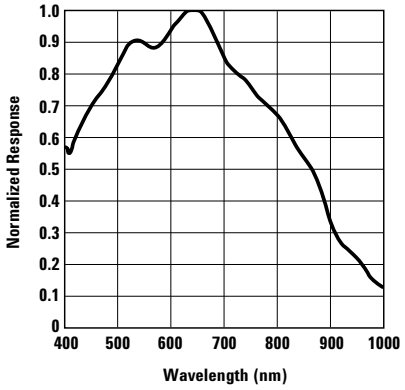


Figure 12. Relative wavelength responsivity.

Power Management Modes

The ADNS-5030 has three power-saving modes. Each mode has a different motion detection period, affecting response time to mouse motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (Typical)	Downshift Time (Typical)
Rest 1	14 ms	<1s
Rest 2	68 ms	7 s
Rest 3	340 ms	410 s

LED Mode

For power savings, the LED will not be continuously on. ADNS-5030 will pulse the LED only when needed.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-5030, and to read out the motion information.

The port is a four wire serial port. The host micro-controller always initiates communication; the ADNS-5030 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

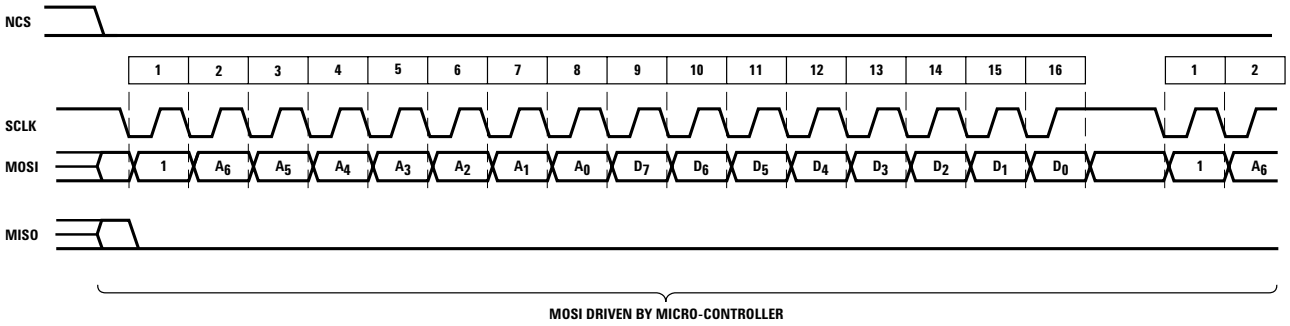
NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

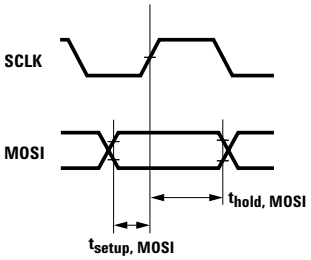
The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-5030, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-5030 reads MOSI on rising edges of SCLK.



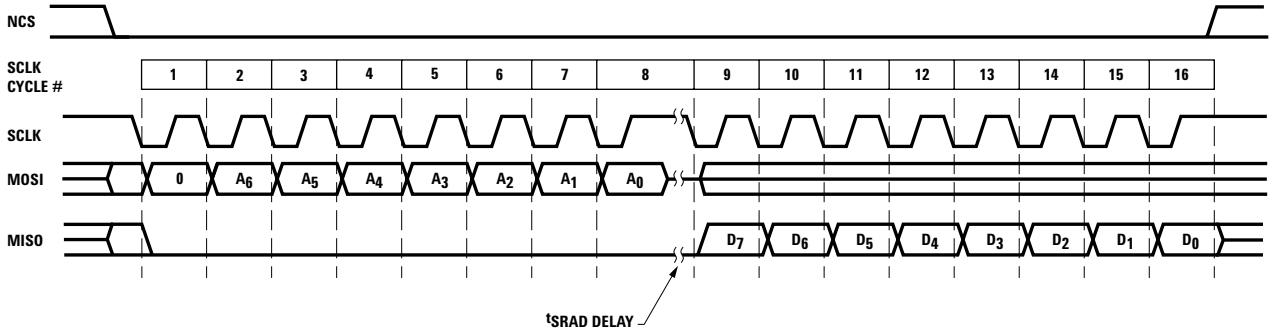
Write Operation



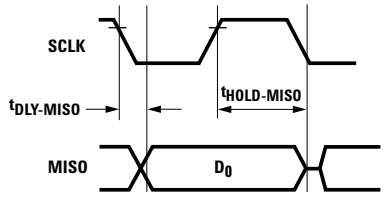
MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADNS-5030 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-5030 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.



Read Operation

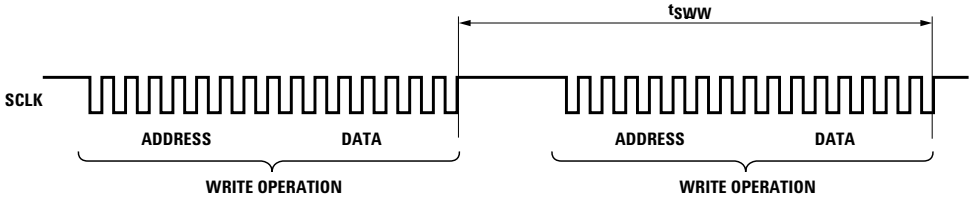


MISO Delay and Hold Time

NOTE: The 200 ns minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-5030. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-5030 will hold the state of data on MISO until the falling edge of SCLK.

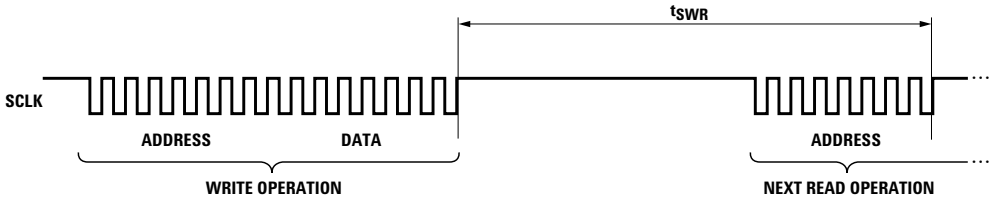
Required Timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.



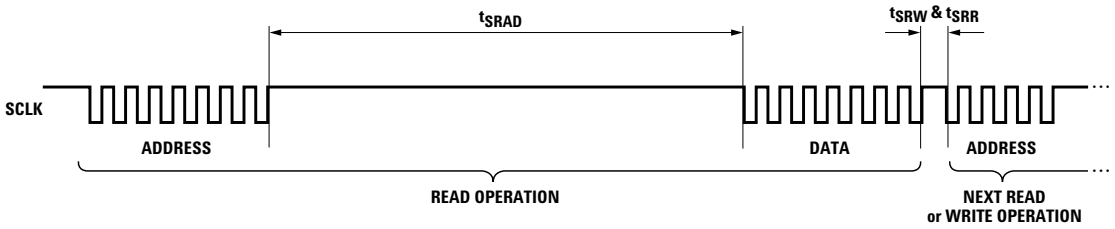
Timing between Two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.



Timing between Write and Read Commands

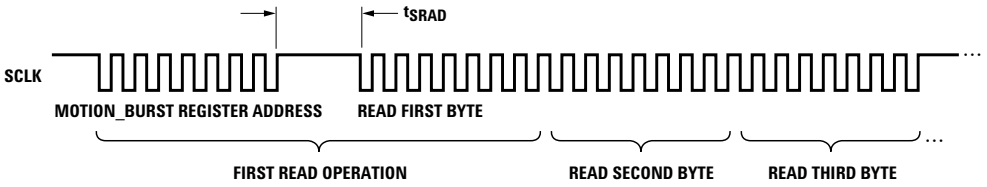
If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.



Timing between Read and Either Write or Subsequent Read Commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-5030 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Motion Burst Timing



Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion_Burst register. The ADNS-5030 will respond with the contents of the Delta_X, Delta_Y, SQUAL, Shutter_Upper, Shutter_Lower, and Maximum_Pixel and Pixel_Sum registers in that order. The burst transaction can be terminated anywhere in the sequence after the Delta_X value by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Avago Technologies highly recommends the usage of burst mode operation in optical mouse sensor design applications.

Notes on Power-up and Reset

The ADNS-5030 does not perform an internal power up self-reset; the NRESET pin must be asserted low every time power is applied. There are two ways to reset the chip, either assert low NRESET pin or by writing 0x5a to register 0x3a. A full reset will thus be executed. Any register settings must then be reloaded.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins after VDD is Valid

Pin	During Reset	After Reset
NCS	Ignored	Functional
MISO	Low	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
XY_LED	High	Functional

Notes on Power Down

The ADNS-5030 can be set in Power Down mode by setting bit 1 of Register 0x0d. In addition, the SPI port should not be accessed during power down. (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during power down. There are 2 ways to exit power down, either assert low NRESET pin or by writing 0x5a to Register 0x3a. A full reset will thus be executed. Wait t_{WAKEUP} before accessing the SPI port. Any register settings must then be reloaded.

Pin	Power Down Active
NRESET	Functional
NCS	Functional*
MISO	Undefined
SCLK	Functional*
MOSI	Functional*
XY_LED	Low current

* NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It can be in either state if the sensor is the only device in addition to the controller microprocessor.

Note: There is long wakeup time from power down. This feature should not be used for power management during normal mouse motion.

Registers

The ADNS-5030 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x11
0x01	Revision_ID	R	0x00
0x02	Motion	R	0x00
0x03	Delta_X	R	Any
0x04	Delta_Y	R	Any
0x05	SQUAL	R	Any
0x06	Shutter_Upper	R	Any
0x07	Shutter_Lower	R	Any
0x08	Maximum_Pixel	R	Any
0x09	Pixel_Sum	R	Any
0x0a	Minimum_Pixel	R	Any
0x0b	Pixel_Grab	R/W	Any
0x0c	Reserved		
0x0d	Mouse Control	R/W	0x00
0x0e – 0x39	Reserved		
0x3a	Chip_Reset	W	N/A
0x3b – 0x3e	Reserved		
0x3f	Inv_Rev_ID	R	0xff
0x40	Sensor_Current_Setting	W	N/A
0x41 – 0x44	Reserved		
0x45	Rest_mode_configuration	R/W	0x00
0x46 – 0x62	Reserved		
0x63	Motion_Burst	R	0x00

Product_ID Address: 0x00

Access: Read Reset Value: 0x11

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-5030. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID Address: 0x01

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-Bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

Motion Address: 0x02

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_X and Delta_Y registers.

Writing anything to this register clears the MOT bit, Delta_X and Delta_Y registers. The written data byte is not saved.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
Reserved	Reserved

Delta X Address: 0x03

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

Delta_Y Address: 0x04

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

Squal	Address: 0x05
Access: Read	Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8 bits of a 9-bit unsigned integer

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 144. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

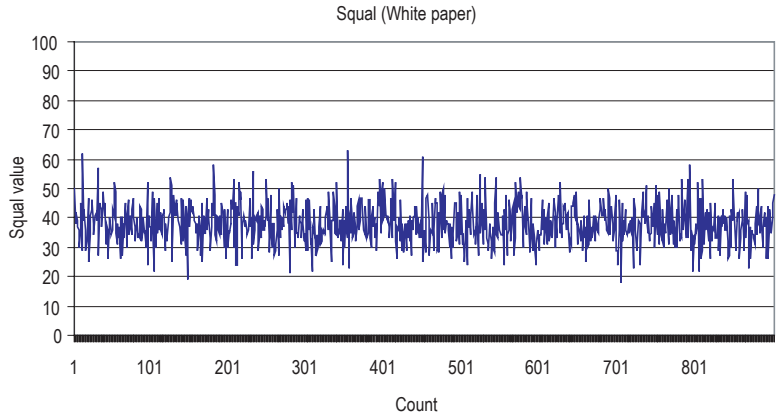


Figure 13. Squal values (white paper).

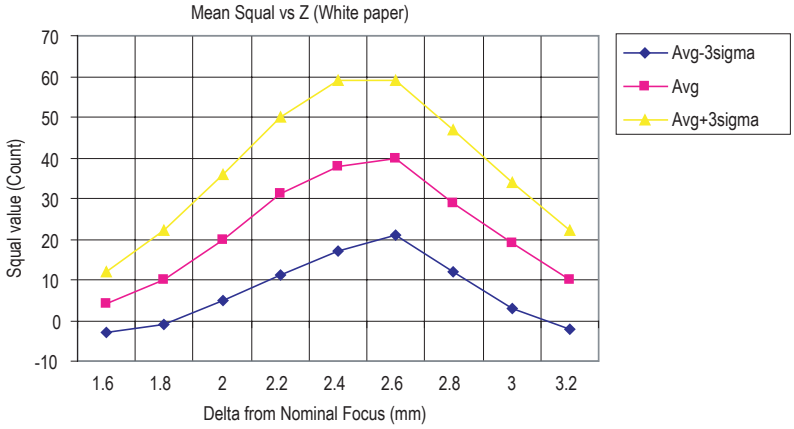


Figure 14. Mean squal vs. Z (white paper).

Shutter_Upper Address: 0x06
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower Address: 0x07
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type: Sixteen bit unsigned integer

USAGE: Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

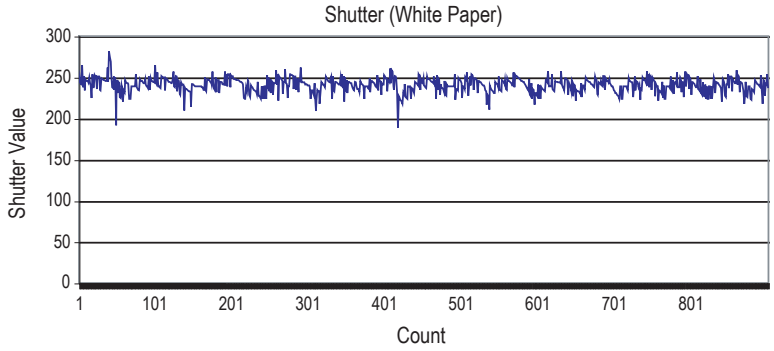


Figure 15. Shutter (white paper).

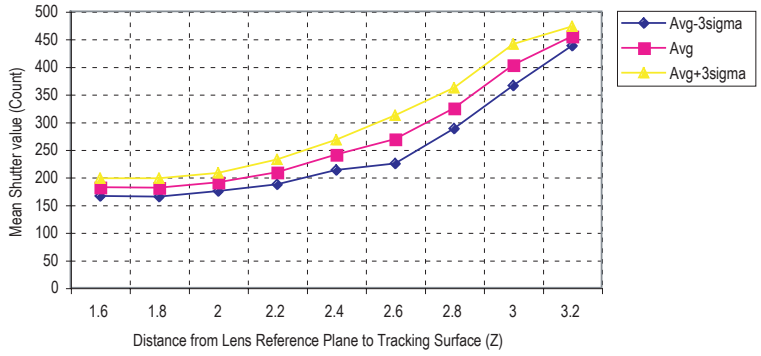


Figure 16. Mean shutter vs. Z (white paper).

Maximum_Pixel Address: 0x08

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_0	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 127. The maximum pixel value can vary with every frame.

Pixel_Sum Address: 0x09

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8 bits of an unsigned 15-bit integer

USAGE: This register is the accumulated pixel value from the last image taken. The maximum accumulator value is 28,575, but only bits [14:7] are reported. It may be described as the full sum divided by 1.76.

The maximum register value is 223. The minimum is 0. The pixel sum value can change on every frame.

Minimum_Pixel Address: 0x0a

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_0	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 127. The minimum pixel value can vary with every frame.

Pixel_Grab	Address: 0x0b
Access: Read/Write	Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Valid	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

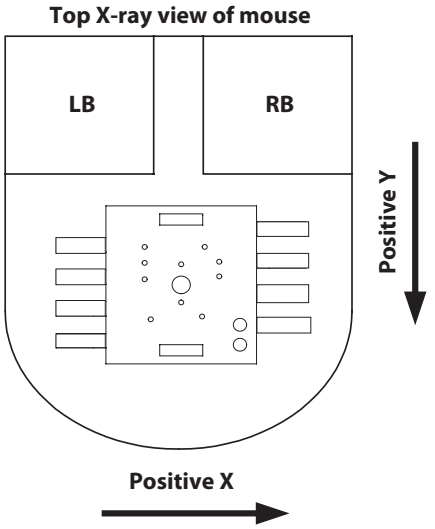
Data Type: Eight-bit word

USAGE: The pixel grabber captures 1 pixel per frame. If there is a valid pixel in the grabber when this register is read, the MSB will be set, an internal counter will incremented to capture the next pixel and the grabber will be armed to capture the next pixel. It will take 225 reads to upload the complete image.

Any write to this register will reset and arm the grabber to grab pixel 0 on the next image.

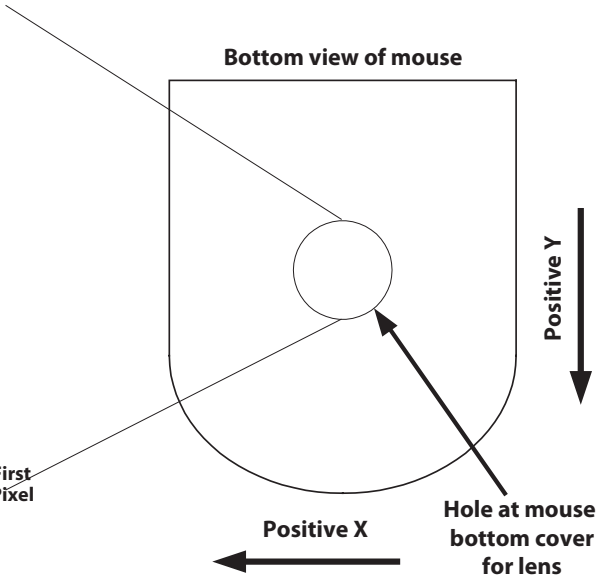
Physical Pixel Address Map – readout order of the array

(looking through the sensor aperture at the bottom of the package)



Last Pixel															
224	209	194	179	164	149	134	119	104	89	74	59	44	29	14
223	208	193	178	163	148	133	118	103	88	73	58	43	28	13
222	207	192	177	162	147	132	117	102	87	72	57	42	27	12
221	206	191	176	161	146	131	116	101	86	71	56	41	26	11
220	205	190	175	160	145	130	115	100	85	70	55	40	25	10
219	204	189	174	159	144	129	114	99	84	69	54	39	24	9
218	203	188	173	158	143	128	113	98	83	68	53	38	23	8
217	202	187	172	157	142	127	112	97	82	67	52	37	22	7
216	201	186	171	156	141	126	111	96	81	66	51	36	21	6
215	200	185	170	155	140	125	110	95	80	65	50	35	20	5
214	199	184	169	154	139	124	109	94	79	64	49	34	19	4
213	198	183	168	153	138	123	108	93	78	63	48	33	18	3
212	197	182	167	152	137	122	107	92	77	62	47	32	17	2
211	196	181	166	151	136	121	106	91	76	61	46	31	16	1
210	195	180	165	150	135	120	105	90	75	60	45	30	15	0

First Pixel



Reserved Address: 0x0c

Mouse_control Address: 0x0d

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PD	RES

Data Type: Eight bit number

USAGE: Mouse sensor resolution and power down settings can be accessed or to be edited by this register.

Field Name	Description
PD	Power Down **0 = normal** 1 = Power Down
RES	Set Resolution **0 = 500 cpi** 1 = 1000 cpi
Reserved	Reserved

Reserved Address: 0x0e-0x39

Chip_Reset Address: 0x3a

Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	CR_7	CR_6	CR_5	CR_4	CR_3	CR_2	CR_1	CR_0

Data Type: 8-Bit unsigned integer

USAGE: Write 0x5a to initiate chip RESET.

Reserved Address: 0x3b-0x3e

Inv_Rev_ID Address: 0x3f

Access: Read Reset Value: 0xff

Bit	7	6	5	4	3	2	1	0
Field	$RRID_7$	$RRID_6$	$RRID_5$	$RRID_4$	$RRID_3$	$RRID_2$	$RRID_1$	$RRID_0$

Data Type: Inverse 8-Bit unsigned integer

USAGE: This register contains the inverse of the revision ID which is located at register 0x01.

Sensor_Current_Setting Address: 0x40
Access: Write Reset Value: N/A

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDC

Data Type: 8-bit number

USAGE: This register is used to set the internal LED driver's drive strength.

Field Name	Description
LDC	Internal LED Driver Current **0 = High current** 1 = Low current
Reserved	Reserved

Reserved Address: 0x41-0x44

Rest_mode_configuration Address: 0x45
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RM_1	RM_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x45 allows the user to change or monitor the rest mode configuration of the sensor. Write operations to RM_1 and RM_0 forces the sensor into rest mode. Read RM_1 and RM_0 for the sensor to report which mode it is in.

Note: Forced Rest has a long wakeup time and should not be used for power management during normal mouse motion.

Field Name	Description
$RM_{[1-0]}$	Write operation: Force rest mode selection **00 = Normal operation** 01 = Rest1 10 = Rest2 11 = Rest3
$RM_{[1-0]}$	Read operation: Reports which mode the sensor is in. **00 = Run** 01 = Rest1 10 = Rest2 11 = Rest3
Reserved	Reserved

Reserved Address: 0x46-0x62

Motion_Burst Address: 0x63
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type: Various

USAGE: Read from this register to activate burst mode. The sensor will return the data in the Delta_X, Delta_Y, Squal, Shutter_Upper, Shutter_Lower, Maximum_Pixel and Pixel_Sum. If the burst is not terminated at this point, the internal address counter stops incrementing and Pixel Sum register's value will be continuously returned. Bursts are terminated when NCS is raised.

AV02-0113EN - July 30, 2007