AD7545

August 1997

12-Bit, Buffered, Multiplying CMOS DAC

Features

- **12-Bit Resolution**
- **Low Gain T.C. 2ppm/^{O}C (Typ)**
- **Fast TTL/CMOS Compatible Data Latches**
- **Single +5V to +15V Supply**
- **Low Power**
- **Low Cost**
- **/883 Processed Versions Available**

Ordering Information

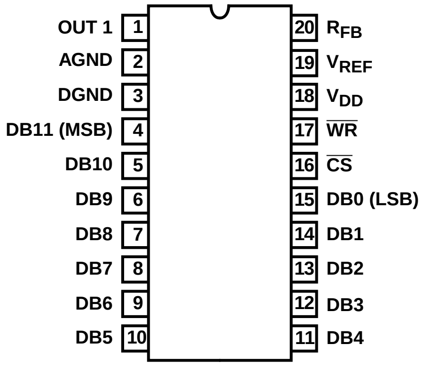
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
AD7545JN	0 to 70	20 Ld PDIP	E20.3
AD7545KN	0 to 70	20 Ld PDIP	E20.3
AD7545AN	-40 to 85	20 Ld PDIP	E20.3
AD7545BN	-40 to 85	20 Ld PDIP	E20.3

Description

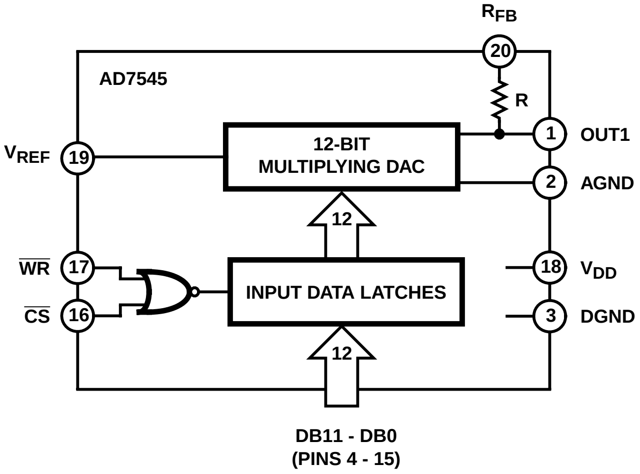
The AD7545 is a low cost monolithic 12-bit, CMOS multiplying DAC with on-board data latches. Data is loaded in a single 12-bit wide word which allows interfacing directly to most 12-bit and 16-bit bus systems. Loading of the input latches is under the control of the CS and WR inputs. A logic low on these control inputs makes the input latches transparent allowing direct unbuffered operation of the DAC.

Pinout

AD7545
(PDIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} to DGND)	-0.3V, +17V
Digital Input Voltage to DGND	-0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND	±25V
V_{PIN1} to DGND	-0.3V, V_{DD} +0.3V
AGND to DGND	-0.3V, V_{DD} +0.3V

Operating Conditions

Temperature Ranges	
Commercial (J, K, Grades)	0^oC to 70^oC
Industrial (A, B, Grades)	-40^oC to 85^oC
Extended (S Grades)	-55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	125
Maximum Junction Temperature (PDIP Package)	150^oC
Maximum Storage Temperature Range	-65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s)	300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = See Note 2, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	V_{DD} = +5V			V_{DD} = +15V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			12			12			Bits
Relative Accuracy	J, A, S		-	-	±2	-	-	±2	LSB
	K, B		-	-	±1	-	-	±1	LSB
Differential Nonlinearity	J, A, S	10-Bit Monotonic T_{MIN} to T_{MAX}	-	-	±4	-	-	±4	LSB
	K, B	12-Bit Monotonic T_{MIN} to T_{MAX}	-	-	±1	-	-	±1	LSB
Gain Error (Using Internal RFB)	J, A, S	DAC Register Loaded with 1111 1111 1111	-	-	±20	-	-	±25	LSB
	K, B	Gain Error is Adjustable Using the Circuits of Figures 4 and 5 (Note 3)	-	-	±10	-	-	±15	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature		Typical Value is $2ppm/^oC$ for V_{DD} = +5V (Note 4)	-	-	±5	-	-	±10	$ppm/^oC$
DC Supply Rejection ΔGain/ΔV_{DD}		ΔV_{DD} = ±5%	0.015	-	0.03	0.01	-	0.02	%
Output Leakage Current at OUT1	J, K	DB0 - DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V (Note 2)	-	-	50	-	-	50	nA
	A, B		-	-	50	-	-	50	nA
	S		-	-	200	-	-	200	nA
DYNAMIC CHARACTERISTICS									
Current Setting Time		To $^1/_2$ LSB, OUT1 LOAD = 100Ω, DAC Output Measured from Falling Edge of $\overline{WR}$, $\overline{CS}$ = 0V (Note 4)	-	-	2	-	-	2	µs
Propagation Delay from Digital Input Change to 90% of Final Analog Output		OUT1 LOAD = 100Ω, C_{EXT} = 13pF (Notes 4 and 5)	-	-	300	-	-	250	ns
Digital to Analog Glitch Impulse		V_{REF} = AGND	-	400	-	-	250	-	nV/s
AC Feedthrough at OUT1		V_{REF} = ±10V, 10kHz Sinewave (Note 6)	-	5	-	-	5	-	mV_{P-P}
ANALOG OUTPUTS									
Output Capacitance									
C_{OUT1}		DB0 - DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V (Note 4)	-	-	70	-	-	70	pF
C_{OUT1}		DB0 - DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V (Note 4)	-	-	200	-	-	200	pF

Electrical Specifications

T_A = See Note 2, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	V_{DD} = +5V			V_{DD} = +15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE INPUT								
Input Resistance (Pin 19 to GND)	Input Resistance TC = -300ppm/°C (Typ)	7	-	-	7	-	-	kΩ
	Typical Input Resistance = 11kΩ	-	-	25	-	-	25	kΩ
DIGITAL INPUTS								
Input High Voltage, V_{IH}		2.4	-	-	-	-	13.5	V
Input Low Voltage, V_{IL}		-	-	0.8	-	-	1.5	V
Input Current, I_{IN}	V_{IN} = 0 or V_{DD} (Note 7)	±1	-	±10	±1	-	±10	µA (Max)
Input Capacitance								
DB0 - DB11	V_{IN} = 0 (Note 4)	-	-	7	-	-	7	pF
$\overline{WR}$, $\overline{CS}$	V_{IN} = 0 (Note 4)	-	-	20	-	-	20	pF
SWITCHING CHARACTERISTICS (Note 4)								
Chip Select to Write Setup Time, t_{CS}	See Figure 1	380	200	-	200	120	-	ns
Chip Select to Write Hold Time, t_{CH}	See Figure 1	0	-	-	0	-	-	ns
Write Pulse Width, t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$, See Figure 1	400	175	-	240	100		ns
Data Setup Time, t_{DS}	See Figure 1	210	100	-	120	60	-	ns
Data Hold Time, t_{DH}	See Figure 1	10	-	-	10	-	-	ns
POWER SUPPLY CHARACTERISTICS								
I_{DD}	All Digital Inputs V_{IL} or V_{IH}	-	-	2	-	-	2	mA
	All Digital Inputs 0V or V_{DD}	-	100	500	-	100	500	µA
	All Digital Inputs 0V or V_{DD}	-	10	-	-	10	-	µA

NOTES:

2. Temperature Ranges as follows: J, K versions: 0°C to 70°C
   A, B versions: -20°C to 85°C
   S version: -55°C to 125°C
   T_A = 25°C for TYP Specifications. MIN and MAX are measured over the specified operating range.
3. This includes the effect of 5ppm maximum gain TC.
4. Parameter not tested. Parameter guaranteed by design, simulation, or characterization.
5. DB0 - DB11 = 0V to V_{DD} or V_{DD} to 0V in plastic and sidebraze package.
6. Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
7. Logic inputs are MOS gates. Typical input current (25°C) is less than 1nA.
8. Typical values are not guaranteed but reflect mean performance specification.
   Specifications subject to change without notice.

Timing Diagrams

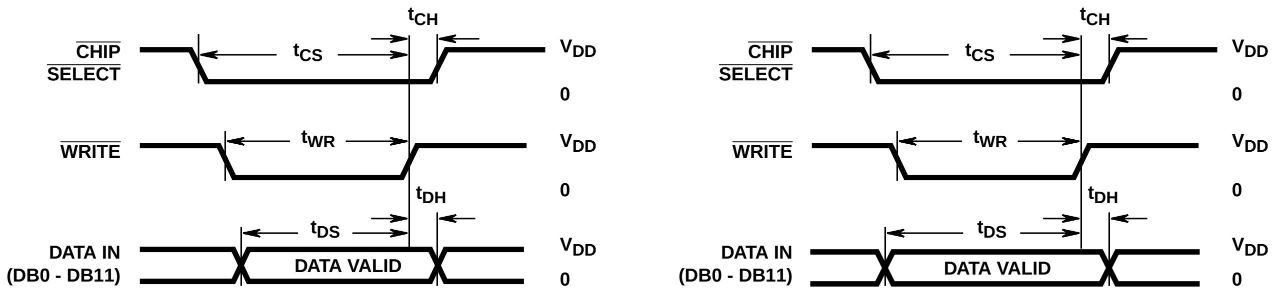


FIGURE 1A. TYPICAL WRITE CYCLE

FIGURE 1B. PREFERRED WRITE CYCLE

FIGURE 1. WRITE CYCLE TIMING DIAGRAM

MODE SELECTION	
WRITE MODE: $\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0 - DB11) inputs	HOLD MODE: Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0 - DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:

9. V_{DD} = +5V; $t_r = t_f$ = 20ns
10. V_{DD} = +15V; $t_r = t_f$ = 40ns
11. All input signal rise and fall times measured from 10% to 90% of V_{DD}.
12. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.
13. Since input data latches are transparent for $\overline{CS}$ and $\overline{WR}$ both low, it is preferred to have data valid before $\overline{CS}$ and $\overline{WR}$ both go low. This prevents undesirable changes at the analog output while the data inputs settle.

Circuit Information - D/A Converter Section

Figure 2 shows a simplified circuit of the D/A converter section of the AD7545. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

The binary weighted currents are switched between the OUT1 bus line and AGND by N-Channel switches, thus maintaining a constant current in each ladder leg independent of the switch state. One of the current switches is shown in Figure 3.

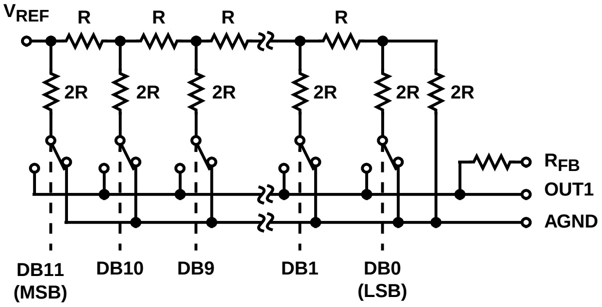


FIGURE 2. SIMPLIFIED D/A CIRCUIT OF AD7545

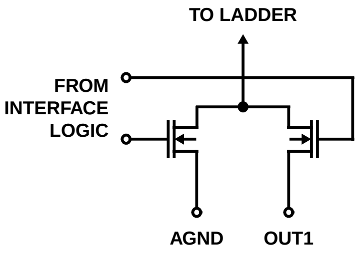


FIGURE 3. N-CHANNEL CURRENT STEERING SWITCH

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to the value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor).

Circuit Information - Digital Section

Figure 4 shows the digital structure for one bit. The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

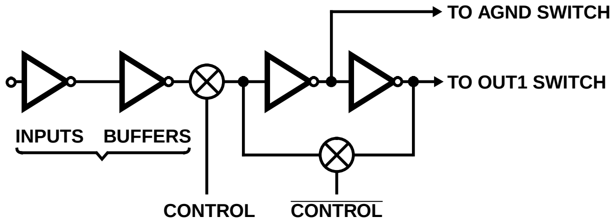


FIGURE 4. DIGITAL INPUT STRUCTURE

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0V to 3.5V the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range 5V $\leq V_{DD} \leq$ 15V. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

Application

Output Offset

CMOS current-steering D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation.

General Ground Management

AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND connection is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches

When $\overline{WR}$ and $\overline{CS}$ are both low the latched are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse ($\overline{WR}$) so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by isolating the analog pins of the AD7545 (pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid isolation at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5V. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induces noise.

Temperature Coefficients

The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/^{o}C and a typical value of 2ppm/^{o}C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100^{o}C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account.

Basic Applications

Figures 5 and 6 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that the circuits of Figures 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0V to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an AC signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20V \le V_{IN} \le +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 4.

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

The choice of the operational amplifiers in Figure 4 and Figure 5 depends on the application and the trade off between required precision and speed. Below is a list of operational amplifiers which are good candidates for many applications. The main selection criteria for these operational amplifiers is to have low V_{OS}, low V_{OS} drift, low bias current and low settling time.

These amplifiers need to maintain the low nonlinearity and monotonic operation of the D/A while providing enough speed for maximum converter performance.

Operational Amplifiers

HA5127	Ultra Low Noise, Precision
HA5137	Ultra Low Noise, Precision, Wide Band
HA5147	Ultra Low Noise, Precision, High Slew Rate
HA5170	Precision, JFET Input

TABLE 1. RECOMMENDED TRIM RESISTOR VALUES vs GRADES FOR V_{DD} = +5V

TRIM RESISTOR	J, A, S	K, B
R1	500Ω	200Ω
R2	150Ω	68Ω

TABLE 2. UNIPOLAR BINARY CODE TABLE FOR CIRCUIT OF FIGURE 4

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -\frac{1}{2}V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0V

TABLE 3. 2'S COMPLEMENT CODE TABLE FOR CIRCUIT OF FIGURE 5

DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \bullet \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \bullet \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0V
1111	1111	1111	$-V_{IN} \bullet \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \bullet \left\{\frac{2048}{2048}\right\}$

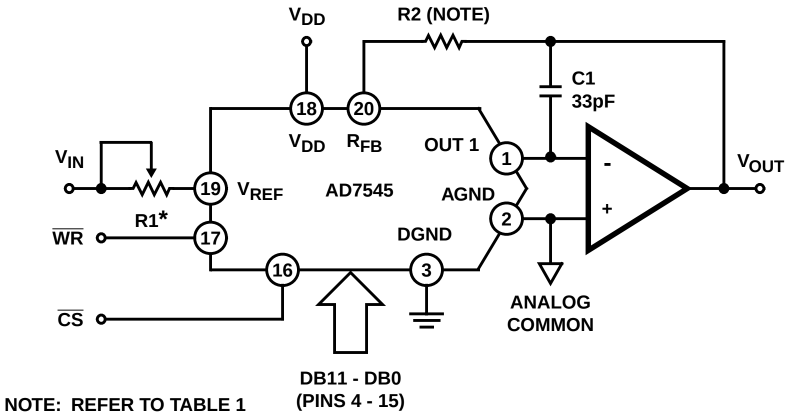


FIGURE 5. UNIPOLAR BINARY OPERATION

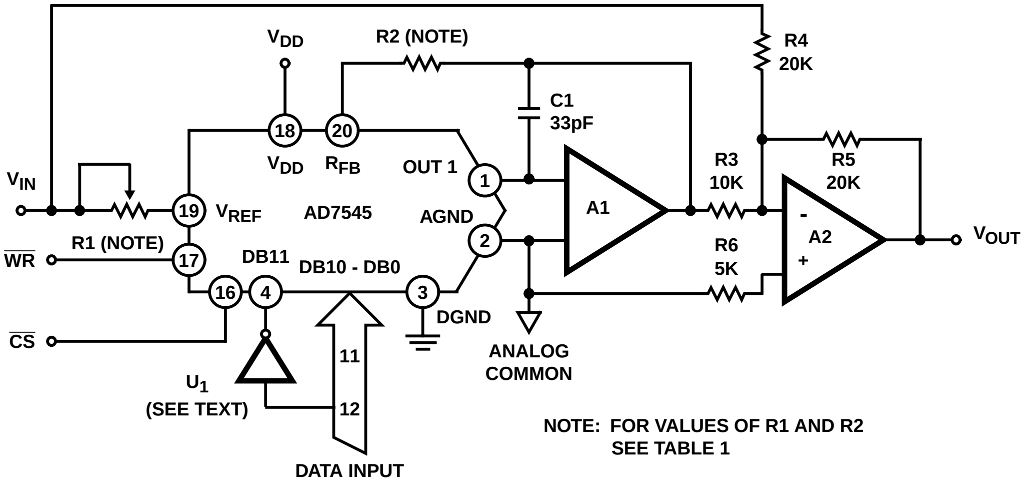


FIGURE 6. BIPOLAR OPERATION (2'S COMPLEMENT CODE)

Die Characteristics

DIE DIMENSIONS:

121 mils x 123 mils (3073micrms x 3124micrms)

METALLIZATION:

Type: Pure Aluminum
Thickness: 10 ±1kÅ

PASSIVATION:

Type: PSG/Nitride
PSG: 7 ±1.4kÅ
Nitride: 8 ±1.2kÅ

PROCESS:

CMOS Metal Gate

Metallization Mask Layout

AD7545