14-Bit, 80 MSPS A/D Converter

AD6645

FEATURES
80 MSPS Guaranteed Sample Rate
SNR = 75 dB, f_{IN} 15 MHz @ 80 MSPS
SNR = 72 dB, f_{IN} 200 MHz @ 80 MSPS
SFDR = 89 dBc, f_{IN} 70 MHz @ 80 MSPS
100 dB Multitone SFDR
IF Sampling to 200 MHz
Sampling Jitter 0.1 ps
1.5 W Power Dissipation
Differential Analog Inputs
Pin-Compatible to AD6644
Two's Complement Digital Output Format
3.3 V CMOS-Compatible
DataReady for Output Latching

APPLICATIONS
Multichannel, Multimode Receivers
Base Station Infrastructure
AMPS, IS-136, CDMA, GSM, WCDMA
Single Channel Digital Receivers
Antenna Array Processing
Communications Instrumentation
Radar, Infrared Imaging
Instrumentation

PRODUCT DESCRIPTION

The AD6645 is a high-speed, high-performance, monolithic 14-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution. The AD6645 provides CMOS-compatible digital outputs. It is the fourth generation in a wideband ADC family, preceded by the AD9042 (12-bit, 41 MSPS), the AD6640 (12-bit, 65 MSPS, IF sampling), and the AD6644 (14-bit, 40 MSPS/65 MSPS).

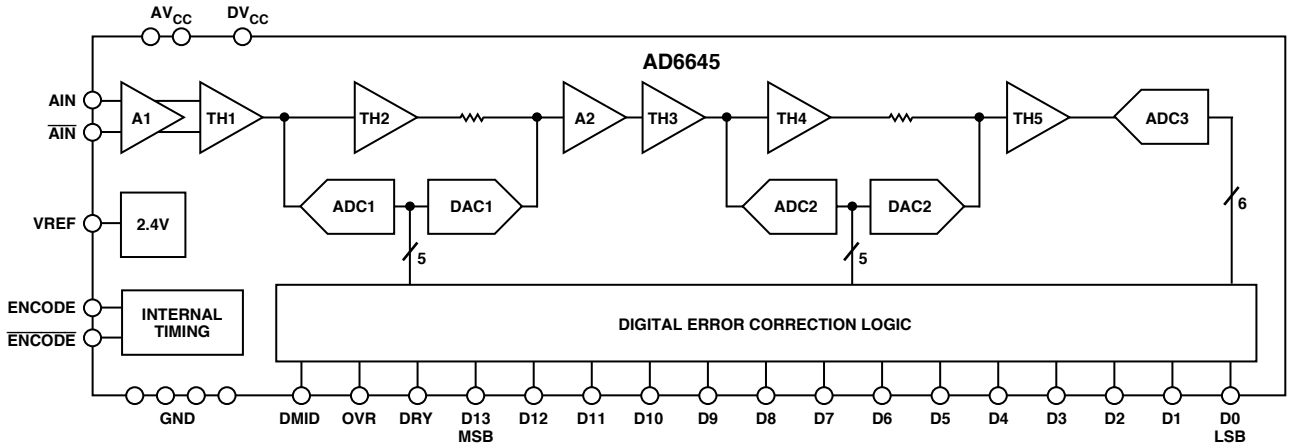
Designed for multichannel, multimode receivers, the AD6645 is part of Analog Device's SoftCell™ transceiver chipset. The AD6645 maintains 100 dB multitone, spurious-free dynamic range (SFDR) through the second Nyquist band. This breakthrough performance eases the burden placed on multimode digital receivers (software radios) that are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74.5 dB through the first Nyquist band.

The AD6645 is built on Analog Devices' high-speed complementary bipolar process (XFCB) and uses an innovative, multipass circuit architecture. Units are available in a thermally enhanced 52-lead PowerQuad 4® (LQFP_ED) specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. IF Sampling
   The AD6645 maintains outstanding ac performance up to input frequencies of 200 MHz. Suitable for multicarrier 3G wideband cellular IF sampling receivers.
2. Pin Compatibility
   The ADC has the same footprint and pin layout as the AD6644, 14-Bit 40 MSPS/65 MSPS ADC.
3. SFDR Performance and Oversampling
   Multitone SFDR performance of –100 dBc can reduce the requirements of high-end RF components and allows the use of receive signal processors such as the AD6620 or AD6624/AD6624A.

FUNCTIONAL BLOCK DIAGRAM



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PowerQuad 4 is a registered trademark of Amkor Technology, Inc.

REV. 0

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AD6645–SPECIFICATIONS

DC SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter	Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
RESOLUTION				14		Bits
ACCURACY						
No Missing Codes	Full	II		Guaranteed		
Offset Error	Full	II	–10	+1.2	+10	mV
Gain Error	Full	II	–10	0	+10	% FS
Differential Nonlinearity (DNL)	Full	II	–1.0	±0.25	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		±0.5		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		1.5		ppm/°C
Gain Error	Full	V		48		ppm/°C
POWER SUPPLY REJECTION (PSRR)	25°C	V		±1.0		mV/V
REFERENCE OUT (VREF)[1]	Full	V		2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)						
Differential Input Voltage Range	Full	V		2.2		V p-p
Differential Input Resistance	Full	V		1		kΩ
Differential Input Capacitance	25°C	V		1.5		pF
POWER SUPPLY						
Supply Voltages						
AV_{CC}	Full	II	4.75	5.0	5.25	V
DV_{CC}	Full	II	3.0	3.3	3.6	V
Supply Current						
I AV_{CC} (AV_{CC} = 5.0 V)	Full	II		275	320	mA
I DV_{CC} (DV_{CC} = 3.3 V)	Full	II		32	45	mA
Rise Time[2]						
AV_{CC}	Full	IV			TBD	ms
POWER CONSUMPTION	Full	II		1.5	1.75	W

NOTES
[1]VREF is provided for setting the common-mode offset of a differential amplifier such as the AD8138 when a dc-coupled analog input is required. VREF should be buffered if used to drive additional circuit functions.
[2]Specified for dc supplies with linear rise-time characteristics. The use of dc supplies with linear rise-times of <45 ms is highly recommended.

Specifications subject to change without notice

DIGITAL SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter (Conditions)	Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
ENCODE INPUTS (ENC, $\overline{ENC}$)						
Differential Input Voltage[1]	Full	IV	0.4			V p-p
Differential Input Resistance	25°C	V		10		kΩ
Differential Input Capacitance	25°C	V		2.5		pF
LOGIC OUTPUTS (D13–D0, DRY, OVR[2])						
Logic Compatibility				CMOS		
Logic "1" Voltage (DV_{CC} = 3.3 V)[3]	Full	II	2.85	DV_{CC} – 0.2		V
Logic "0" Voltage (DV_{CC} = 3.3 V)[3]	Full	II		0.2	0.5	V
Output Coding				Two's Complement		
DMID	Full	V		DV_{CC}/2		V

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]The functionality of the Over-Range bit is specified for a temperature range of 25°C to 85°C only.
[3]Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF will degrade performance.

Specifications subject to change without notice.

AC SPECIFICATIONS[1] (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{ENCODE}$ = 80 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter (Conditions)		Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
SNR							
Analog Input	15.5 MHz	25°C	V		75.0		dB
@ –1 dBFS	30.5 MHz	25°C	II	72.5	74.5		dB
	70.0 MHz	25°C	II	72.0	73.5		dB
	150.0 MHz	25°C	V		73.0		dB
	200.0 MHz	25°C	V		72.0		dB
SINAD							
Analog Input	15.5 MHz	25°C	V		75.0		dB
@ –1 dBFS	30.5 MHz	25°C	II	72.5	74.5		dB
	70.0 MHz	25°C	V		73.0		dB
	150.0 MHz	25°C	V		68.5		dB
	200.0 MHz	25°C	V		62.5		dB
WORST HARMONIC (2^{nd} or 3^{rd})							
Analog Input	15.5 MHz	25°C	V		93.0		dBc
@ –1 dBFS	30.5 MHz	25°C	II	85.0	93.0		dBc
	70.0 MHz	25°C	V		89.0		dBc
	150.0 MHz	25°C	V		70.0		dBc
	200.0 MHz	25°C	V		63.5		dBc
WORST HARMONIC (4^{th} or HIGHER)							
Analog Input	15.5 MHz	25°C	V		96.0		dBc
@ –1 dBFS	30.5 MHz	25°C	II	85.0	95.0		dBc
	70.0 MHz	25°C	V		90.0		dBc
	150.0 MHz	25°C	V		90.0		dBc
	200.0 MHz	25°C	V		88.0		dBc
TWO TONE SFDR @	30.5 MHz[2, 3]	25°C	V		100		dBFS
	55.0 MHz[2, 4]	25°C	V		100		dBFS
TWO TONE IMD REJECTION[3, 4]							
F1, F2 @ –7 dBFS		25°C	V		90		dBc
ANALOG INPUT BANDWIDTH		25°C	V		270		MHz

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]Analog input signal power swept from –10 dBFS to –100 dBFS.
[3]F1 = 30.5 MHz, F2 = 31.5 MHz.
[4]F1 = 55.25 MHz, F2 = 56.25 MHz.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{ENCODE}$ = 80 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter (Conditions)	Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
Maximum Conversion Rate	Full	II	80			MSPS
Minimum Conversion Rate	Full	IV			30	MSPS
ENCODE Pulsewidth High (t_{ENCH})*	Full	IV	5.625			ns
ENCODE Pulsewidth Low (t_{ENCL})*	Full	IV	5.625			ns

*Several timing parameters are a function of t_{ENCL} and t_{ENCH}.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (continued)

(AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{\text{ENCODE}}$ = 80 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C, C_{LOAD} = 10 pF, unless otherwise noted.)

Parameter (Conditions)	Name	Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
ENCODE Input Parameters[1]							
Encode Period[1] @ 80 MSPS	t_{ENC}	Full	V		12.5		ns
Encode Pulsewidth High[2] @ 80 MSPS	t_{ENCH}	Full	V		6.25		ns
Encode Pulsewidth Low @ 80 MSPS	t_{ENCL}	Full	V		6.25		ns
ENCODE/DataReady							
Encode Rising to DataReady Falling	t_{DR}	Full	V	1.0	2.0	3.1	ns
Encode Rising to DataReady Rising	t_{E_DR}	Full	V		$t_{ENCH} + t_{DR}$		ns
@ 80 MSPS (50% Duty Cycle)		Full	V	7.3	8.3	9.4	ns
ENCODE/DATA (D13:0), OVR							
ENC to DATA Falling Low	t_{E_FL}	Full	V	2.4	4.7	7.0	ns
ENC to DATA Rising Low	t_{E_RL}	Full	V	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Hold Time)[3]	t_{H_E}	Full	V	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Setup Time)[4]	t_{S_E}	Full	V		$t_{ENC} - t_{E\_FL}$		ns
Encode = 80 MSPS (50% Duty Cycle)		Full	V	5.3	7.6	10.0	ns
DataReady (DRY[5])/DATA, OVR							
DataReady to DATA Delay (Hold Time)[2]	t_{H_DR}	Full	V		Note 6		ns
Encode = 80 MSPS (50% Duty Cycle)				6.6	7.2	7.9	
DataReady to DATA Delay (Setup Time)[2]	t_{S_DR}	Full	V		Note 6		ns
Encode = 80 MSPS (50% Duty Cycle)				2.1	3.6	5.1	
APERTURE DELAY	t_A	25°C	V		–500		ps
APERTURE UNCERTAINTY (Jitter)	t_J	25°C	V		0.1		ps rms

NOTES

[1]Several timing parameters are a function of t_{ENC} and t_{ENCH}.

[2]To compensate for a change in duty cycle for t_{H_DR} and t_{S_DR} use the following equation:

$Newt_{H\_DR} = (t_{H\_DR} - \%\ Change(t_{ENCH}))$

$Newt_{S\_DR} = (t_{S\_DR} - \%\ Change(t_{ENCH}))$

[3]ENCODE TO DATA Delay (Hold Time) is the absolute minimum propagation delay through the Analog-to-Digital Converter, $t_{E\_RL} = t_{H\_E}$.

[4]ENCODE TO DATA Delay (Setup Time) is calculated relative to 80 MSPS (50% duty cycle). To calculate t_{S_E} for a given encode, use the following equation:

$Newt_{S\_E} = t_{ENC(NEW)} - t_{ENC} + t_{S\_E}$ (i.e., for 40 MSPS: $Newt_{S\_E(TYP)} = 25 \times 10^{-9} - 15.38 \times 10^{-9} + 9.8 \times 10^{-9} = 19.4 \times 10^{-9}$).

[5]DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock will correspondingly change the duty cycle of DRY.

[6]DataReady to DATA Delay (t_{H_DR} and t_{S_DR}) is calculated relative to 80 MSPS (50% duty cycle) and is dependent on t_{ENC} and duty cycle. To calculate t_{H_DR} and t_{S_DR} for a given encode, use the following equations:

$Newt_{H\_DR} = t_{ENC(NEW)}/2 - t_{ENCH} + t_{H\_DR}$ (i.e., for 40 MSPS: $Newt_{H\_DR(TYP)} = 12.5 \times 10^{-9} - 6.25 \times 10^{-9} + 7.2 \times 10^{-9} = 13.45 \times 10^{-9}$

$Newt_{S\_DR} = t_{ENC(NEW)}/2 - t_{ENCH} + t_{S\_DR}$ (i.e., for 40 MSPS: $Newt_{S\_DR(TYP)} = 12.5 \times 10^{-9} - 6.25 \times 10^{-9} + 3.6 \times 10^{-9} = 9.85 \times 10^{-9}$

Specifications subject to change without notice.

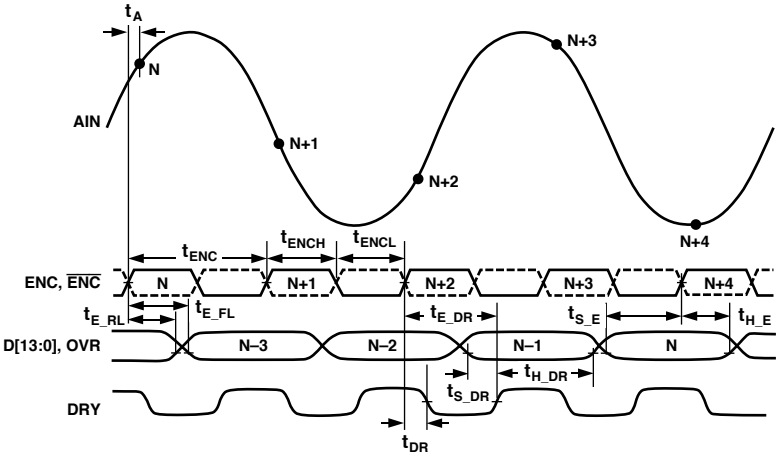


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
ELECTRICAL			
AV_{CC} Voltage	0	7	V
DV_{CC} Voltage	0	7	V
Analog Input Voltage	0	AV_{CC}	V
Analog Input Current		25	mA
Digital Input Voltage	0	AV_{CC}	V
Digital Output Current		4	mA
ENVIRONMENTAL			
Operating Temperature Range (Ambient)	–40	+85	°C
Maximum Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec)		300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

*Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

THERMAL CHARACTERISTICS

52-Lead PowerQuad 4 . . . . . LQFP_ED
θ_{JA} = 23°C/W . . . . . Soldered Slug, No Airflow
θ_{JA} = 17°C/W . . . . . Soldered Slug, 200 LFPM Airflow
θ_{JA} = 30°C/W . . . . . Unsoldered Slug, No Airflow
θ_{JA} = 24°C/W . . . . . Unsoldered Slug, 200 LFPM Airflow
θ_{JC} = 2°C/W . . . . . Bottom of Package (Heatslug)

Typical Four-Layer JEDEC Board Horizontal Orientation

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.
II. 100% production tested at 25°C and guaranteed by design and characterization at temperature extremes.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.

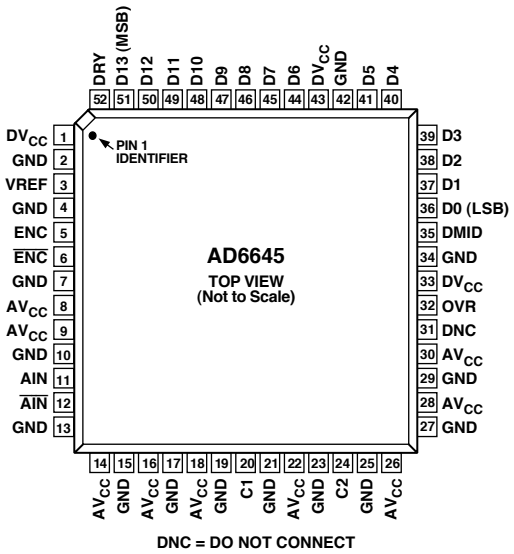
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6645ASQ-80	–40°C to +85°C (Ambient)	52-Lead PowerQuad 4 (LQFP_ED)	SQ-52
AD6645/PCB	25°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6645 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



DNC = DO NOT CONNECT

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 33, 43	DV_{CC}	3.3 V Power Supply (Digital) Output Stage Only
2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	GND	Ground
3	VREF	2.4 V Reference. Bypass to ground with a 0.1 µF microwave chip capacitor.
5	ENC	Encode Input. Conversion initiated on rising edge.
6	$\overline{ENC}$	Complement of ENC, Differential Input
8, 9, 14, 16, 18, 22, 26, 28, 30	AV_{CC}	5 V Analog Power Supply
11	AIN	Analog Input
12	$\overline{AIN}$	Complement of AIN, Differential Analog Input
20	C1	Internal Voltage Reference. Bypass to ground with a 0.1 µF chip capacitor.
24	C2	Internal Voltage Reference. Bypass to ground with a 0.1 µF chip capacitor.
31	DNC	Do not connect this pin.
32	OVR*	Over-Range Bit. A logic-level high indicates analog input exceeds ±FS.
35	DMID	Output Data Voltage Midpoint. Approximately equal to $(DV_{CC})/2$.
36	D0 (LSB)	Digital Output Bit (Least Significant Bit); Two's Complement
37–41, 44–50	D1–D5, D6–D12	Digital Output Bits in Two's Complement
51	D13 (MSB)	Digital Output Bit (Most Significant Bit); Two's Complement
52	DRY	DataReady Output

*The functionality of the Over-Range bit is specified for a temperature range of 25°C to 85°C only.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specs define an acceptable ENCODE duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{Full\ Scale} = 10\log\left[\frac{\frac{V^2{}_{Full\ Scale\ rms}}{|Z|_{Input}}}{0.001}\right]$$

Harmonic Distortion, 2nd
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, 3rd
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Noise (For Any Range Within the ADC)

$$V_{NOISE} = \sqrt{|Z| \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

Where Z is the input impedance, FS is the full scale of the device for the frequency in question; SNR is the value for the particular input level; and Signal is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Power Supply Rise Time
The time from when the dc supply is initiated, until the supply output reaches the minimum specified operating voltage for the ADC. The dc level is measured at supply pin(s) of the ADC.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Two Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

EQUIVALENT CIRCUITS

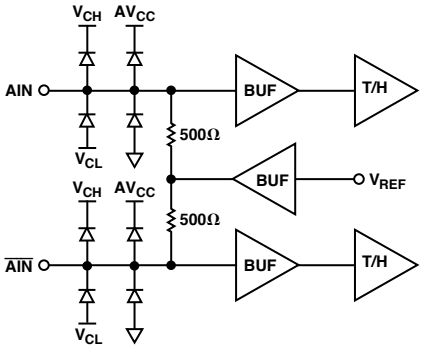


Figure 2. Analog Input Stage

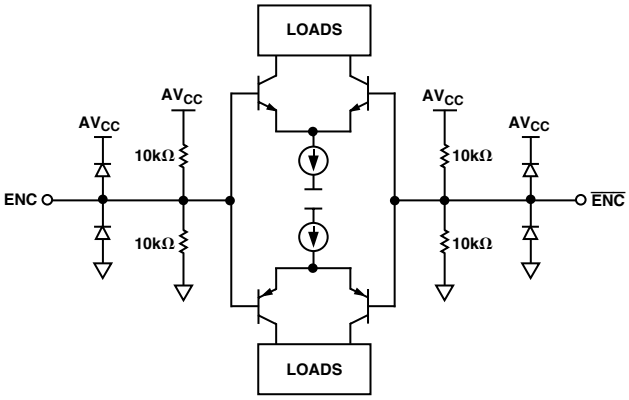


Figure 3. Encode Inputs

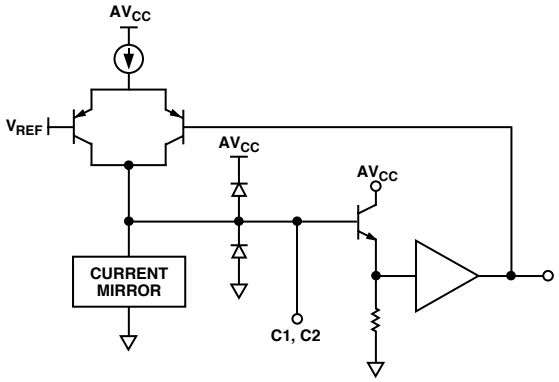


Figure 4. Compensation Pin, C1 or C2

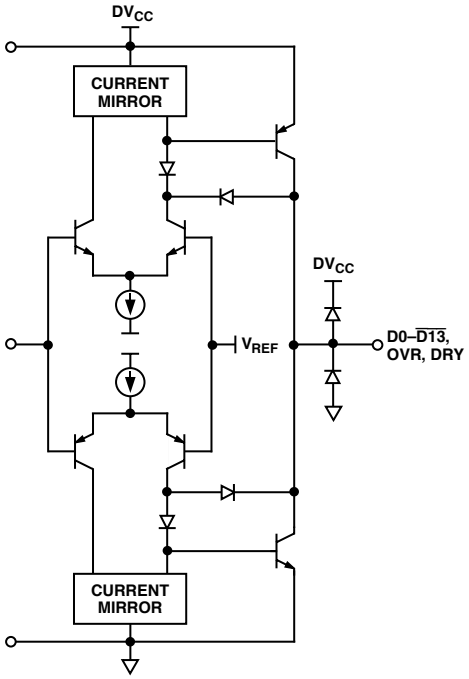


Figure 5. Digital Output Stage

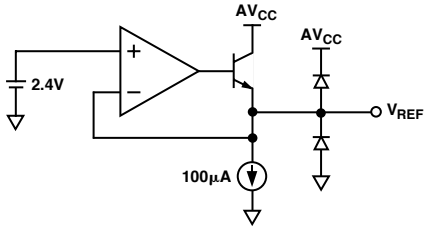


Figure 6. 2.4 V Reference

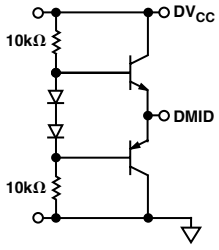
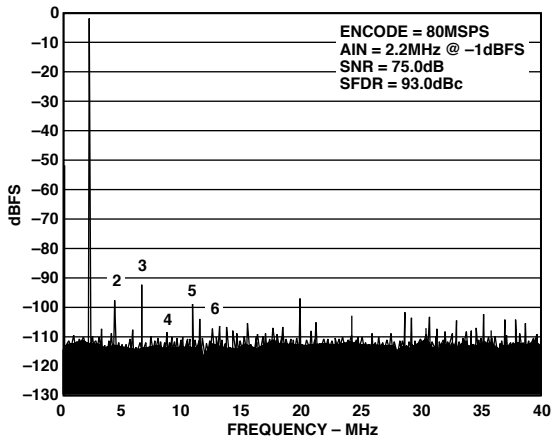
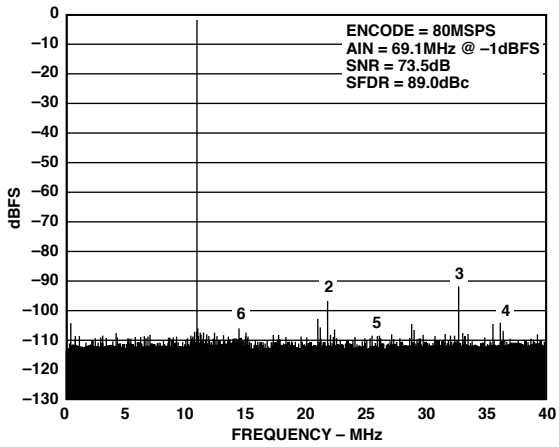


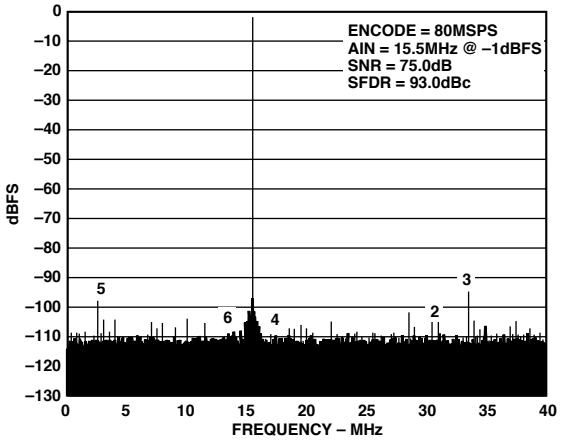
Figure 7. DMID Reference



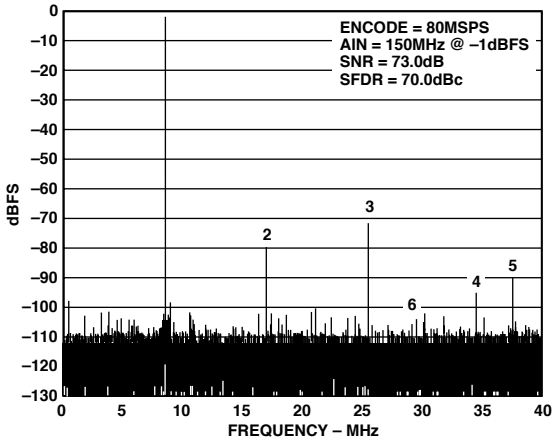
TPC 1. Single Tone @ 2.2 MHz



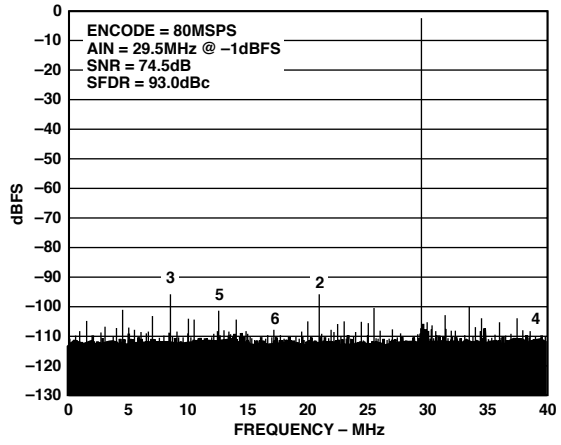
TPC 4. Single Tone @ 69.1 MHz



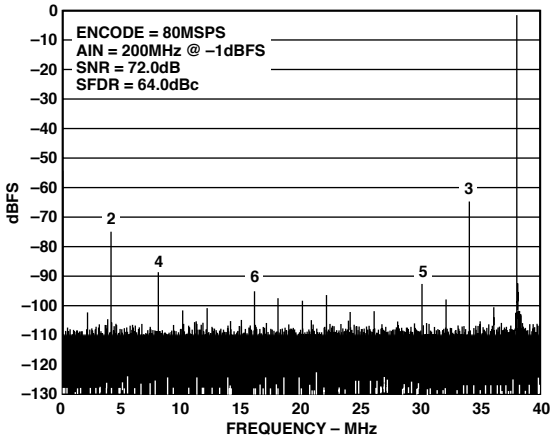
TPC 2. Single Tone @ 15.5 MHz



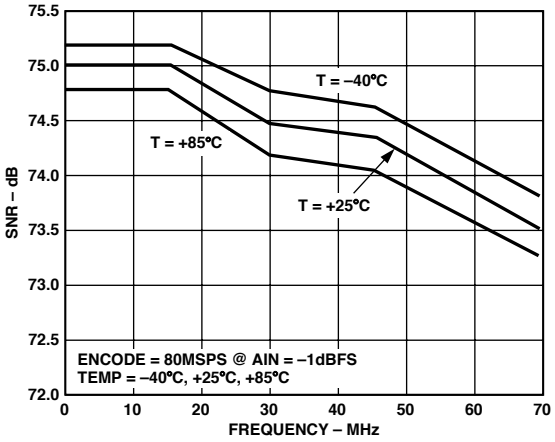
TPC 5. Single Tone @ 150 MHz



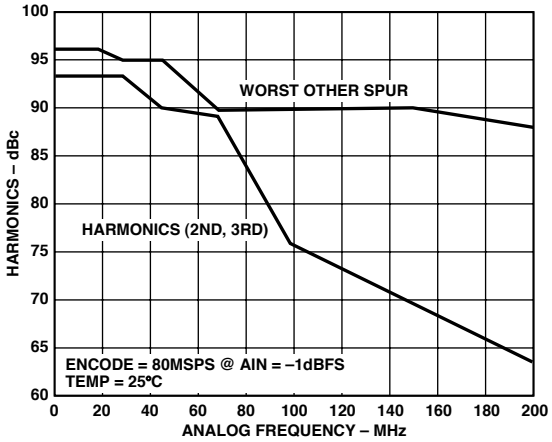
TPC 3. Single Tone @ 29.5 MHz



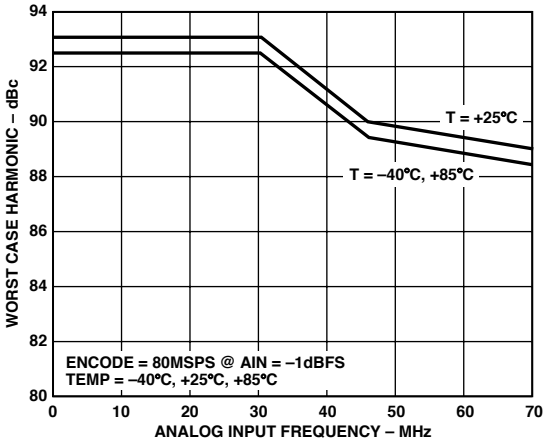
TPC 6. Single Tone @ 200 MHz



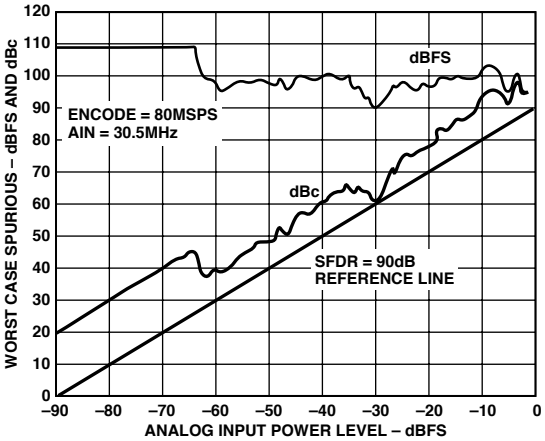
TPC 7. Noise vs. Analog Frequency



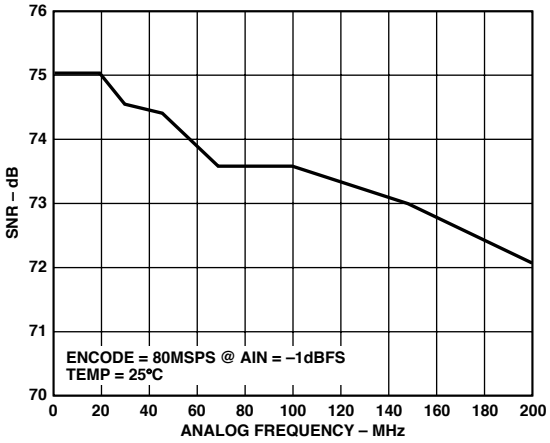
TPC 10. Harmonics vs. Analog Frequency (IF)



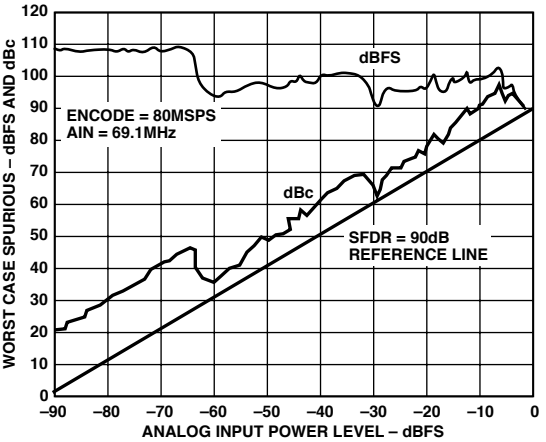
TPC 8. Harmonics vs. Analog Frequency



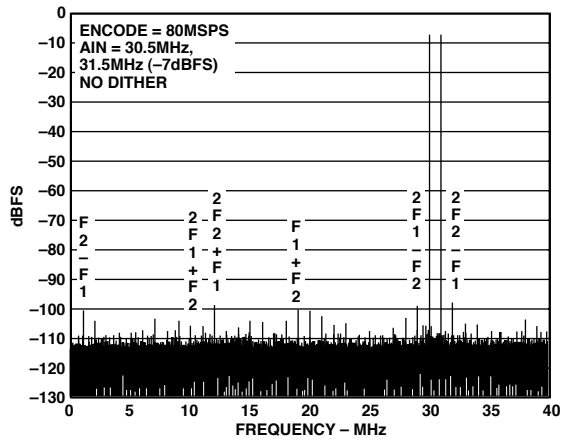
TPC 11. Single Tone SFDR @ 30.5 MHz



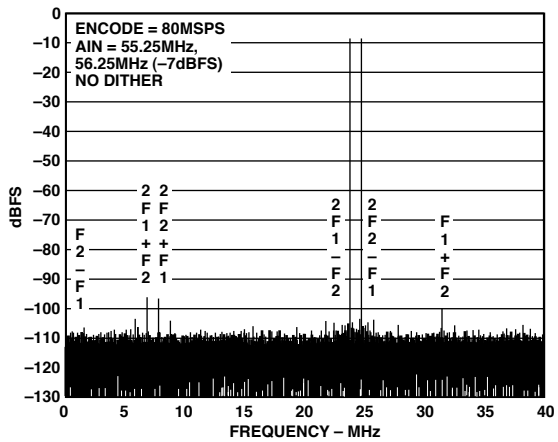
TPC 9. Noise vs. Analog Frequency (IF)



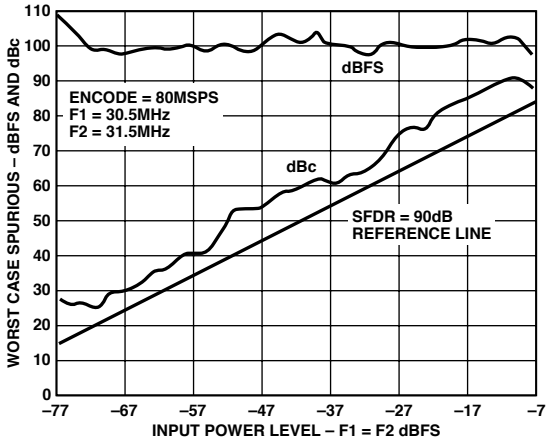
TPC 12. Single Tone SFDR @ 69.1 MHz



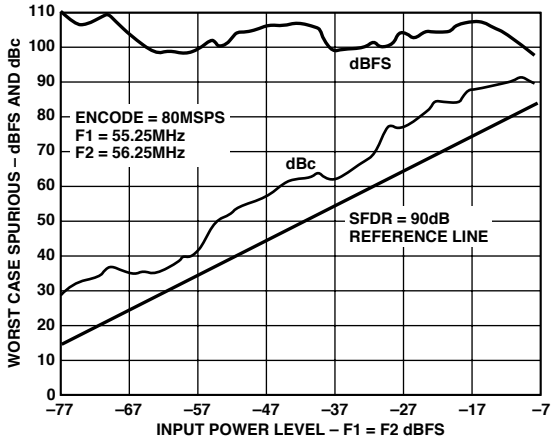
TPC 13. Two Tones @ 30.5 MHz and 31.5 MHz



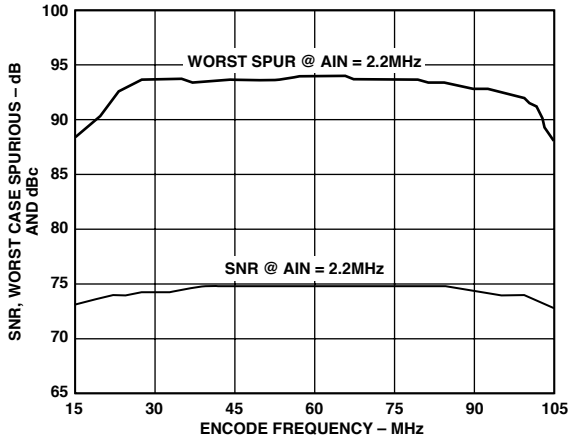
TPC 16. Two Tone SFDR @ 55.25 MHz and 56.25 MHz



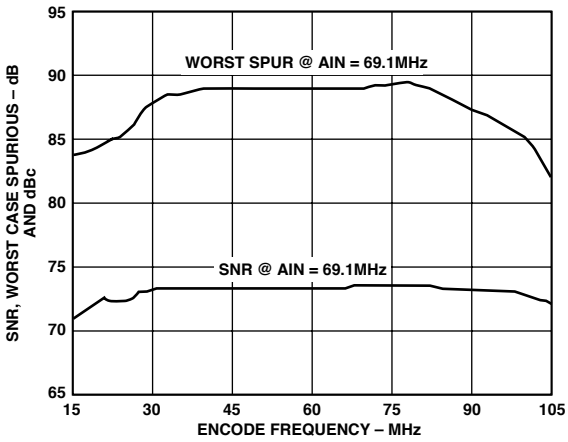
TPC 14. Two Tone SFDR @ 30.5 MHz and 31.5 MHz



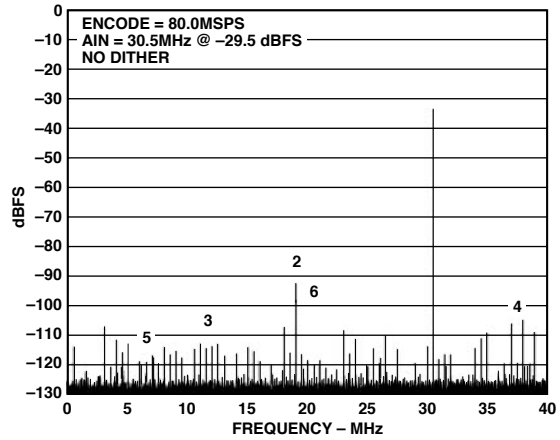
TPC 17. Two Tone SFDR @ 55.25 MHz and 56.25 MHz



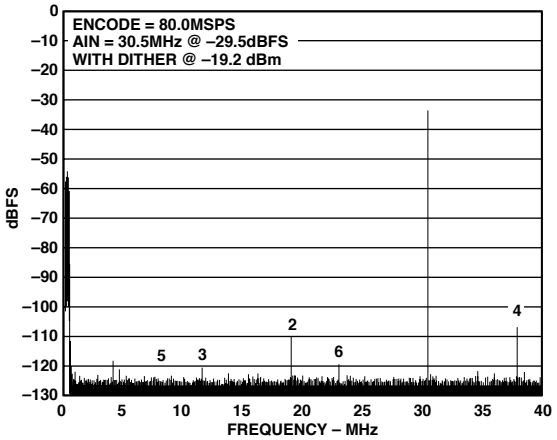
TPC 15. SNR, Worst Spurious vs. Encode @ 2.2 MHz



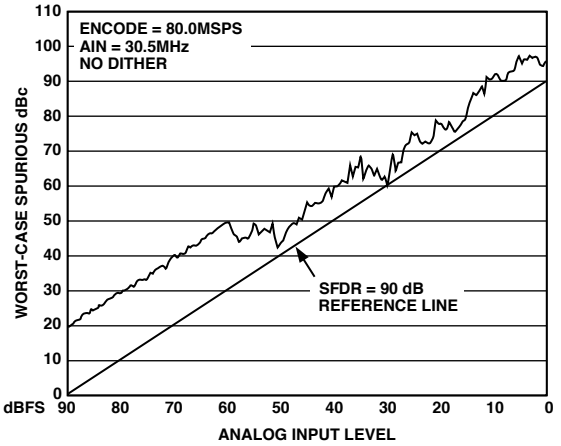
TPC 18. SNR, Worst Spurious vs. Encode @ 69.1 MHz



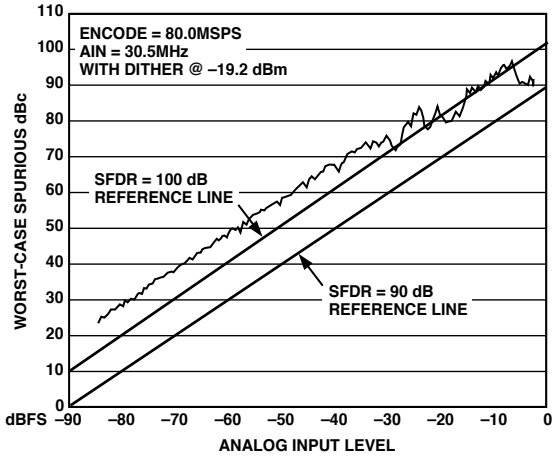
TPC 19. 1 M FFT without Dither



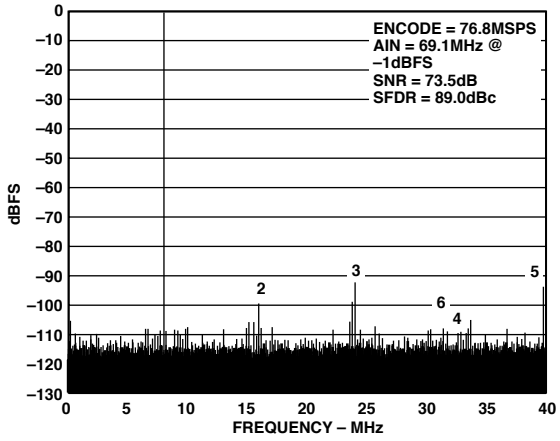
TPC 22. 1 M FFT with Dither



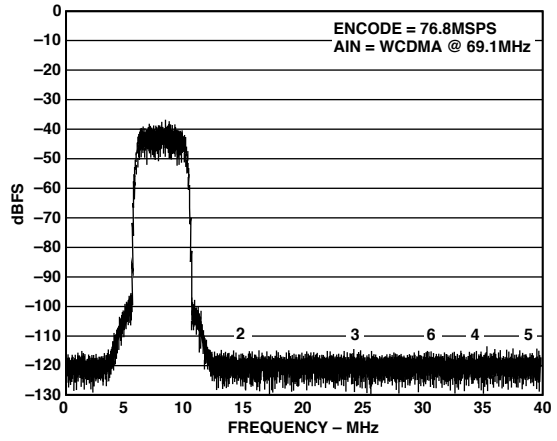
TPC 20. SFDR without Dither



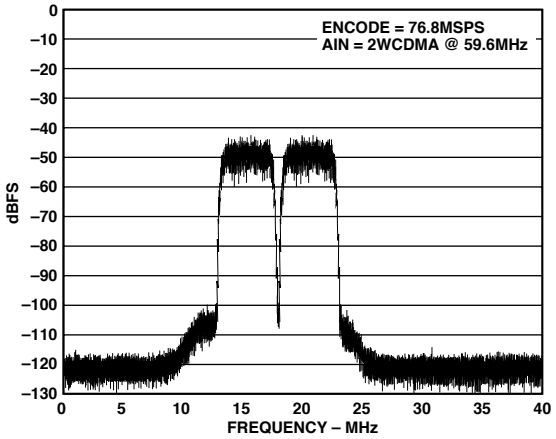
TPC 23. SFDR with Dither



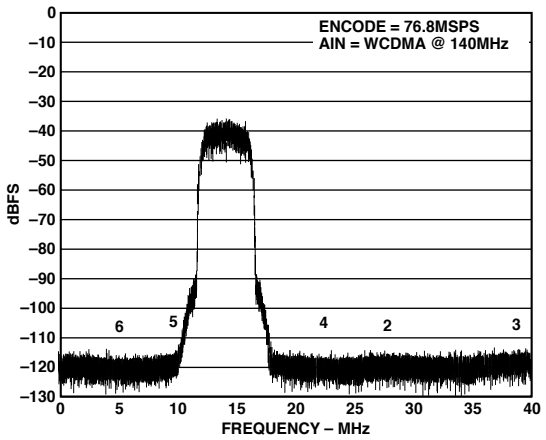
TPC 21. Single Tone 69.1 MHz: Encode = 76.8 MSPS



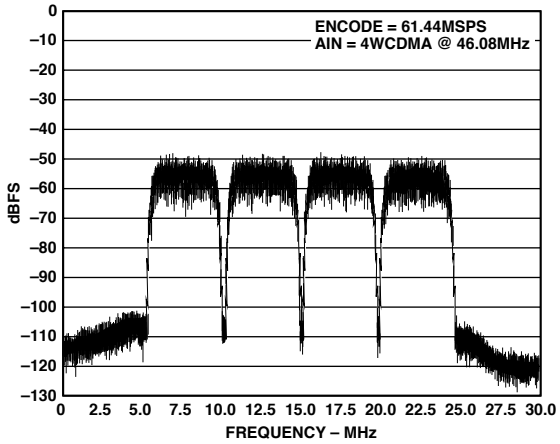
TPC 24. WCDMA Tone 69.1 MHz: Encode = 76.8 MSPS



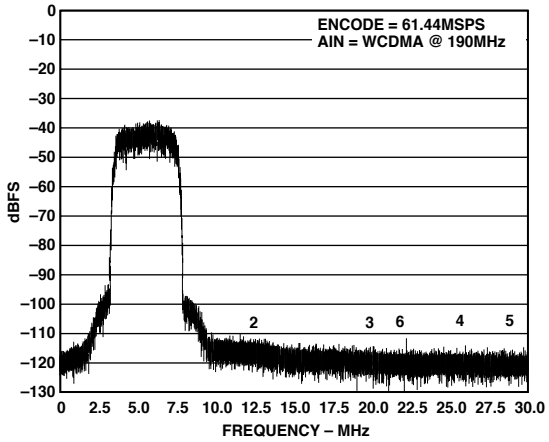
TPC 25. 2 WCDMA Carriers @ A_{IN} = 59.6 MHz: Encode = 76.8 MSPS



TPC 27. WCDMA Tone 140 MHz: Encode = 76.8 MSPS



TPC 26. 4 WCDMA Carriers @ A_{IN} = 46.08 MHz: Encode = 61.44 MSPS



TPC 28. WCDMA Tone 190 MHz: Encode = 61.44 MSPS

THEORY OF OPERATION

The AD6645 analog-to-digital converter (ADC) employs a three stage subrange architecture. This design approach achieves the required accuracy and speed while maintaining low power and small die size.

As shown in the functional block diagram, the AD6645 has complementary analog input pins, AIN and $\overline{AIN}$. Each analog input is centered at 2.4 V and should swing ±0.55 V around this reference (see Figure 2). Since AIN and $\overline{AIN}$ are 180 degrees out of phase, the differential analog input signal is 2.2 V peak-to-peak.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives a 5-bit digital-to-analog converter, DAC1. DAC1 requires 14 bits of precision, which is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residue signal is applied to a second conversion stage consisting of a 5-bit ADC2, 5-bit DAC2, and pipeline TH4. The second DAC requires 10 bits of precision, which is met by the process with no trim. The input to TH5 is a second residue signal generated by subtracting the quantized output of DAC2 from the first residue signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS-compatible word, coded as two's complement.

APPLYING THE AD6645

Encoding the AD6645

The AD6645 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3–4 dB with 70 MHz analog input signals when using a high jitter clock source. See AN-501, "Aperture Uncertainty and ADC System Performance" for complete details.

For optimum performance, the AD6645 must be clocked differentially. The encode signal is usually ac-coupled into the ENC and $\overline{ENC}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Shown below is one preferred method for clocking the AD6645. The clock source (low jitter) is converted from single-ended to differential using a RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6645 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6645, and limits the noise presented to the encode inputs.

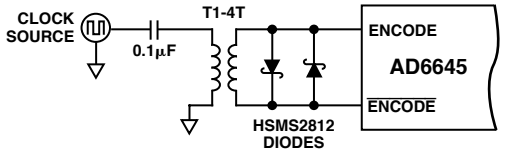


Figure 8. Crystal Clock Oscillator, Differential Encode

If a low jitter clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown below. The MC100EL16 (or same family) from ON-SEMI offers excellent jitter performance.

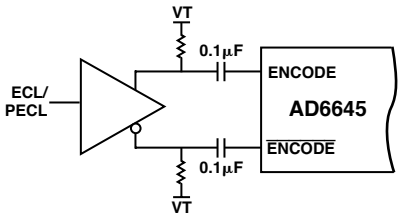


Figure 9. Differential ECL for Encode

Driving the Analog Inputs

As with most new high-speed, high dynamic range analog-to-digital converters, the analog input to the AD6645 is differential. Differential inputs improve on-chip performance as signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even-order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection to stray signals such as ground and power noise. Second, they provide good rejection to common-mode signals such as local oscillator feed-through.

The AD6645 analog input voltage range is offset from ground by 2.4 V. Each analog input connects through a 500 Ω resistor to the 2.4 V bias voltage and to the input of a differential buffer (Figure 2). The resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6645 should be ac-coupled to the input pins. Since the differential input impedance of the AD6645 is 1 kΩ, the analog input power requirement is only –2 dBm, simplifying the driver amplifier in many cases. To take full advantage of this high input impedance, a 20:1 transformer would be required. This is a large ratio and could result in unsatisfactory performance. In this case, a lower step-up ratio could be used. The recommended method for driving the analog input of the AD6645 is to use a 4:1 RF transformer. For example, if RT were set to 60.4 Ω and RS were set to 25 Ω, along with a 4:1 impedance ratio transformer, the input would match to a 50 Ω source with a full-scale drive of 4.8 dBm. Series resistors (RS) on the secondary side of the transformer should be used to isolate the transformer from A/D. This will limit the amount of dynamic current from the A/D flowing back into the secondary of the transformer. The 50 Ω impedance matching can also be incorporated on the secondary side of the transformer as shown in the evaluation board schematic (Figure 13).

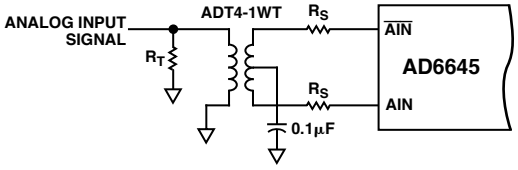


Figure 10. Transformer-Coupled Analog Input Circuit

In applications where dc-coupling is required, a differential output op amp such as the AD8138 from Analog Devices can be used to drive the AD6645 (Figure 11). The AD8138 op amp provides single-ended-to-differential conversion, which reduces overall system cost and minimizes layout requirements.

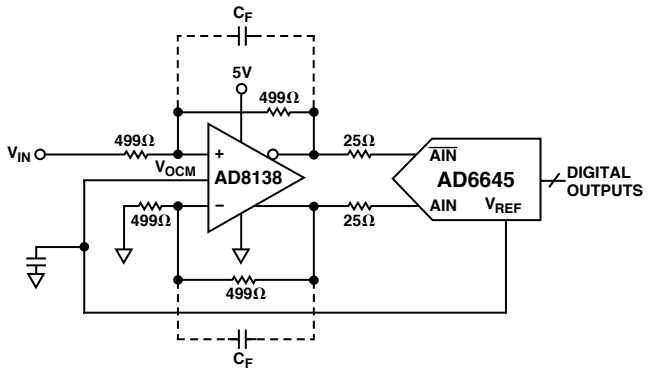


Figure 11. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. The use of linear dc supplies with rise-times of <45 ms is highly recommended. Switching supplies tend to have radiated components that may be "received" by the AD6645. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD6645 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. Although analog and digital supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD6645 is specified for DV_{CC} = 3.3 V as this is a common supply for digital ASICS.

Digital Outputs

Care must be taken when designing the data receivers for the AD6645. It is recommended that the digital outputs drive a series resistor followed by a gate such as the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic shown in Figure 13. The digital outputs of the AD6645 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace will have a load of approximately 10 pF. Therefore, as each bit switches 10 mA $\left(10\ pF \times 1V \div 1\ ns\right)$ of dynamic current per bit will flow in or out of the device. A full-scale transition can cause up to 140 mA (14 bits × 10 mA/bit) of current to flow through the output stages. The series resistors should be placed as close to the AD6645 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD6645. It should be noted that extra capacitive loading will increase output timing and invalidate timing specifications. Digital output timing is guaranteed for output loads up to 10 pF.

Digital output states for given analog input levels are shown in Table I.

Grounding

For optimum performance, it is highly recommended that a common ground be utilized between the analog and digital power planes. The primary concern with splitting grounds is that dynamic currents may be forced to travel significant distances in the system before recombining back at the common source ground. This can result in a large and undesirable ground loop. The most common place for this to occur is on the digital outputs of the ADC. Ground loops can contribute to digital noise being coupled back onto the ADC front end. This can manifest itself as either harmonic spurs, or very high order spurious products that can cause excessive spikes on the noise floor. This noise coupling is less likely to occur at lower clock speeds since the digital noise has more time to settle between samples. In general, splitting the analog and digital grounds can frequently contribute to undesirable EMI-RFI and should therefore be avoided.

Conversely, if not properly implemented, common grounding can actually impose additional noise issues since the digital ground currents are riding on top of the analog ground currents in close proximity to the ADC input. To minimize the potential for noise coupling further, it is highly recommended that multiple ground return traces/vias be placed such that the digital output currents do not flow back towards the analog front end, but are routed quickly away from the ADC. This does not require a split in the ground plane and can be accomplished by simply placing substantial ground connections directly back to the supply at a point between the analog front end and the digital outputs. The judicious use of ceramic chip capacitors between the power supply and ground planes will also help suppress digital noise. The layout should incorporate enough bulk capacitance to supply the peak current requirements during switching periods.

Layout Information

The schematic of the evaluation board (Figure 13) represents a typical implementation of the AD6645. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6645 facilitates ease of use in the implementation of high-frequency, high-resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6645, minimal capacitive loading should be placed on these outputs. It is recommended that a fan-out of only one gate should be used for all AD6645 digital outputs.

The layout of the encode circuit is equally critical. Any noise received on this circuitry will result in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

Table I. Two's Complement Output Coding

AIN Level	$\overline{AIN}$ Level	Output State	Output Code
V_{REF} + 0.55 V	V_{REF} – 0.55 V	Positive FS	01 1111 1111 1111
V_{REF}	V_{REF}	Midscale	00…0/11…1
V_{REF} – 0.55 V	V_{REF} + 0.55 V	Negative FS	10 0000 0000 0000

Jitter Considerations

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, the above equation accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

F_{ANALOG} = analog input frequency
$t_{j\ rms}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry)
ϵ = average DNL of the ADC (typically 0.41 LSB)
n = number of bits in the ADC
$V_{NOISE\ rms}$ = V rms thermal noise referred to the analog input of the ADC (typically 0.9 LSB rms)

For a 14-bit analog-to-digital converter, like the AD6645, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrate the expected SNR performance of the AD6645 as jitter increases. The chart is derived from the above equation.

For a complete discussion of aperture jitter, please consult AN-501, "Aperture Uncertainty and ADC System Performance."

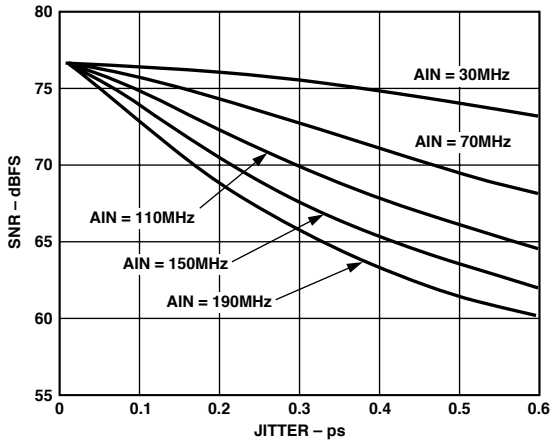


Figure 12. Jitter vs. SNR

$$SNR = 1.76 - 20\log\left[\left(2\pi \times F_{ANALOG} \times t_{j\ rms}\right)^2 + \left(\frac{1+\varepsilon}{2^n}\right)^2 + \left(\frac{2\times\sqrt{2}\times V_{NOISE\ rms}}{2^n}\right)^2\right]^{\frac{1}{2}}$$

Table II. AD6645ASQ/PCB Bill of Materials

Item No.	Qty	Reference ID[1]	Description	Manufacturer
1	1	6645EE01C	AD6644/AD6645 Evaluation Printed Circuit Board	PCSM, Inc. (6645EE01C)
2	3	C1, C2, C38	Capacitor, Tantalum SMT T491C, 10 µF; 16 V; 10%	Kemet (T491C106M016AS)
3	9	C3, C7–C11, C16, C30, C32	Capacitor, SMT 0508, 0.1 µF; 16 V; 10%	Presidio Components (0508X7R104K16VP6)
4	8	C4, C22–C26, C29, (C33), (C34), C39	Capacitor, SMT 0805, 0.1 µF; 25 V; 10%	Panasonic (ECJ-2VB1E104K)
5	0	(C5, C6)	Capacitor, SMT 0805, 0.01 µF; 50 V; 10%	Panasonic (ECJ-2YB1H103K)
6	9	C12–C14, C17–C21, C40	Capacitor, SMT 0508, 0.01 µF; 16 V; 10%	Presidio Components (0508X7R103M2P3)
7	1	CR1	Diode, Schottky Barrier, Dual	Panasonic (MA716-TX)
8	1	E3, E4, E5	100" Straight Male Header (Single Row), 3 of 50 pins	Samtec (TSW-1-50-08-G-S)
9	4	F1–F4	EMI Suppression Ferrite Chip, SMT 0805	Steward (HZ0805E601R-00)
10	1	J1	Connector, PCB Pin Strip; 5 pins; 5 mm pitch	Wieland (Z5.530.0525.0)
11	1	J1	Connector, PCB Terminal; 5 pins; 5 mm pitch	Wieland (25.602.2553.0)
12	1	J2	Terminal Strip, 50 pin; right angle	Samtec (TSW-125-08-T-DRA)
13	0	(J3)	Connector, SMA; RF; Gold	Johnson Components, Inc. (142-0701-201)
14	2	J4, J5	Connector, Coaxial RF Receptacle; 50 Ω	AMP (227699-2)
15	0	(R1)	Resistor, SMT 0402; 100; 1/16w; 1%	Panasonic (ERJ-2RKF1000X)
16	0	(R2)[2]	Resistor, SMT 1206; 60.4; 1/8w; 1%	Panasonic (ERJ-8ENF60R4V)
17	0	(R3, R4, R5, R8)	Resistor, SMT 0805; 499; 1/10w; 1%	Panasonic (ERJ-6ENF4990V)
18	2	R6, R7	Resistor, SMT 0805; 25.5; 1/10w; 1%	Panasonic (ERJ-6ENF25R5V)
19	1	R9	Resistor, SMT 0805; 348; 1/10w; 1%	Panasonic (ERJ-6ENF3480V)
20	1	R10	Resistor, SMT 0805; 619; 1/10w; 1%	Panasonic (ERJ-6ENF6190V)
21	0	(R11), (R13)	Resistor, SMT 0805; 66.5; 1/10w; 1%	Panasonic (ERJ-6ENF66R5V)
22	0	(R12), (R14)	Resistor, SMT 0805; 100; 1/10w; 1%	Panasonic (ERJ-6ENF1000V)
23	1	R15[2]	Resistor, SMT 0402; 178; 1/16w; 1%	Panasonic (ERJ-2RKF1780X)
24	1	R35	Resistor, SMT 0805; 49.9; 1/10w; 1%	Panasonic (ERJ-6ENF49R9V)
25	2	RN1, RN3	Resistor Array, SMT 0402; 470; 1/4w; 5%	Panasonic (EXB2HV471JV)
26	2	RN2, RN4	Resistor Array, SMT 0402; 220; 1/4w; 5%	Panasonic (EXB2HV221JV)
27	1	T2	RF Transformer, SMT KK81, 0.2–350 MHz; 4:1 Ω Ratio	Mini-Circuits (T4-1-KK81)
28	1	T3	RF Transformer, SMT CD542, 2–775 MHz; 4:1 Ω Ratio	Mini-Circuits (ADT4-1WT)
29	1	U1	I.C., QFP-52; 14-Bit, 80 MSPS Wideband Analog-to-Digital Converter	Analog Devices (AD6645ASQ)
30	2	U2, U7	I.C., SOIC-20; Octal D-Type Flip-Flop	Fairchild (74LCX574WM)
31	0	(U3)	I.C., SOIC-8; Low Distortion Differential ADC Driver	Analog Devices (AD8138AR)
32	2	U4, U6	I.C., SMT SOT-23; TinyLogic UHS 2-Input OR Gate	Fairchild (NC7SZ32)
33	1	U5[3]	Clock Oscillator, Full Size MX045; 80 MHz	CTS Reeves (MXO45-80)
34	4	U5[3]	Connector, Miniature Spring Socket,	Amp (5-330808-3)
35	0	(U8)	I.C., SOIC-8; Differential Receiver	Motorola (MC100EL16)
36	4	See drawing	Circuit Board Support on Base	Richo (CBSB-14-01)
37	1	See drawing	0.100" Shorting Block	Jameco (152670)

NOTES
[1]Reference designators in parentheses are not installed on standard units. (AC-coupled AIN and ENCODE.)
AC-coupled AIN is standard, R3, R4, R5, R8, and U3 are not installed.
If dc-coupled AIN is required, C30, T3, and R15 are not installed.
AC-coupled ENCODE is standard. C5, C6, C33, C34, R1, R11–R14, and U8 are not installed.
If PECL ENCODE is required, CR1 and T2 are not installed.
[2]R2 is installed for 50 Ω impedance input matching on the primary of T3. R15 is not installed.
R15 is installed for 50 Ω impedance input matching on the secondary of T3. R2 is not installed.
[3]U5 Clock Oscillator is installed with pin sockets for removal if OPT_CLK input is used.

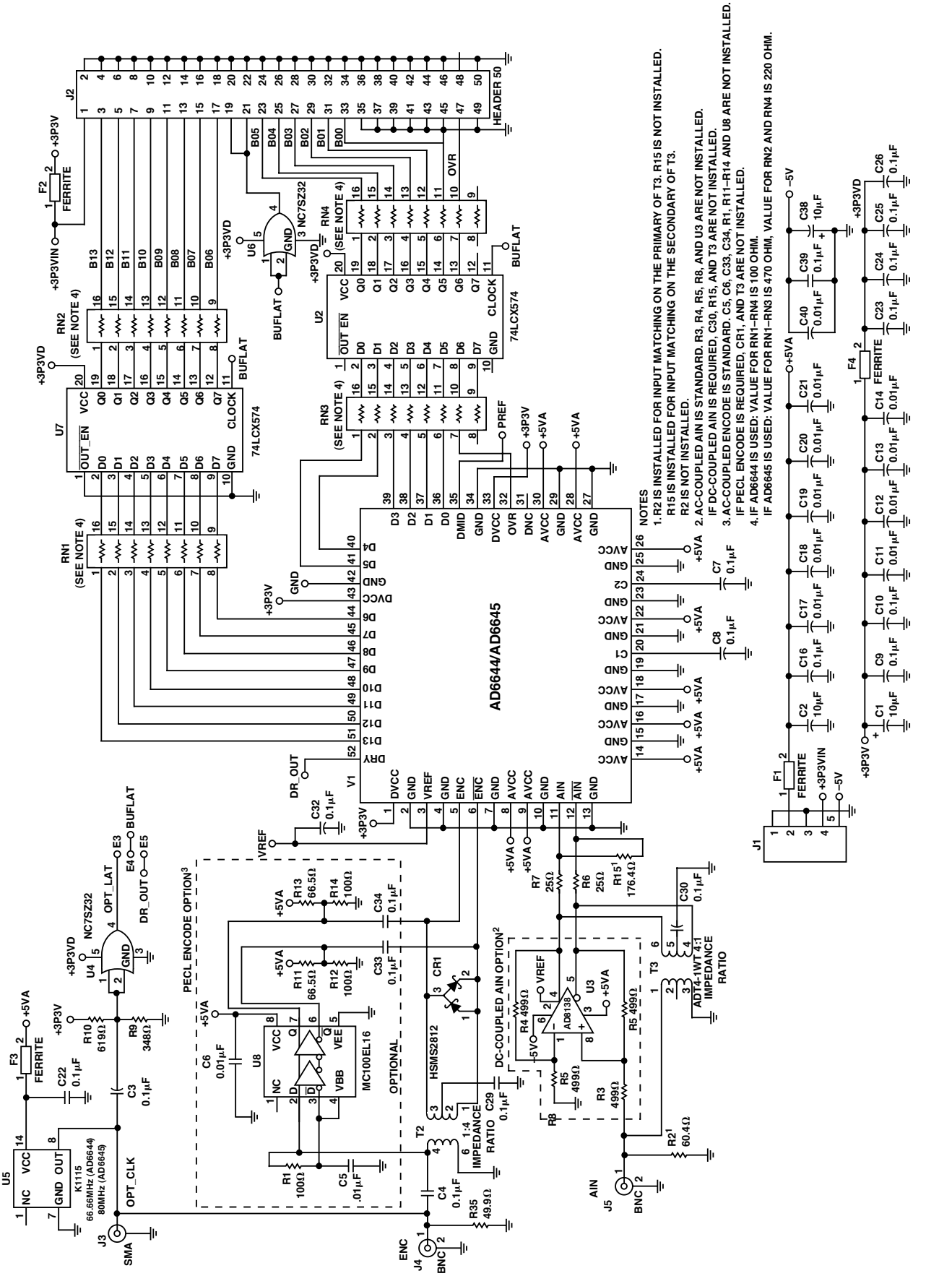


Figure 13. Evaluation Board Schematic

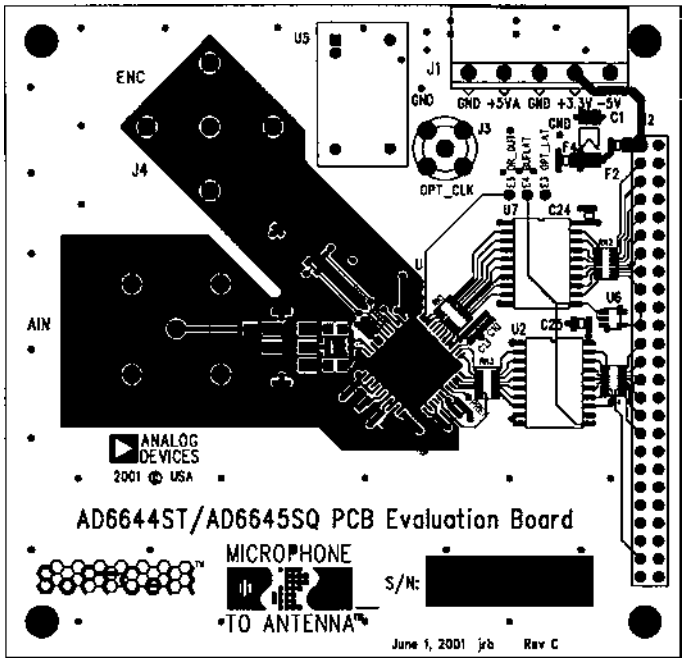


Figure 14. Top Signal Level

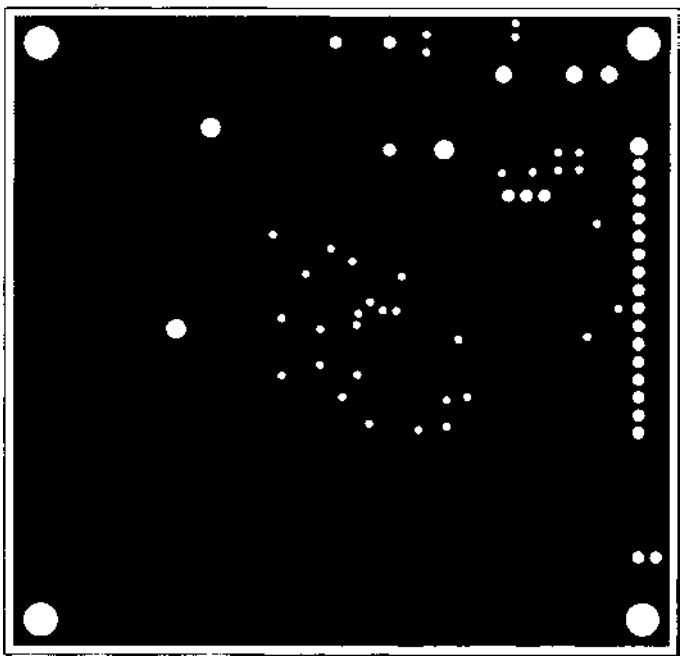


Figure 16. Ground Plane Layer 2 and 5

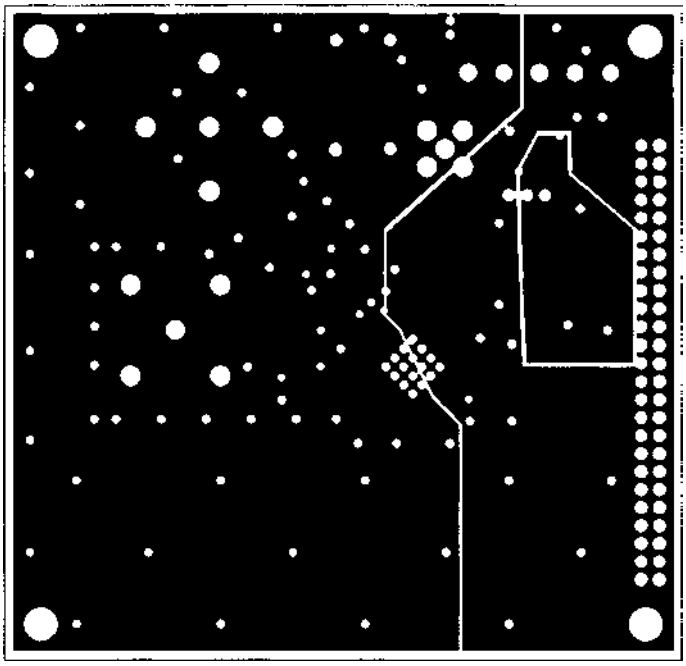


Figure 15. 5.0 V/3.3 V Plane Layers 3 and 4

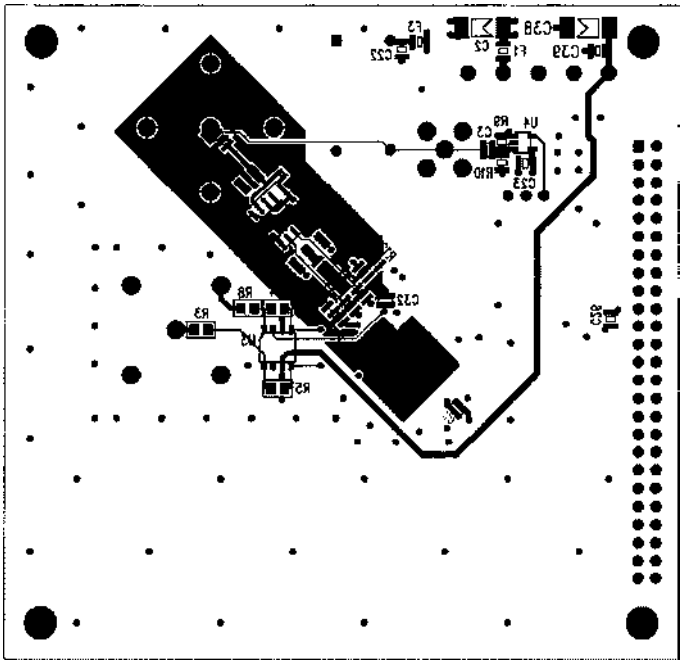
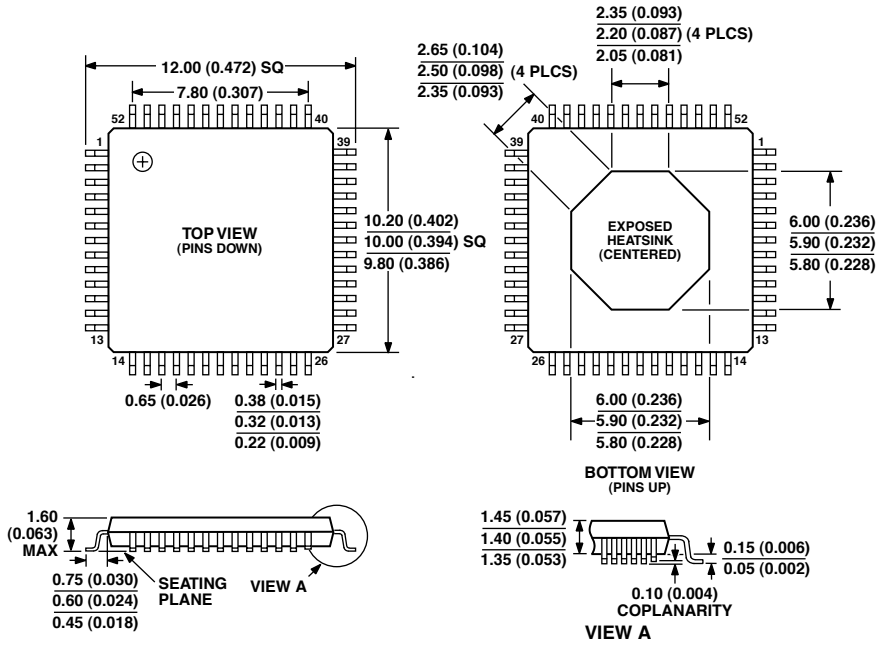


Figure 17. Bottom Signal Layer

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches).

52-Lead PowerQuad 4 (LQFP_ED)
(SQ-52)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

THE AD6645 POWERQUAD 4 (LQFP_ED) HAS A THERMALLY AND ELECTRICALLY CONDUCTIVE HEAT SLUG EXPOSED ON THE BOTTOM OF THE PACKAGE WHICH CAN BE UTILIZED FOR ENHANCED THERMAL MANAGEMENT. IT IS RECOMMENDED THAT NO UNMASKED ACTIVE PCB TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME INTO CONTACT WITH THE GROUNDED HEAT SLUG. ALTHOUGH NOT A REQUIREMENT FOR SPECIFIED OPERATION, SOLDERING THE SLUG TO A GROUND PLANE WITH SUFFICIENT THERMAL CAPACITY WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE. THIS MAY PROVE BENEFICIAL IN HIGH RELIABILITY APPLICATIONS WHERE LOWER JUNCTION TEMPERATURES TYPICALLY CONTRIBUTE TO INCREASED SEMICONDUCTOR RELIABILITY.

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