AC‘97 SoundMAX® Codec

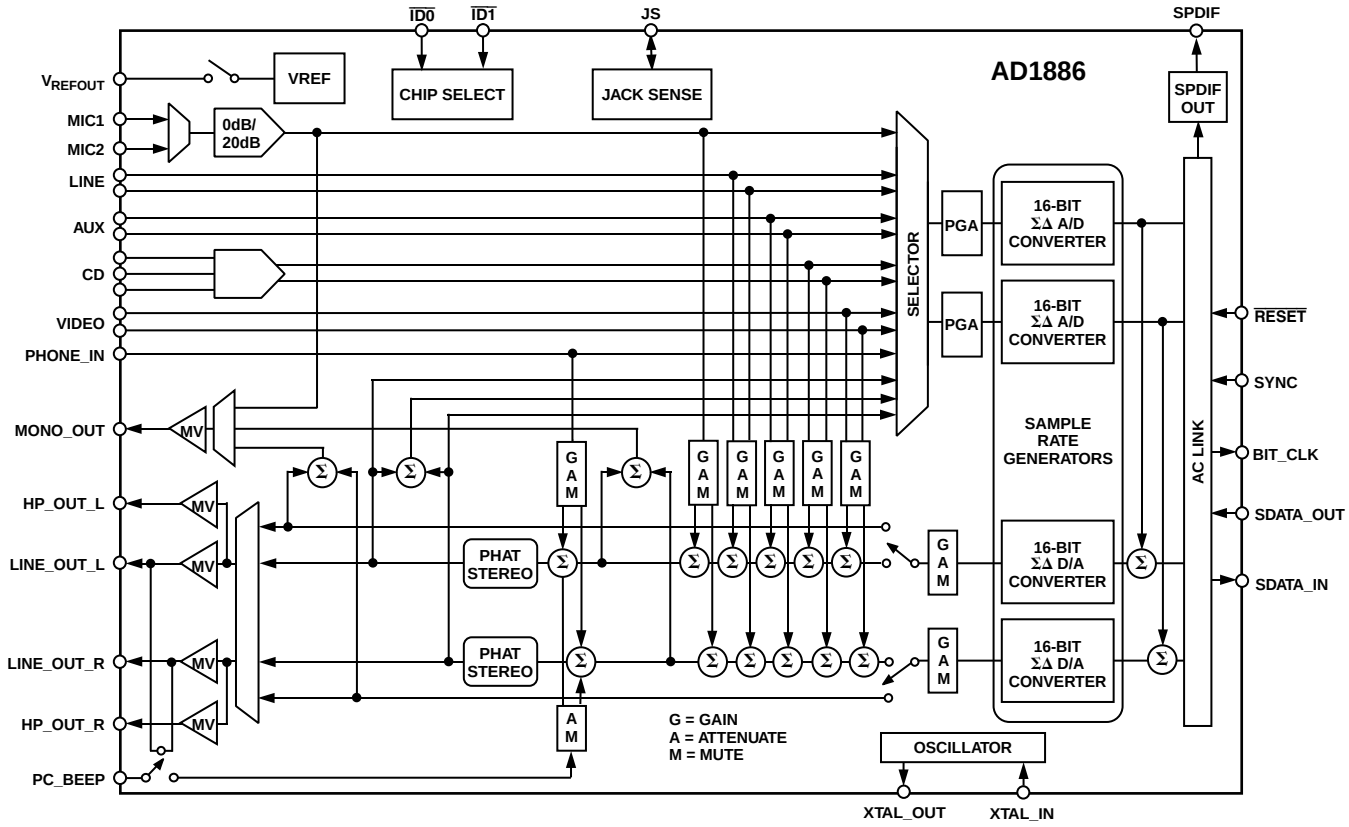
AD1886

AC’97 2.1 FEATURES
Variable Sample Rate Audio
Multiple Codec Configuration Options
External Audio Power-Down Control

AC ’97 FEATURES
AC ’97 2.1 Compliant
Greater than 90 dB Dynamic Range
Stereo Headphone Amplifier
Multibit Σ-Δ Converter Architecture for Improved S/N Ratio Greater than 90 dB
16-Bit Stereo Full-Duplex Codec
Four Analog Line-Level Stereo Inputs for: LINE-IN, CD, VIDEO, and AUX
Two Analog Line-Level Mono Inputs for Speakerphone and PC BEEP
Mono MIC Input w/Built-In 20 dB Preamp, Switchable from Two External Sources
High-Quality CD Input with Ground Sense
Stereo Line Level Outputs
Mono Output for Speakerphone or Internal Speaker
Power Management Support
48-Terminal TQFP Package

ENHANCED FEATURES
S/PDIF Output with 48 kHz, 44.1 kHz, and 32 kHz Sample Rates
Full Duplex Variable Sample Rates from 7040 Hz to 48 kHz with 1 Hz Resolution
Jack Sense Pins Provide Automatic Output Switching
Software-Enabled V_{REFOUT} Output for Microphones and External Power Amp
Split Power Supplies (3.3 V Digital/5 V Analog)
Mobile Low-Power Mixer Mode
Extended 6-Bit Master Volume Control
Extended 6-Bit Headphone Volume Control
Digital Audio Mixer Mode
Phat™ Stereo 3D Stereo Enhancement

FUNCTIONAL BLOCK DIAGRAM



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REV. 0

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AD1886–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25°C	*DAC Test Conditions*
Digital Supply (V_{DD})	3.3 V	Calibrated
Analog Supply (V_{CC})	5.0 V	–3 dB Attenuation Relative to Full Scale
Sample Rate (F_S)	48 kHz	Input 0 dB
Input Signal	1008 Hz	10 kΩ Output Load (LINE_OUT)
Analog Output Passband	20 Hz to 20 kHz	32 Ω Output Load (HP_OUT)
V_{IH}	2.0 V	
V_{IL}	0.8 V	*ADC Test Conditions*
V_{IH} (CS0, CS1, CHAIN_IN)	4.0 V	Calibrated
V_{IL}	1.0 V	0 dB Gain
		Input –3.0 dB Relative to Full Scale

ANALOG INPUT

Parameter	Min	Typ	Max	Unit
Input Voltage (RMS Values Assume Sine Wave Input)				
LINE_IN, AUX, CD, VIDEO, PHONE_IN, PC_BEEP		1		V rms
		2.83		V p-p
MIC with +20 dB Gain (M20 = 1)		0.1		V rms
		0.283		V p-p
MIC with 0 dB Gain (M20 = 0)		1		V rms
		2.83		V p-p
Input Impedance*		20		kΩ
Input Capacitance*		5	7.5	pF

MASTER VOLUME

Parameter	Min	Typ	Max	Unit
Step Size (0 dB to –94.5 dB); LINE_OUT_L, LINE_OUT_R		1.5		dB
Output Attenuation Range Span*		–94.5		dB
Step Size (0 dB to –46.5 dB); MONO_OUT		1.5		dB
Output Attenuation Range Span*		–46.5		dB
Step Size (+6 dB to –88.5 dB); HP_OUT_R, HP_OUT_L		1.5		dB
Output Attenuation Range Span*		–94.5		dB
Mute Attenuation of 0 dB Fundamental*			80	dB

PROGRAMMABLE GAIN AMPLIFIER—ADC

Parameter	Min	Typ	Max	Unit
Step Size (0 dB to 22.5 dB)		1.5		dB
PGA Gain Range Span		22.5		dB

ANALOG MIXER—INPUT GAIN/AMPLIFIERS/ATTENUATORS

Parameter	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)				
CD to LINE_OUT		90		dB
Other to LINE_OUT		90		dB
Step Size (+12 dB to –34.5 dB): (All Steps Tested)				
MIC, LINE_IN, AUX, CD, VIDEO, PHONE_IN, DAC		1.5		dB
Input Gain/Attenuation Range:				
MIC, LINE, AUX, CD, VIDEO, PHONE_IN, DAC		–46.5		dB
Step Size (0 dB to –45 dB): (All Steps Tested)				
PC_BEEP		3.0		dB
Input Gain/Attenuation Range: PC_BEEP		–45		dB

*Guaranteed but not tested.

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

Parameter	Min	Typ	Max	Unit
Passband	0		$0.4 \times F_S$	Hz
Passband Ripple			±0.09	dB
Transition Band	$0.4 \times F_S$		$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$		∞	Hz
Stopband Rejection	–74			dB
Group Delay			$12/F_S$	sec
Group Delay Variation over Passband			0.0	µs

ANALOG-TO-DIGITAL CONVERTERS

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Total Harmonic Distortion (THD)		–84		dB
Dynamic Range (–60 dB input THD + N Referenced to Full Scale, A-Weighted)	84	87		dB
Signal-to-Intermodulation Distortion* (CCIF Method)		85		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–100	–90	dB
LINE_IN to Other		–90	–85	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			±5	mV

DIGITAL-TO-ANALOG CONVERTERS

Parameter	Min	Typ	Max	Unit
Resolution		16		bits
Total Harmonic Distortion (THD) LINE_OUT		–85		dB
Total Harmonic Distortion (THD) HP_OUT		–75		dB
Dynamic Range (–60 dB Input THD + N Referenced to Full Scale, A-Weighted)	85	90		dB
Signal-to-Intermodulation Distortion* (CCIF Method)		–100		dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)		±10		%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.7	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			–80	dB
Total Audible Out-of-Band Energy (Measured from $0.6 \times F_S$ to 20 kHz)*		–40		dB

ANALOG OUTPUT

Parameter	Min	Typ	Max	Unit
Full-Scale Output Voltage; LINE_OUT		1		V rms
		2.83		V p-p
Output Impedance*			800	Ω
External Load Impedance*	10			kΩ
Output Capacitance*		15		pF
External Load Capacitance			100	pF
Full-Scale Output Voltage; HP_OUT (0 dB Gain)		1		V rms
Output Capacitance*			100	pF
External Load Impedance*			32	Ω
V_{REF}	2.05	2.25	2.45	V
V_{REF_OUT}		2.25		V
V_{REF_OUT} Current Drive			5	mA
Mute Click (Muted Output Minus Unmuted Midscale DAC Output)		±5		mV

*Guaranteed but not tested.

AD1886–SPECIFICATIONS

STATIC DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
High-Level Input Voltage (V_{IH}): Digital Inputs	$0.65 \times DV_{DD}$			V
Low-Level Input Voltage (V_{IL})			$0.35 \times DV_{DD}$	V
High-Level Output Voltage (V_{OH}), I_{OH} = 2 mA	$0.9 \times DV_{DD}$			V
Low-Level Output Voltage (V_{OL}), I_{OL} = 2 mA			$0.1 \times DV_{DD}$	V
Input Leakage Current	–10		10	µA
Output Leakage Current	–10		10	µA

POWER SUPPLY

Parameter	Min	Typ	Max	Unit
Power Supply Range—Analog (AV_{DD})	4.75		5.25	V
Power Supply Range—Digital (DV_{DD})	3.15		3.45	V
Power Dissipation—5 V/3.3 V		TBD		mW
Analog Supply Current—5 V (AV_{DD})		TBD		mA
Digital Supply Current—3.3 V (DV_{DD})		TBD		mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)		40		dB

CLOCK SPECIFICATIONS*

Parameter	Min	Typ	Max	Unit
Input Clock Frequency		24.576		MHz
Recommended Clock Duty Cycle	40	50	60	%

POWER-DOWN STATES

Parameter	Set Bits	DV_{DD} Typ	AV_{DD} Typ	Unit
ADC	PR0	TBD	TBD	mA
DAC	PR1	TBD	TBD	mA
ADC + DAC	PR1, PR0	TBD	TBD	mA
ADC + DAC + Mixer (Analog CD On)	LPMIX, PR1, PR0	TBD	TBD	mA
Mixer	PR2	TBD	TBD	mA
ADC + Mixer	PR2, PR0	TBD	TBD	mA
DAC + Mixer	PR2, PR1	TBD	TBD	mA
ADC + DAC + Mixer	PR2, PR1, PR0	TBD	TBD	mA
Analog CD Only (AC-Link On)	LPMIX, PR5, PR1, PR0	TBD	TBD	mA
Analog CD Only (AC-Link Off)	LPMIX, PR1, PR0, PR4, PR5	TBD	TBD	mA
Standby	PR5, PR4, PR3, PR2, PR1, PR0	TBD	TBD	mA
Headphone Standby	PR6	TBD	TBD	mA

NOTES

*Guaranteed but not tested.

Specifications subject to change without notice.

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

Parameter	Symbol	Min	Typ	Max	Unit
RESET Active Low Pulsewidth	t_{RST_LOW}		1.0		µs
RESET Inactive to BIT_CLK Startup Delay	$t_{RST2CLK}$	162.8			ns
SYNC Active High Pulsewidth	t_{SYNC_HIGH}		1.3		ms
SYNC Low Pulsewidth	t_{SYNC_LOW}		19.5		µs
SYNC Inactive to BIT_CLK Startup Delay	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter*				750	ps
BIT_CLK High Pulsewidth	t_{CLK_HIGH}	32.56	42	48.84	ns
BIT_CLK Low Pulsewidth	t_{CLK_LOW}	32.56	38	48.84	ns
SYNC Frequency			48.0		kHz
SYNC Period	t_{SYNC_PERIOD}		20.8		µs
Setup to Falling Edge of BIT_CLK	t_{SETUP}	5	2.5		ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	5			ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	10	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	10	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	10	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	10	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	10	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	10	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	10	ns
SDATA_OUT Fall Time	$t_{FALLDOUT}$	2	4	10	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low	t_{S2_PDOWN}	0		1.0	µs
Setup to Trailing Edge of RESET (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of RESET to HI-Z Delay	t_{OFF}			25	ns
Propagation Delay				15	ns
RESET Rise Time				50	ns
Output Valid Delay from Rising Edge of BIT_CLK to SDI Valid				15	ns

NOTES

*Output jitter is directly dependent on crystal input jitter.

Specifications subject to change without notice.

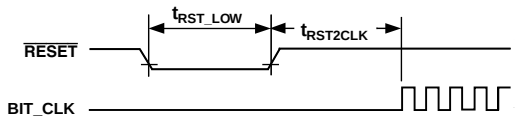


Figure 1. Cold Reset

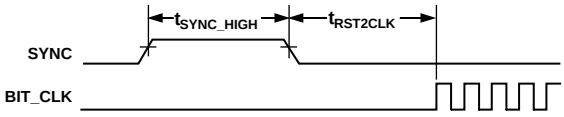


Figure 2. Warm Reset

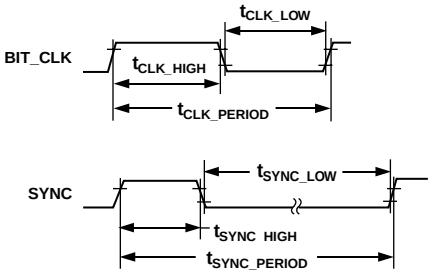


Figure 3. Clock Timing

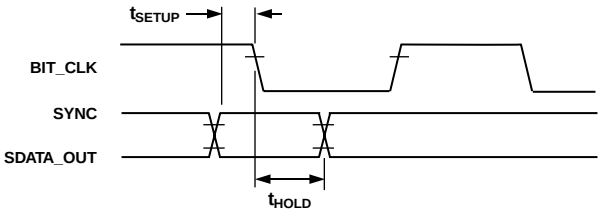


Figure 4. Data Setup and Hold

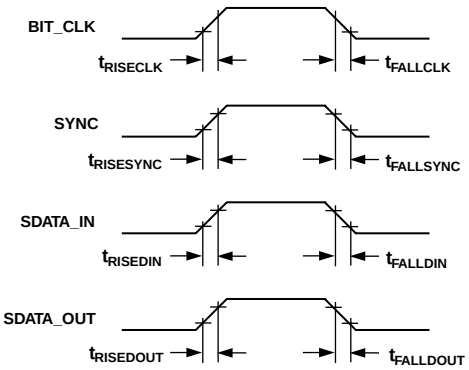


Figure 5. Signal Rise and Fall Time

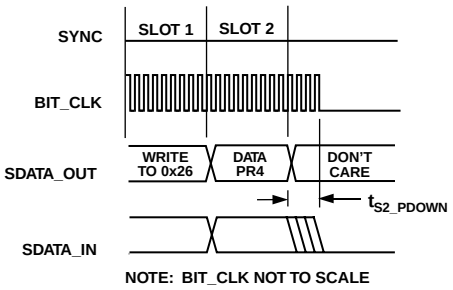


Figure 6. AC Link Low Power Mode Timing

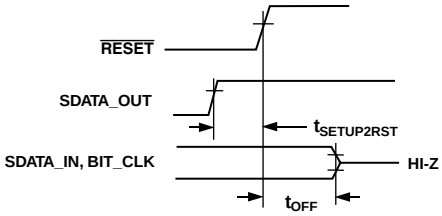


Figure 7. ATE Test Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
Power Supplies			
Digital (DV_{DD})	–0.3	+3.6	V
Analog (AV_{CC})	–0.3	+6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	AV_{DD} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	DV_{DD} + 0.3	V
Ambient Temperature (Operating)	0	70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1886JST	0°C to 70°C	48-Lead TQFP	ST-48

*ST = Thin Quad Flatpack.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} – (P_D \times \theta_{CA})$

T_{CASE} = Case Temperature in °C

P_D = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

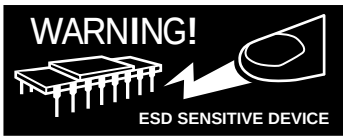
θ_{JA} = Thermal Resistance (Junction-to-Ambient)

θ_{JC} = Thermal Resistance (Junction-to-Case)

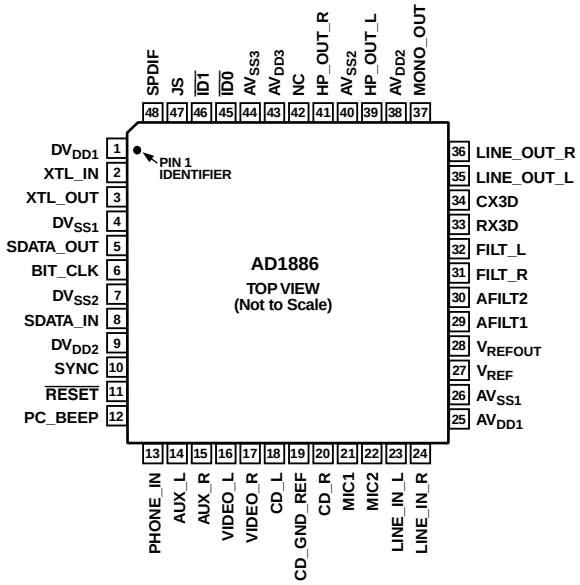
Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	76.2°C/W	17°C/W	59.2°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1886 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Digital I/O

Pin Name	TQFP	I/O	Description
XTL_IN	2	I	Crystal (or Clock) Input, 24.576 MHz.
XTL_OUT	3	O	Crystal Output.
SDATA_OUT	5	I	AC-Link Serial Data Output, AD1886 Input Stream.
BIT_CLK	6	O/I*	AC-Link Bit Clock. 12.288 MHz Serial Data Clock. Daisy Chain Output Clock.
SDATA_IN	8	O	AC-Link Serial Data Input. AD1886 Output Stream.
SYNC	10	I	AC-Link Frame Sync.
$\overline{\text{RESET}}$	11	I	AC-Link Reset. AD1886 Master H/W Reset.
SPDIF	48	O	SPDIF Output

CHIP SELECTS

Pin Name	TQFP	Type	Description
$\overline{\text{ID0}}$	45	I	Chip Select Input 0 (Active Low)
$\overline{\text{ID1}}$	46	I	Chip Select Input 1 (Active Low)

JACK SENSE/GENERAL-PURPOSE DIGITAL OUTPUT

The JS pin can be used to sense the presence of an audio plug in the output jacks and automatically mute the MONO and/or LINE_OUT audio outputs. Alternatively, the JS can be programmed as a general-purpose digital output pin.

Pin Name	TQFP	Type	Description
JS	47	I/O	JACK SENSE input, or GPIO.

Analog I/O

These signals connect the AD1886 component to analog sources and sinks, including microphones and speakers.

Pin Name	TQFP	I/O	Description
PC_BEEP	12	I	PC Beep. PC Speaker beep passthrough.
PHONE	13	I	Phone. From telephony subsystem speakerphone or handset.
AUX_L	14	I	Auxiliary Input Left Channel.
AUX_R	15	I	Auxiliary Input Right Channel.
VIDEO_L	16	I	Video Audio Left Channel.
VIDEO_R	17	I	Video Audio Right Channel.
CD_L	18	I	CD Audio Left Channel.
CD_GND_REF	19	I	CD Audio Analog Ground Reference for Differential CD Input.
CD_ R	20	I	CD Audio Right Channel.
MIC1	21	I	Microphone 1. Desktop microphone input.
MIC2	22	I	Microphone 2. Second microphone input.
LINE_IN_L	23	I	Line in Left Channel.
LINE_IN_R	24	I	Line in Right Channel.
LINE_OUT_L	35	O	Line out Left Channel.
LINE_OUT_R	36	O	Line out Right Channel.
MONO_OUT	37	O	Monaural Output to telephony subsystem speakerphone.
HP_OUT_L	39	O	Headphones out Left Channel.
HP_OUT_R	41	O	Headphones out Right Channel.

Filter/Reference

These signals are connected to resistors, capacitors, or specific voltages.

Pin Name	TQFP	I/O	Description
V_{REF}	27	O	Voltage Reference Filter.
V_{REFOUT}	28	O	Voltage Reference Output 5 mA Drive (Intended for Mic Bias).
AFILT1	29	O	Antialiasing Filter Capacitor—ADC Right Channel.
AFLIT2	30	O	Antialiasing Filter Capacitor—ADC Left Channel.
FILT_R	31	O	AC-Coupling Filter Capacitor—ADC Right Channel.
FILT_L	32	O	AC-Coupling Filter Capacitor—ADC Left Channel.
RX3D	33	O	3D Phat Stereo Enhancement—Resistor.
CX3D	34	I	3D Phat Stereo Enhancement—Capacitor.

Power and Ground Signals

Pin Name	TQFP	Type	Description
$DV_{DD}1$	1	I	Digital V_{DD} 3.3 V
$DV_{SS}1$	4	I	Digital GND
$DV_{SS}2$	7	I	Digital GND
$DV_{DD}2$	9	I	Digital V_{DD} 3.3 V
$AV_{DD}1$	25	I	Analog V_{DD} 5.0 V
$AV_{SS}1$	26	I	Analog GND
$AV_{DD}2$	38	I	Analog V_{DD} 5.0 V
$AV_{SS}2$	40	I	Analog GND
$AV_{DD}3$	43	I	Analog V_{DD} 5.0 V
$AV_{SS}3$	44	I	Analog GND

No Connects

Pin Name	TQFP	Type	Description
NC	42		No Connect

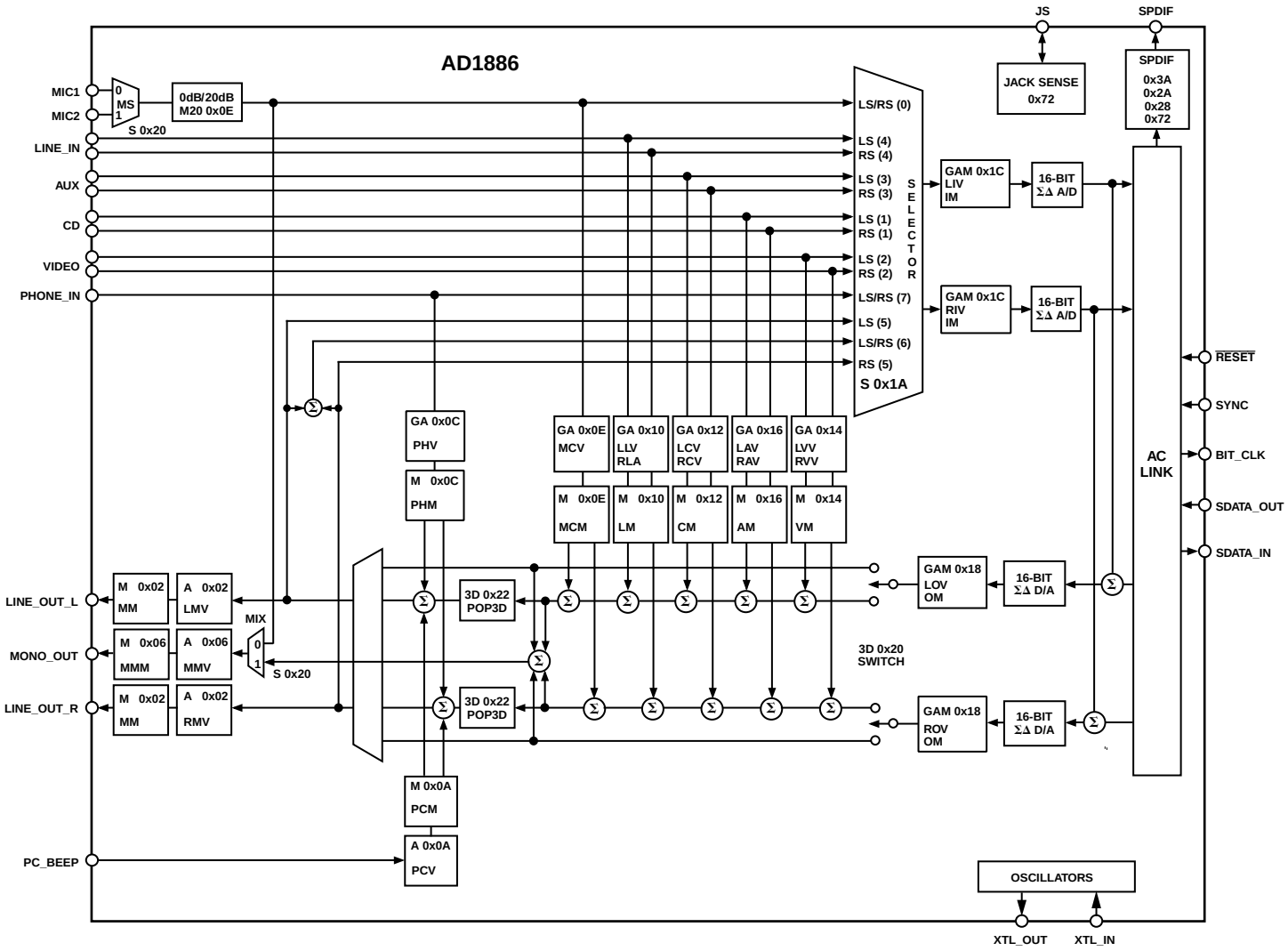


Figure 8. Block Diagram Register Map

Indexed Control Registers

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0410h
02h	Master Volume	MM	X	LMV 5	LMV 4	LMV 3	LMV 2	LMV 1	LMV 0	X	X	RMV 5	RMV 4	RMV 3	RMV 2	RMV 1	RMV0 0	8000h
04h	Headphones Volume	HPM	X	LHV 5	LHV 4	LHV 3	LHV 2	LHV 1	LHV 0	X	X	RHV 5	RHV 4	RHV 3	RHV 2	RHV 1	RHV 0	8000h
06h	Master Volume Mono	MMM	X	X	X	X	X	X	X	X	X	X	MMV 4	MMV 3	MMV 2	MMV 1	MMV 0	8000h
08h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0Ah	PC Beep Volume	PCM	X	X	X	X	X	X	X	X	X	X	PCV3	PCV2	PCV1	PCV0	X	8000h
0Ch	Phone-In Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV 4	PHV 3	PHV 2	PHV 1	PHV 0	8008h
0Eh	Mic Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV 4	MCV 3	MCV 2	MCV 1	MCV 0	8008h
10h	Line-In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	X	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h
12h	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	X	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h
14h	Video Volume	VM	X	X	LVV4	LVV3	LVV2	LVV1	LVV0	X	X	X	RVV4	RVV3	RVV2	RVV1	RVV0	8808h
16h	Aux Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	X	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	8808h
18h	PCM Out Vol	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	X	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	X	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h
20h	General-Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
26h	Power-Down Ctrl/Stat	X	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
28h	Ext'd Audio ID	$\overline{ID1}$	$\overline{ID0}$	X	X	X	X	X	X	X	X	X	X	X	SPDF	X	VRA	0005h
2Ah	Ext'd Audio Stat/Ctrl	X	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0000h
2Ch/ (7Ah)*	PCM DAC Rate (SR1)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h/ (78h)*	PCM ADC Rate (SR0)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ah	SPDIF Control	V	X	SPSR 1	SPSR 0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUD	PRO	0000h
72h	Jack Sense/SPDIF	X	JSOD	X	JSPD	X	JSOE	JSLM	JSD	X	JSC	JSMM	JSM	VWI	JS1	JS0	JSI	0000h
74h	Serial Configuration	SLOT 16	REG M2	REG M1	REG M0	DRQ EN	DLR Q2	DLR Q1	DLR Q0	X	X	X	X	X	DRR Q2	DRR Q1	DRR Q0	7X0Xh
76h	Misc Control Bits	DAC Z	LPMI X	X	DAM	DMS	DLSR	X	ALSR	MOD EN	SRX1 0D7	SRX8 D7	X	X	DRSR	X	ARSR	0404h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5361h

NOTES
All registers not shown and bits containing an X are assumed to be reserved.
Odd register addresses are aliased to the next lower even address.
Reserved registers should not be written.
Zeros should be written to reserved bits.
*Indicates Aliased register for AD1819, AD1819A backward compatibility

AD1886

Reset (Index 00h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0400h

Note: Writing any value to this register performs a register reset, which causes all registers to revert to their default values (except 74h, which forces the serial configuration). Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement.

ID[9:0] Identify Capability. The ID decodes the capabilities of AD1886 based on the following:

Bit = 1	Function	AD1886*
ID0	Dedicated Mic PCM in Channel	0
ID1	Modem Line Codec support	0
ID2	Bass and Treble Control	0
ID3	Simulated Stereo (Mono to Stereo)	0
ID4	Headphone Out Support	0
ID5	Loudness (Bass Boost) Support	0
ID6	18-Bit DAC Resolution	0
ID7	20-Bit DAC Resolution	0
ID8	18-Bit ADC Resolution	0
ID9	20-Bit ADC Resolution	0

*The AD1886 contains none of the optional features identified by these bits.

SE[4:0] Stereo Enhancement. The 3D stereo enhancement identifies the Analog Devices 3D stereo enhancement.

Master Volume Registers (Index 02h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Master Volume	MM	X	LMV5	LMV4	LMV3	LMV2	LMV1	LMV0	X	X	RMV5	RMV4	RMV3	RMV2	RMV1	RMV0	8000h

RMV[5:0] Right Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –94.5 dB.

LMV[5:0] Left Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –94.5 dB.

MM Master Volume Mute. When this bit is set to "1," the channel is muted.

MM	xMV5 . . . xMV0	Function
0	00 0000	0 dB Attenuation
0	01 1111	–46.5 dB Attenuation
0	11 1111	–94.5 dB Attenuation
1	xx xxxx	–∞ dB Attenuation

Headphones Volume Registers (Index 04h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Headphones Volume	HPM	X	LHV5	LHV4	LHV3	LHV2	LHV1	LHV0	X	X	RHV5	RHV4	RHV3	RHV2	RHV1	RHV0	8000h

RHV[5:0] Right Headphone Volume Control. The least significant bit represents 1.5 dB. This register controls the output from +6 dB to a maximum attenuation of –88.5 dB.

LHV[5:0] Left Headphone Volume Control. The least significant bit represents 1.5 dB. This register controls the output from +6 dB to a maximum attenuation of –88.5 dB.

HPM Headphones Volume Mute. When this bit is set to "1," the channel is muted.

HPM	xHV5 . . . xHV0	Function
0	00 0000	6 dB Gain
0	01 1111	–40.5 dB Attenuation
0	11 1111	–88.5 dB Attenuation
1	xx xxxx	–∞ dB Attenuation

Master Volume Mono (Index 06h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	Master Volume Mono	MMM	X	X	X	X	X	X	X	X	X	MMV5	MMV4	MMV3	MMV2	MMV1	MMV0	8000h

MMV[5:0] Mono Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –94.5 dB.

MMM Mono Master Volume Mute. When this bit is set to "1," the channel is muted.

PC Beep Register (Index 0Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	PC_BEEP Volume	PCM	X	X	X	X	X	X	X	X	X	X	PCV3	PCV2	PCV1	PCV0	X	8000h

PCV[3:0] PC Beep Volume Control. The least significant bit represents 3 dB attenuation. This register controls the output from 0 dB to a maximum attenuation of –45 dB. The PC Beep is routed to Left and Right Line outputs even when AD1886 is in a $\overline{\text{RESET}}$ State. This is so Power-On Self-Test (POST) codes can be heard by the user in case of a hardware problem with the PC.

PCM PC Beep Mute. When this bit is set to "1," the channel is muted.

PCM	PCV3 . . . PCV0	Function
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

Phone Volume (Index 0Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	Phone Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV4	PHV3	PHV2	PHV1	PHV0	8008h

PHV[4:0] Phone Volume. Allows setting the Phone Volume Attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

PHM Phone Mute. When this bit is set to "1," the channel is muted.

Mic Volume (Index 0Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	MIC Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h

MCV[4:0] Mic Volume Gain. Allows setting the Mic Volume attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

M20 Microphone 20 dB Gain Block
0 = Disabled; Gain = 0 dB
1 = Enabled; Gain = 20 dB

MCM Mic Mute. When this bit is set to "1," the channel is muted.

Line In Volume (Index 10h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	X	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h

RLV[4:0] Right Line In Volume. Allows setting the Line In right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LLV[4:0] Line In Volume Left. Allows setting the Line In left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LM Line In Mute. When this bit is set to "1," the channel is muted.

CD Volume (Index 12h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	X	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h

RCV[4:0] Right CD Volume. Allows setting the CD right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LCV[4:0] Left CD Volume. Allows setting the CD left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

CVM CD Volume Mute. When this bit is set to "1," the channel is muted.

Video Volume (Index 14h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	Video Volume	VM	X	X	LVV4	LVV3	LVV2	LVV1	LVV0	X	X	X	RVV4	RVV3	RVV2	RVV1	RVV0	8808h

RVV[4:0] Right Video Volume. Allows setting the Video right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LVV[4:0] Left Video Volume. Allows setting the Video left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

VM Video Mute. When this bit is set to "1," the channel is muted.

AUX Volume (Index 16h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	Aux Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	X	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	8808h

RAV[4:0] Right Aux Volume. Allows setting the Aux right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LAV[4:0] Left Aux Volume. Allows setting the Aux left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

AM Aux. Mute. When this bit is set to "1," the channel is muted.

PCM Out Volume (Index 18h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Out Volume	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	X	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h

ROV[4:0] Right PCM Out Volume. Allows setting the PCM right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LOV[4:0] Left PCM Out Volume. Allows setting the PCM left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

OM PCM Out Volume Mute. When this bit is set to "1," the channel is muted.

Volume Table (Index 0Ch to 18h)

Mute	x4 . . . x0	Function
0	00000	+12 dB Gain
0	01000	0 dB Gain
0	11111	–34.5 dB Gain
1	xxxxx	–∞ dB Gain

AD1886

Record Select Control Register (Index 1Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h

RS[2:0] Right Record Select

LS[2:0] Right Record Select.

Used to select the record source independently for right and left. See table for legend.

The default value is 0000h, which corresponds to Mic in.

RS2 . . . RS0	Right Record Source
0	MIC
1	CD_R
2	VIDEO_R
3	AUX_R
4	LINE_IN_R
5	Stereo Mix (R)
6	Mono Mix
7	PHONE_IN

LS2 . . . LS0	Left Record Source
0	MIC
1	CD_L
2	VIDEO_L
3	AUX_L
4	LINE_IN_L
5	Stereo Mix (L)
6	Mono Mix
7	PHONE_IN

Record Gain (Index 1Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	X	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h

RIM[3:0] Right Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB and the range is 0 dB to +22.5 dB.

LIM[3:0] Left Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB and the range is 0 dB to +22.5 dB.

IM Input Mute.
0 = Unmuted,
1 = Muted or –∞ dB gain.

IM	xIM3 . . . xIM0	Function
0	1111	+22.5 dB Gain
0	0000	0 dB Gain
1	xxxxx	–∞ dB Gain

General Purpose Register (Index 20h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General-Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h

Note: This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h, which is all off.

LPBK Loopback Control. ADC/DAC digital loopback mode.

MS Mic Select
0 = Mic1
1 = Mic2

MIX Mono Output Select
0 = Mix
1 = Mic

3D 3D Phat Stereo Enhancement
0 = Phat Stereo is off.
1 = Phat Stereo is on.

POP PCM Output Path and Mute. The POP bit controls the optional PCM out 3D bypass path (the pre and post 3D PCM out paths are mutually exclusive).
0 = pre 3D.
1 = post 3D.

3D Control Register (Index 22h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h

DP[2:0] Depth Control. Sets 3D “Depth” Phat Stereo enhancement according to table below.

DP3 . . . DP0	Depth
0	0%
1	6.67%
.	.
.	.
14	93.33%
15	100%

Subsection Ready Register (Index 26h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Power-Down Cntrl/Stat	X	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	NA

Note: The ready bits are read only, writing to REF, ANL, DAC, ADC will have no effect. These bits indicate the status for the AD1886 subsections. If the bit is a one, that subsection is "ready." Ready is defined as the subsection able to perform in its nominal state.

ADC ADC section ready to transmit data.

DAC DAC section ready to accept data.

ANL Analog gainuators, attenuators, and mixers ready.

REF Voltage References, V_{REF} and V_{REFOUT} up to nominal level.

PR[5:0] AD1886 Power-Down Modes. The first three bits are to be used individually rather than in combination with each other. The last bit, PR3, can be used in combination with PR2 or by itself. The mixer and reference cannot be powered down via PR3 unless the ADCs and DACs are also powered down. Nothing else can be powered up until the reference is up.

PR5 has no effect unless all ADCs, DACs, and the AC-Link are powered down. The reference and the mixer can be either up or down, but all power-up sequences must be allowed to run to completion before PR5 and PR4 are both set.

In multiple-codec systems, the master codec's PR5 and PR4 bits control the slave codec. PR5 is also effective in the slave codec if the master's PR5 bit is clear, but the PR4 bit has no effect except to enable or disable PR5.

Power-Down State	Set Bits
ADCs and Input Mux Power-Down	PR0
DACs Power-Down	PR1
Analog Mixer Power-Down (V_{REF} and V_{REFOUT} On)	PR1, PR2
Analog Mixer Power-Down (V_{REF} and V_{REFOUT} OZff)	PR0, PR1, PR3
AC-Link Interface Power-Down	PR4
Internal Clocks Disabled	PR0, PR1, PR4, PR5
ADC and DAC Power-Down	PR0, PR1
V_{REF} Standby Mode	PR0, PR1, PR2, PR4, PR5
Total Power-Down	PR0, PR1, PR2, PR3, PR4, PR5

Extended Audio ID Register (Index 28h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0001h

Note: The Extended Audio ID is a read only register.

VRA Variable Rate Audio. VRA = 1 indicates support for Variable Rate Audio.

SPDF "1" indicates SPDIF support, "0" indicates no SPDIF support.

ID[1:0] ID1, ID0 is a 2-bit field which indicates the codec configuration: Primary is 00; Secondary is 01, 10, or 11.

Extended Audio Status and Control Register (Index 2Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Ext'd Audio Stat/Ctrl	X	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0000h

Note: The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

VRA — Variable Rate Audio. VRA = 1 indicates support for Variable Rate Audio mode (sample rate control registers and SLOTREQ signaling.

SPDIF — SPDIF transmitter subsystem enable/disable bit:
"1" indicates SPDIF is enabled, "0" indicates SPDIF is disabled.

SPSA[1,0] — SPDIF Slot Assignment:
SPSA[1, 0] = 00 SPDIF uses AC-LINK slots 3 and 4.
SPSA[1, 0] = 01 SPDIF uses AC-LINK slots 7 and 8.
SPSA[1, 0] = 10 SPDIF uses AC-LINK slots 6 and 9.
SPSA[1, 0] = 11 Reserved.

SPCV — SPDIF Configuration Valid: (Read Only)
"1" indicates current SPDIF configuration (SPA, SPR, DAC-Rate) is supported.
"0" indicates current SPDIF configuration (SPA, SPR, DAC-Rate) is not supported

PCM DAC Rate Register (Index 2Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch/(7Ah)	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Note: 2Ch is an alias for 7Ah. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA, both sample rates are reset to 48 kHz.

SR[15:0] — Writing to this register allows programming of the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. Programming a value outside of the range 7040 Hz (1b80h) to 48000 Hz (bb80h) causes the codec to saturate. For all rates, if the value written to the register is supported, that value will be echoed back when read, otherwise the closest rate supported is returned.

PCM ADC Rate Register (Index 32h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h/(78h)	PCM ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Note: 32h is an alias for 78h. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR[15:0] — Writing to this register allows programming of the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. Programming a value outside of the range 7040 Hz (1b80h) to 48000 Hz (bb80h) causes the codec to saturate. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest rate supported is returned.

SPDIF Control Register (Index 3Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ah	SPDIF Control	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	$\overline{AUD}$	PRO	0000h

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit in register 2Ah is "0"). This ensures that control and status information startup correctly at the beginning of SPDIF transmission.

PRO — Professional: "1" indicates Professional use of channel status, "0" Consumer.

$\overline{AUD}$ — Non-Audio: "1" indicates data is non PCM format, "0" data is PCM.

COPY — Copyright: "1" indicates copyright is asserted, "0" copyright is not asserted.

PRE — Preemphasis: "1" indicates filter preemphasis is 50/15 µs, "0" preemphasis is none.

CC[6-0] — Category Code: Programmed according to IEC standards, or as appropriate.

L — Generation Level: Programmed according to IEC standards, or as appropriate.

SPSR[1,0] — SPDIF Transmit Sample Rate:
SPSR[1:0] = "00" Transmit Sample Rate = 44.1 kHz.
SPSR[1:0] = "01" Reserved.
SPSR[1:0] = "10" Transmit Sample Rate = 48 kHz.
SPSR[1:0] = "11" Not supported.

V — Validity: This bit affects the "Validity flag," bit <28> transmitted in each subframe and enables the SPDIF transmitter to maintain connection during error or mute conditions.
V = 1 Each SPDIF subframe (L + R) has bit <28> set to "1." This tags both samples as invalid.
V = 0 Each SPDIF subframe (L + R) has bit <28> set to "0" for valid data and "1" for invalid data (error condition).

Jack Sense/SPDIF Register (Index 72h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
72h	Jack Sense/SPDIF	X	JS0D	X	JSPD	X	JSOE	JSLM	JSD	X	JSC	JSMM	JSM	VW1	JS1	JS0	JS1	0000h

Note: All register bits are *read/write* except for JSI, JSO, JS1 and VWI, which are read only.

JSI — Indicates that Jack Sense pin has generated an interrupt. Must be enabled by JSM bit and remains set until software clears JSC bit.

JS0 — Reflects JS0 pin state.

JS1 — Reflects JS1 pin state.

VWI — Indicates Voice Wake Interrupt occurred.

JSM — Jack Sense Mode:
1 = Interrupt Mode (Software intervention required).
0 = Jack Sense Mode (Hardware asserted Mono/Line Muting).

JSMM — Jack Sense Mono Mute:
Setting this bit enables Jack Sense to mute the Mono output.

JSC — Jack Sense Clear:
Setting this bit clears the Jack Sense interrupt (only needed when JSM = 1)

JSD — Jack Sense Disabled:
Setting this bit disables Jack Sense functionality.

JSLM — Jack Sense Line Mute:
Setting this bit enables Jack Sense to mute the LINE_OUT output.

JSOE — Jack Sense Output Enable:
Setting this bit allows the JS pin to operate as GPIO (output mode only).

JSPD — Jack Sense Pull-up Disable:
Setting this bit disables the internal Jack Sense pull-up.

JSOD — Jack Sense Output Data:
Data on this bit is transferred to the JS pin if JSOE = 1 (otherwise no effect).

Serial Configuration (Index 74h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
74h	Serial Configuration	SLOT 16	REGM2	REGM1	REGM0	X	X	DHWR	X	X	X	X	X	X	X	X	X	X

Note: This register is not reset when the reset register (Register 00h) is written.

DHWR Disable Hardware Reset.

REGM0 Master Codec register mask.

REGM1 Slave 1 Codec register mask.

REGM2 Slave 2 Codec register mask.

SLOT16 Enable 16-bit slots.

If your system uses only a single AD1886, you can ignore the register mask bits.

SLOT16 makes all AC Link slots 16 bits in length, formatted into 16 slots.

Miscellaneous Control Bits (Index 76h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
76h	Misc Control Bits	DACZ	LPMIX	X	DAM	DMS	DLSR	X	ALSR	MODEN	SRX10D7	SRX8D7	X	X	DRSR	X	ARSR	0000h

ARSR ADC right sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

DRSR DAC right sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

SRX8D7 Multiply SR1 rate by 8/7.

SRX10D7 Multiply SR1 rate by 10/7. SRX10D7 and SRX8D7 are mutually exclusive; SRX10D7 has priority if both are set.

MODEN Modem filter enable (left channel only). Change only when DACs are powered down.

ALSR ADC left sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

DLSR DAC left sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch) .

DMS Digital Mono Select.
0 = Mixer
1 = Left DAC + Right DAC .

DAM Digital Audio Mode. DAC Outputs bypass analog mixer and sent directly to the codec output.

LPMIX Low-Power Mixer.

DACZ Zero-fill (vs. repeat) if DAC is starved for data.

Sample Rate 0 (Index 78h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
(32h)/78h	Sample Rate 0	SR015	SR014	SR013	SR012	SR011	SR010	SR09	SR08	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00	BB80h

Note: 32h is an alias for 78h. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR0[15:0] Writing to this register allows the user to program the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hertz increments. Programming a value greater than 48 kHz or less than 7 kHz may cause unpredictable results.

Sample Rate 1 (Index 7Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
(2Ch)/7Ah	Sample Rate 1	SR115	SR114	SR113	SR112	SR111	SR110	SR19	SR18	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10	BB80h

Note: 2Ch is an alias for 7Ah. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR1[15:0] Writing to this register allows the user to program the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hertz increments. Programming a value greater than 48 kHz or less than 7 kHz may cause unpredictable results.

Vendor ID Registers (Index 7Ch–7Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h

S[7:0] This register is ASCII encoded to ‘A.’

F[7:0] This register is ASCII encoded to ‘D.’

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5361h

T[7:0] This register is ASCII encoded to ‘S.’

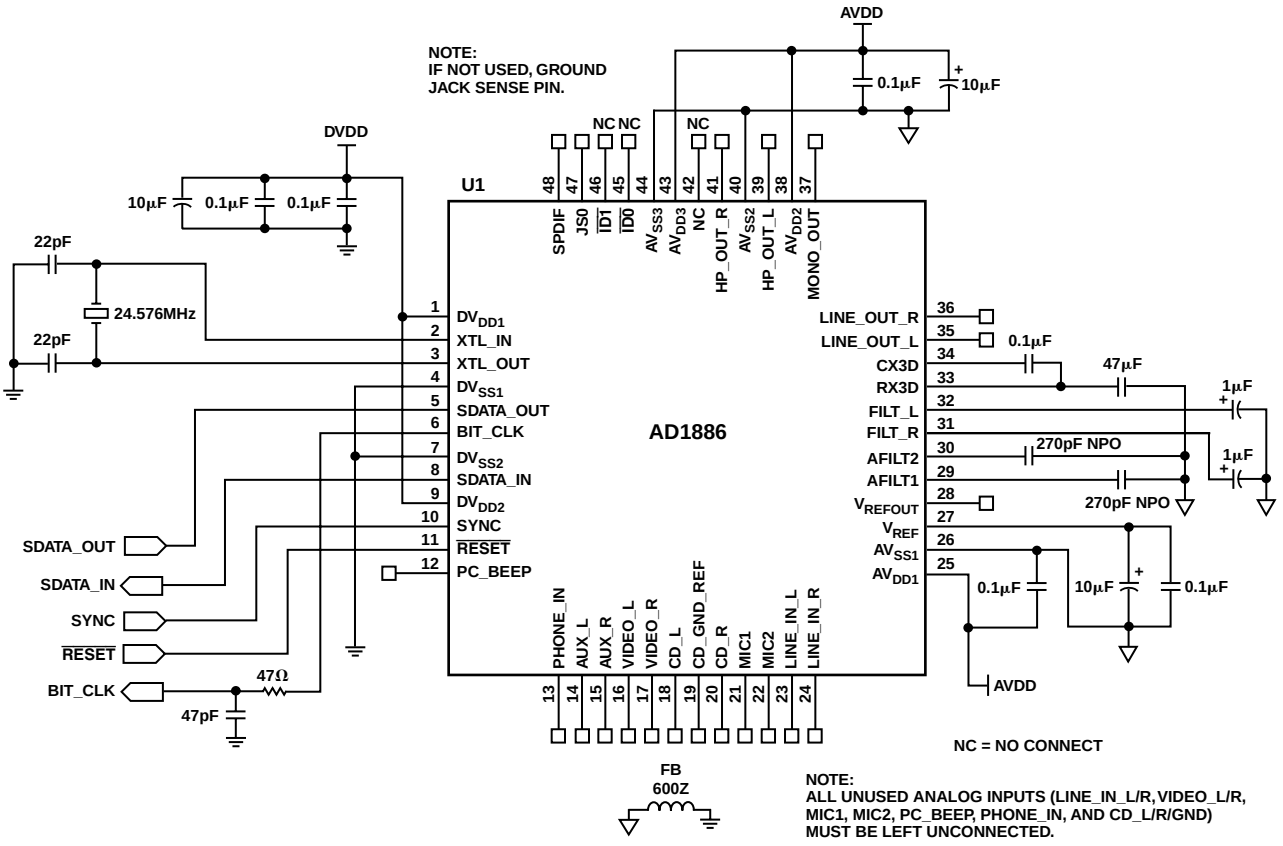


Figure 9. Recommended Power Connections, Decoupling and Support Components

S/PDIF TRANSMITTER OUTPUT CONNECTION

The codec S/PDIF output is located on Pin 48. This pin has a weak internal pull-up that allows detection of S/PDIF connector hardware at power-up and automatically enables or disables the S/PDIF transmitter. This feature allows system manufacturers to populate or depopulate S/PDIF connector hardware according to their requirements.

When the output pin is simply left open (NC) or strapped high by a pull-up resistor, the internal sense circuitry disables the S/PDIF transmitter. This condition prevents the S/PDIF enable bit on Register 2Ah from being enabled.

When the output pin is strapped low by a pull-down resistor (10 kΩ or less), the S/PDIF transmitter is enabled and the S/PDIF enable bit on Register 2Ah can be asserted.

The following circuits (Figure 10 and Figure 11) describe two ways to provide an S/PDIF connection to the codec.

The first option consists of an optical link using a TOSLINK fiber-optic transmitting module. A typical offering is the TOSHIBA TOTX173 module for PCB mounted applications. This module can drive fiber optic cables up to 10 meters long, depending on the cable hardware used. This solution offers compatibility with state of the art audio systems and provides excellent common-mode rejection and noise immunity. R1 sets the current level for the internal LED and R2 allows the S/PDIF transmitter to be enabled at power-up. Note that the TOSLINK module requires V_{CC} = 5 V (PC logic supply).

The second method uses an electrical connection matching the requirements of the IEC958 "Digital Audio Interface" for consumer products. This method uses a 75 Ω coax cable as the connecting medium, with RCA type connectors at both ends. The transmission distance is at least 10 to 15 meters depending on the hardware used. The nominal electrical levels are 0.5 V p-p with a required bandwidth of 7 MHz. The 1:1 ratio transformer is used for galvanic isolation and for improved common-mode noise rejection. R1 and R2 provide the proper signal amplitude and impedance matching. R3 allows the S/PDIF transmitter to be enabled at power-up.

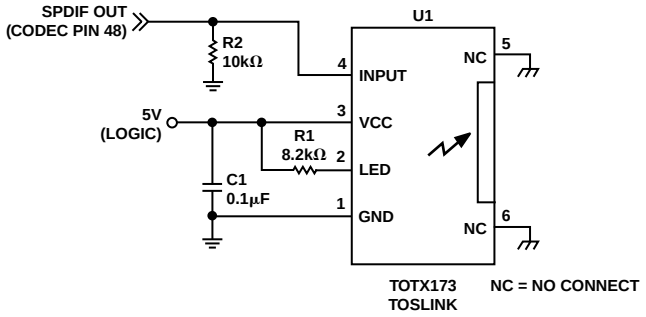


Figure 10. S/PDIF Output Connection Using Optical Link

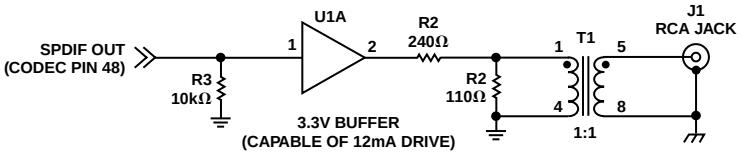


Figure 11. S/PDIF Output Connection Using Electrical Link

JACK SENSE OPERATION

The AD1886 features a Jack Sense pin (JS) that can be used with the HP_OUT or LINE_OUT jacks to automatically mute the other audio outputs. When the Jack Sense pin is connected to one of the output jacks, the AD1886 can sense whether an audio plug has been inserted into the jack and automatically mute the LINE_OUT or MONO_OUT or both outputs.

The JS pin should normally be connected to the HP_OUT jack to automatically mute the MONO_OUT and LINE_OUT audio signals, alternatively the JS pin can be connected to the LINE_OUT jack to automatically mute the MONO_OUT signal. The action of the JS pin can be programmed by setting the JSLM and JSMM bits in the Jack Sense Register (72h). The following table summarizes the Jack Sense operation:

Table I. Jack Sense Operation Table

JSLM Bit (Reg 72h, D9 Bit)	JSMM Bit (Reg 72h, D5 Bit)	JS State = HIGH (PLUG INSERTED)	JS State = LOW (PLUG REMOVED)
0	0	LINE_OUT = ON MONO_OUT = ON	LINE_OUT = ON MONO_OUT = ON
0	1	LINE_OUT = ON MONO_OUT = MUTE	LINE_OUT = ON MONO_OUT = ON
1	0	LINE_OUT = MUTE MONO_OUT = ON	LINE_OUT = ON MONO_OUT = ON
1	1	LINE_OUT = MUTE MONO_OUT = MUTE	LINE_OUT = ON MONO_OUT = ON

The Jack Sense functionality is enabled by default on codec power-up (JSD bit = 0), however the JSLM and JSMM bits are set to zero, therefore the muting action is not enabled for both outputs. The JSLM and JSMM bits have to be configured by the software or INF configuration file for the desired muting action.

The Jack Sense pin is active high and contains an active internal pull-up. If the Jack Sense input is not going to be used, it should be pulled down to digital ground using 10 kΩ resistors.

CONNECTING THE JACK SENSE TO THE OUTPUT JACKS

Headphone Jack

The diagram on Figure 12 shows the preferred method to connect the Jack Sense line to the HP_OUT jack. This scheme requires a stereo jack with a normally closed and isolated single switch. The switch holds the Jack Sense line low (grounded) until an audio plug is inserted, causing the switch to open and the Jack Sense line to go high due to the codec internal pull-up.

The R2 and R3 resistors keep the electrolytic output caps properly polarized while the HP_OUT jack is not used.

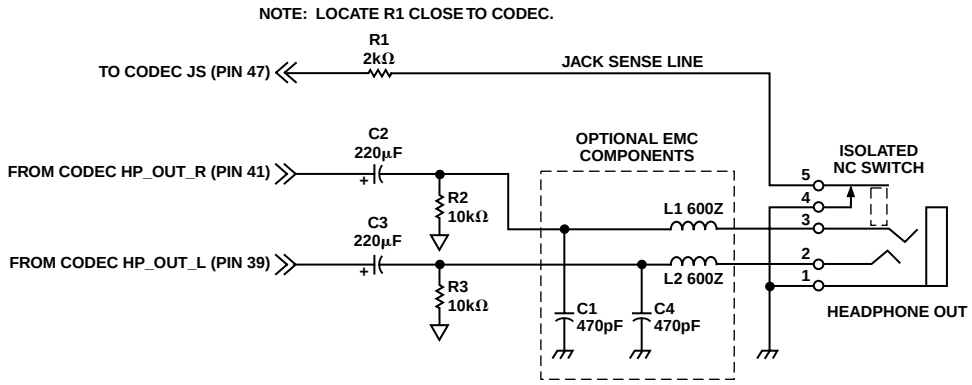


Figure 12. Jack Sense Connection to HP_OUT Jack, Using Isolated Switch

Alternatively, when an audio output jack containing an isolated switch is not available, the circuit shown in Figure 13 can be used. While the audio plug is out, this circuit keeps the Jack Sense line state low, by the pull-down affect of R2 (with no audio present) or by tracking the lower peaks of the HP_OUT audio signal. Once an audio plug is inserted and the jack switch opens, the Jack Sense line switches to a high state due to the codec internal pull-up, which quickly charges C1 to DV_{DD}.

The R2 and R3 resistors also keep the electrolytic output caps properly polarized while the HP_OUT jack is not used.

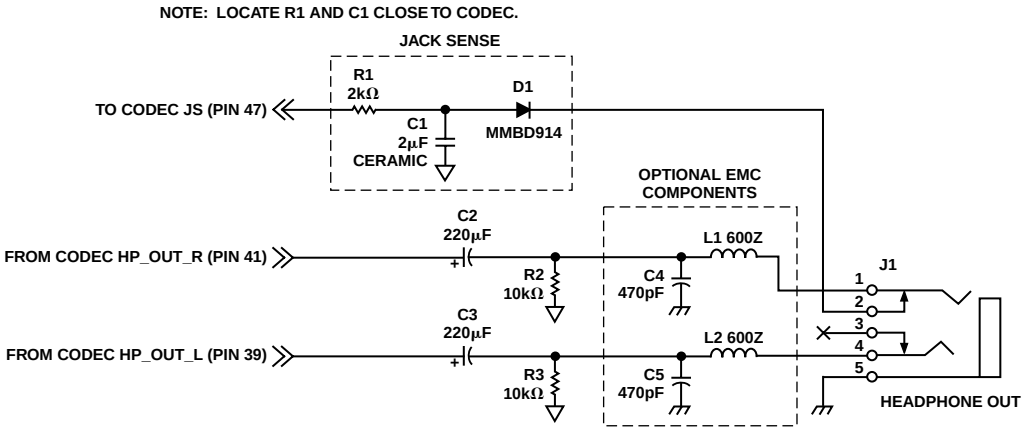


Figure 13. Jack Sense Connection to HP_OUT Jack, Using Nonisolated Switch

LINE OUT JACK

Although not shown, if a LINE_OUT jack is used and the Jack Sense functionality is desired with this jack, the LINE_OUT jack should be wired in a similar configuration as shown above for the HP_OUT jack (preferably Figure 12). We recommend that in this case the output coupling caps (C2, C3) be set to 2.2 μF. All other values should be kept the same.

APPLICATION CIRCUITS

CD-ROM CONNECTIONS

Typical CD-ROM drives generate 2 V rms output and require a voltage divider for compatibility with the Codec input (1 V rms range). The recommended circuit is a group of divide-by-two voltage dividers as shown on Figure 14.

The CD_GND_REF pin is used to cancel differential ground noise from the CD-ROM. For optimal noise cancellation, this section of the divider should have approximately half the impedance of the Right and Left channel section dividers.

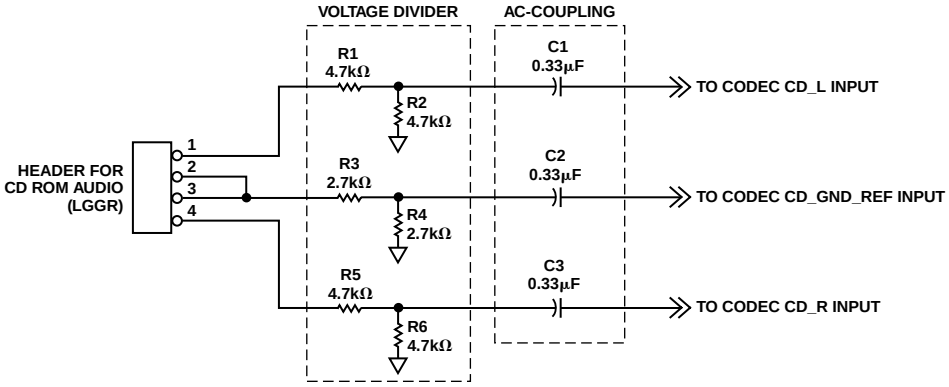


Figure 14. Typical CD-ROM Audio Connections

LINE_IN, AUX, AND VIDEO INPUT CONNECTIONS

Most audio sources also generate 2 V rms audio level and require a –6 dB input voltage divider to be compatible with the Codec inputs. Figure 15 shows the recommended application circuit. For applications requiring EMC compliance, the EMC components should be configured and selected to provide adequate RF immunity and emissions control.

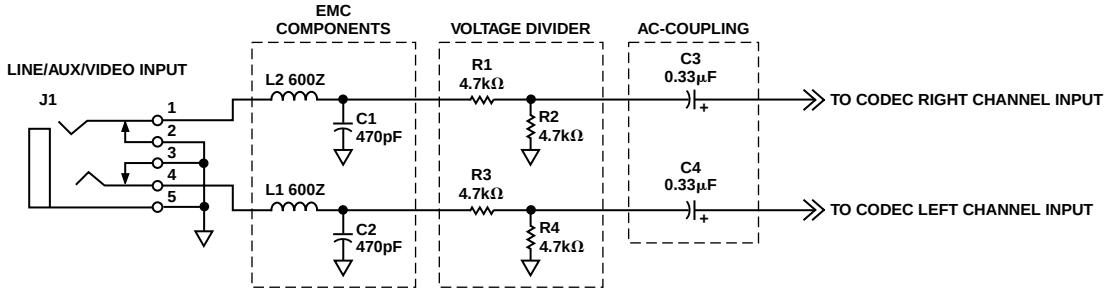


Figure 15. LINE_IN, AUX and VIDEO Input Connections

MICROPHONE CONNECTIONS

The AD1886 contains an internal microphone preamp with 20 dB gain; in most cases a direct microphone connection as shown in Figure 16 is adequate. If the microphone level is too low, an external preamp can be added as shown in Figure 17. In either case the microphone bias can be derived from the codec's internal reference (V_{REFOUT}) using a 2.2 kΩ resistor. For the preamp circuit, the V_{REFOUT} signal can also provide the midpoint bias for the amplifier.

To meet the PC99 1.0A requirements, the MIC signal should be placed on the microphone jack tip and the bias on the ring. This configuration supports electret microphones with three conductor plugs as well as dynamic microphones with two conductor plugs (ring and sleeve shorted together).

Additional filtering may be required to limit the microphone response to the audio band of interest.

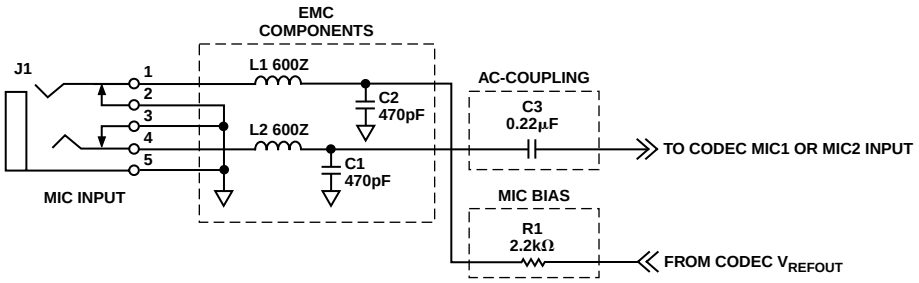


Figure 16. Recommended Microphone Input Connections

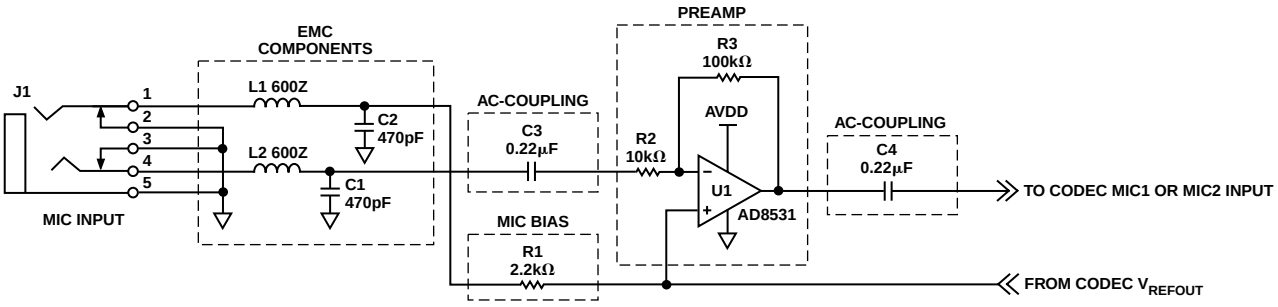


Figure 17. Microphone with Additional External Preamp (20 dB Gain)

LINE OUTPUT CONNECTIONS

The AD1886 Codec provides stereo LINE_OUT signals at a standard 1 V rms level. These signals must be ac-coupled before they can be connected to an external load. After the ac-coupling, a minimal resistive load is recommended to keep the capacitors properly biased and reduce clicks and pops when plugging stereo equipment into the output jack. The capacitor values should be selected to provide a desired frequency response, taking into account the nominal impedance of the external load. To meet the PC99 specification for PCs, testing must be performed with a 10 kΩ load, therefore a minimum of 1 µF value is recommended to achieve less than –3 dB roll-off at 20 Hz.

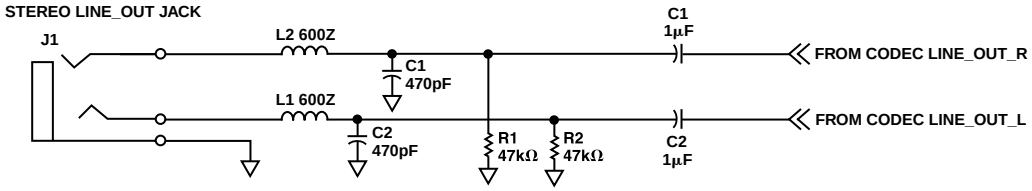


Figure 18. Recommended LINE_OUT Connections

PC BEEP INPUT CONNECTIONS

The recommended PC BEEP input circuit is shown below. Under most cases the PC_BEEP signal should be attenuated, filtered and then ac-coupled into the Codec.

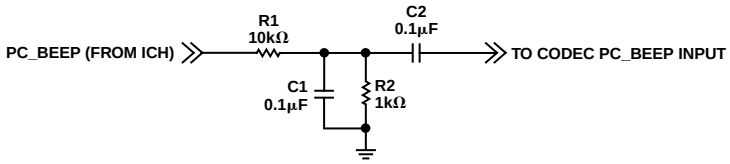
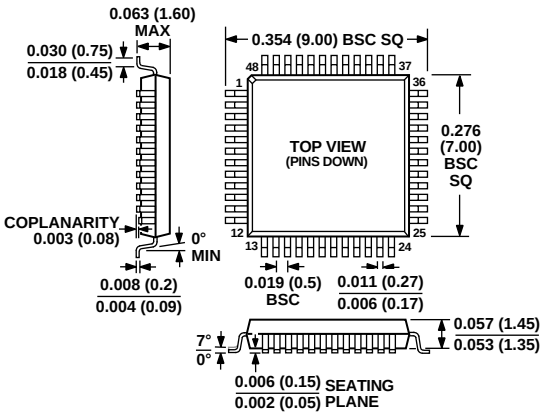


Figure 19. Recommended PC_BEEP Connections

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Thin Plastic Quad Flatpack (LQFP)
(ST-48)



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