ACT–F128K32 High Speed
4 Megabit FLASH Multichip Module

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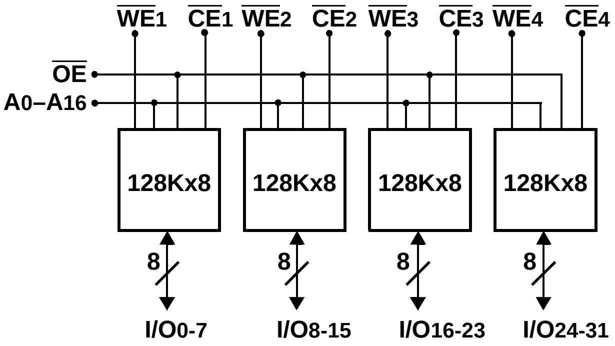
Features

- 4 Low Power 128K x 8 FLASH Die in One MCM Package
- Organized as 128K x 32
  - User Configurable to 256K x 16 or 512K x 8
  - Upgradable to 512K x 32 in same Package Style
- Access Times of 60, 70, 90, 120 and 150ns
- +5V Programing, 5V ±10% Supply
- 100,000 Erase/Program Cycles Typical, 0°C to +70°C
- Low Standby Current
- TTL Compatible Inputs and CMOS Outputs
- Embedded Erase and Program Algorithms
- Page Program Operation and Internal Program Control Time
- Commercial, Industrial and Military Temperature Ranges
- MIL-PRF-38534 Compliant MCMs Available
- Industry Standard Pinouts
- Packaging – Hermetic Ceramic
  - 68 Lead, .88" x .88" x .160" Single-Cavity Small Outline gull wing, Aeroflex code# "F5" *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 66 Pin, 1.08" x 1.08" x .160" PGA Type, No Shoulder, Aeroflex code# "P3"
  - 66 Pin, 1.08" x 1.08" x .185" PGA Type, With Shoulder, Aeroflex code# "P7"
- Sector Architecture (Each Die)
  - 8 Equal size sectors of 64K bytes each
  - Any Combination of Sectors can be erased with one command sequence
  - Supports Full Chip Erase
- DESC SMD# 5962–94716 Released (P3,P7,F5)

Block Diagram – PGA Type Package(P3,P7) & CQFP(F5)



Pin Description

I/O_{0-31}	Data I/O
A_{0-16}	Address Inputs
$\overline{\text{WE}}_{1-4}$	Write Enables
$\overline{\text{CE}}_{1-4}$	Chip Enables
$\overline{\text{OE}}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

General Description

The ACT–F128K32 is a high speed, 4 megabit CMOS flash multichip module (MCM) designed for full temperature range military, space, or high reliability applications.

The MCM can be organized as a 128K x 32 bits, 256K x 16 bits or 512K x 8 bits device and is input TTL and output CMOS compatible. The command register is written by bringing $\overline{\text{WE}}$ to a logic low level (V_{IL}), while $\overline{\text{CE}}$ is low and $\overline{\text{OE}}$ is at logic high level (V_{IH}). Reading is accomplished by chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) being logically active, see Figure 9. Access time grades of 60ns, 70ns, 90ns, 120ns and 150ns maximum are standard.

The ACT–F128K32 is packaged in a hermetically

General Description, Cont'd,

sealed co-fired ceramic 66 pin, 1.08" sq PGA or a 68 lead, .88" sq Ceramic Gull Wing CQFP package for operation over the temperature range of -55°C to +125°C and military environment.

Each flash memory die is organized as 128KX8 bits and is designed to be programmed in-system with the standard system 5.0V Vcc supply. A 12.0V VPP is not required for write or erase operations. The MCM can also be reprogrammed with standard EPROM programmers (with the proper socket).

The standard ACT-F128K32 offers access times between 60ns and 150ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$). The ACT-F128K32 is command set compatible with JEDEC standard 1 Mbit EEPROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations.

Reading data out of the device is similar to reading from 12.0V Flash or EPROM devices. The ACT-F128K32 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array, (if it is not already programmed before) executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

Each die in the module or any individual sector of the die is typically erased and verified in 1.3 seconds (if already completely preprogrammed).

Each die also features a sector erase architecture. The sector mode allows for 16K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The ACT-F128K32 is erased when shipped from the factory.

The device features single 5.0V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low VCC detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of D7 or by the Toggle Bit feature on D6. Once the end of a program or erase cycle has been completed,-+ the device internally resets to the read mode.

All bits of each die, or all bits within a sector of a die, are erased via Fowler-Nordhiem tunneling. Bytes are programmed one byte at a time by hot electron injection.

DESC Standard Military Drawing (SMD) numbers are released.

Absolute Maximum Ratings

Parameter	Symbol	Range	Units
Case Operating Temperature	T_C	-55 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Supply Voltage Range	V_{CC}	-2.0 to +7.0	V
Signal Voltage Range (Any Pin Except A9) Note 1	V_G	-2.0 to +7.0	V
Maximum Lead Temperature (10 seconds)		300	°C
Data Retention		10	Years
Endurance (Write/Erase cycles)		100,000 Minimum	
A9 Voltage for sector protect, Note 2	V_{ID}	-2.0 to +14.0	V

Note 1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot V_{SS} to -2.0v for periods of up to 20ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5V. During voltage transitions, inputs and I/O pins may overshoot to V_{CC} + 2.0V for periods up to 20 ns.
Note 2. Minimum DC input voltage on A9 is -0.5V. During voltage transitions, A9 may undershoot V_{SS} to -2.0V for periods of up to 20ns. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14.0V for periods up to 20ns.

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V
T_C	Operating Temperature (Military)	-55	+125	°C
V_{ID}	A9 Voltage for sector protect	11.5	12.5	V

Capacitance

(V_{IN}= 0V, f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{16} Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	Write Enable Capacitance		
	CQFP(F5) Package	20	pF
	PGA(P3,P7) Package	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O0 – I/O31 Capacitance	20	pF

Parameters Guaranteed but not tested

DC Characteristics – CMOS Compatible

(Vcc = 5.0V, Vss = 0V, T_C = -55°C to +125°C, unless otherwise indicated)

Parameter	Sym	Conditions	Speeds 60, 70, 90, 120 & 150ns		
			Minimum	Maximum	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOX32}	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}		10	µA
Active Operating Supply Current for Read (1)	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		140	mA
Active Operating Supply Current for Program or Erase(2)	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		200	mA
Standby Supply Current	I_{CC3}	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH}, f = 5MHz		6.5	mA
Static Supply Current (4)	I_{CC4}	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH}		0.6	mA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA, V_{CC} = 4.5V		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = –2.5 mA, V_{CC} = 4.5V	0.85 x V_{CC}		V
Output High Voltage (4)	V_{OH2}	I_{OH} = –100 µA, V_{CC} = 4.5V	V_{CC} – 0.4		V
Low Power Supply Lock-Out Voltage (4)	V_{LKO}		3.2		V

Note 1. The Icc current listed includes both the DC operating current and the frequency dependent component (At 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IN}.
Note 2. Icc active while Embedded Algorithm (Program or Erase) is in progress.
Note 3. DC Test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V, unless otherwise indicated
Note 4. Parameter Guaranteed but not tested.

Characteristics – Read Only Operations

(Vcc = 5.0V, Vss = 0V, Tc = -55°C to +125°C)

Parameter	Symbol		–60		–70		–90		–120		–150		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	60		70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		60		70		90		120		150	ns
Chip Enable Access Time	t_{ELQV}	t_{CE}		60		70		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		30		35		40		50		55	ns
Chip Enable to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		25		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		25		30		35	ns
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		0		0		0		0		ns

Note 1. Guaranteed by design, but not tested

AC Characteristics – Write/Erase/Program Operations, $\overline{WE}$ Controlled

(Vcc = 5.0V, Vss = 0V, Tc = -55°C to +125°C)

Parameter	Symbol		–60		–70		–90		–120		–150		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAC}	t_{WC}	60		70		90		120		150		ns
Chip Enable Setup Time	t_{ELWL}	t_{CE}	0		0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	30		35		45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	30		30		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		45		50		50		ns
Chip Enable Hold Time (1)	t_{WHEH}	t_{CH}	0		0		0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation	t_{WHWH1}		14	TYP	14	TYP	14	TYP	14	TYP	14	TYP	µs
Sector Erase Time	t_{WHWH2}			60		60		60		60		60	Sec
Chip Erase Time	t_{WHWH3}			120		120		120		120		120	Sec
Read Recovery Time before Write (1)	t_{GHWL}		0		0		0		0		0		µs
Vcc Setup Time (1)		t_{VCE}	50		50		50		50		50		µs
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	Sec
Output Enable Setup Time (1)		t_{OES}	0		0		0		0		0		ns
Output Enable Hold Time (1)		t_{OEH}	10		10		10		10		10		ns

Note 1. Guaranteed by design, but not tested

AC Characteristics – Write/Erase/Program Operations, $\overline{CE}$ Controlled

(Vcc = 5.0V, Vss = 0V, Tc = -55°C to +125°C)

Parameter	Symbol		–60		–70		–90		–120		–150		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAC}	t_{WC}	60		70		90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		ns
Chip Enable Pulse Width	t_{ELEH}	t_{CP}	35		35		45		50		55		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	30		30		45		50		55		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		45		50		55		ns
Write Enable Hold Time (1)	t_{EHWH}	t_{WH}	0		0		0		0		0		ns
Write Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		ns
Duration of Byte Programming	t_{WHWH1}		14	TYP	14	TYP	14	TYP	14	TYP	14	TYP	µs
Sector Erase Time	t_{WHWH2}			60		60		60		60		60	Sec
Chip Erase Time	t_{WHWH3}			120		120		120		120		120	Sec
Read Recovery Time (1)	t_{GHEL}		0		0		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	Sec

Note 1. Guaranteed by design, but not tested

Device Operation

The ACT-F128K32 MCM is composed of four, one megabit flash EEPROMs. The following description is for the individual flash EEPROM device, is applicable to each of the four memory chips inside the MCM. Chip 1 is distinguished by $\overline{CE}_1$ and I/O$_{1-7}$, Chip 2 by $\overline{CE}_2$ and I/0$_{8-15}$, Chip 3 by $\overline{CE}_3$ and I/0$_{16-23}$, and Chip 4 by $\overline{CE}_4$ and I/0$_{24-31}$.

Programming of the ACT-F128K32 is accomplished by executing the program command sequence. The program algorithm, which is an internal algorithm, automatically times the program pulse widths and verifies proper cell status. Sectors can be programed and verified in less than 0.3 second. Erase is accomplished by executing the erase command sequence. The erase algorithm, which is internal, automatically preprograms the array if it is not already programed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell status. The entire memory is typically erased and verified in 3 seconds (if pre-programmed). The sector mode allows for 16K byte blocks of memory to be erased and reprogrammed without affecting other blocks.

Bus Operation

READ

The ACT-F128K32 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins of the chip selected. Figure 7 illustrates AC read timing waveforms.

OUTPUT DISABLE

With Output-Enable at a logic high level (V_{IH}), output from the device is disabled. Output pins are placed in a high impedance state.

STANDBY MODE

The ACT-F128K32 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc + 0.5V), where the current consumed is typically less than 400 µA; and a TTL standby mode ($\overline{CE}$ is held V_{IH}) is approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

WRITE

Device erasure and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to a logic low level (V_{IL}), while $\overline{CE}$ is low and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. Data is latched on the rising edge of the $\overline{WE}$ or $\overline{CE}$ whichever occurs first. Standard microprocessor write timings are used. Refer to AC Program Characteristics and Waveforms, Figures 3, 8 and 13.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Table 3 defines these register command sequences.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard Microprocessor read cycles will retrieve array data. This

Table 1 – Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	I/O
READ	L	L	H	A_0	A_1	A_9	DOUT
STANDBY	H	X	X	X	X	X	HIGH Z
OUTPUT DISABLE	L	H	H	X	X	X	HIGH Z
WRITE	L	H	L	A_0	A_1	A_9	D_{IN}
ENABLE SECTOR PROTECT	L	V_{ID}	L	X	X	V_{ID}	X
VERIFY SECTOR PROTECT	L	L	H	L	H	V_{ID}	Code

Table 2 – Sector Addresses Table

	A16	A15	A14	Address Range
SA0	0	0	0	00000h – 03FFFh
SA1	0	0	1	04000h – 07FFFh
SA2	0	1	0	08000h – 0BFFFh
SA3	0	1	1	0C000h – 0FFFFh
SA4	1	0	0	10000h – 13FFFh
SA5	1	0	1	14000h – 17FFFh
SA6	1	1	0	18000h – 1BFFFh
SA7	1	1	1	1C000h – 1FFFFh

Table 3 — Commands Definitions

Command Sequence	Bus Write Cycle Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Byte Program	6	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

NOTES:
1. Address bit A15 = X = Don't Care. Write Sequences may be initiated with A15 in either state.
2. Address bit A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).
3. RA = Address of the memory location to be read
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{\text{WE}}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14 will uniquely select any sector.
4. RD = Data read from location RA during read Operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{\text{WE}}$.

default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Figure 7 for the specific timing parameters.

BYTE PROGRAMING

The device is programmed on a byte-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs later, while the data is latched on the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever occurs first. The rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the program algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell.

The automatic programming operation is completed when the data on D7 (also used as $\overline{\text{Data}}$ Polling) is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address be supplied by the system at this particular instance of time for $\overline{\text{Data}}$ Polling operations. $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a “1". Attempting to do so may cause the device to exceed programming time limits (D5 = 1) or result in an apparent success, according to the data polling algorithm, but a read from reset/read mode will show that the data is still “0". Only erase operations can convert “0"s to “1"s.

Figure 3 illustrates the programming algorithm using typical command strings and bus operations.

CHIP ERASE

Chip erase is a six bus cycle operation. There are two 'unlock' write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence (Figure 4) the device will automatically program and verify the entire memory for an all zero data pattem prior to electrical erase. The erase is performed concurrently on all sectors at the same time . The system is not required to provide any controls or timings during these operations. *Note: Post Erase data state is all "1"s.*

The automatic erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse in the command sequence and terminates when the data on D7 is "1" (see Write Operation Status section - Table 3) at which time the device retums to read mode. See Figures 4 and 9.

SECTOR ERASE

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "setup" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{WE}}$, while the command (30H) is latched on the rising edge of $\overline{\text{WE}}$. After a time-out of 80µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the sector erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80µs from the rising edge of the last $\overline{\text{WE}}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{\text{WE}}$ occurs within the 80µs time-out window the timer is reset. (Monitor D3 to determine if the sector erase timer window is still open, see section D3, Sector Erase Timer.) Any command other than Sector Erase during this period will reset the device to read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete.

Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations. Post Erase data state is all "1"s.

The automatic sector erase begins after the 80µs time out from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command pulse and terminates when the data on D7, $\overline{\text{Data}}$ Polling, is “1" (see Write Operation Status secton) at which time the device returns to read mode. $\overline{\text{Data}}$ Polling must be performed at an address within any of the sectors being erased.

Figure 4 illustrates the Embedded Erase Algorithm.

Data Protection

The ACT-F128K32 is designed to offer protection against accidental erasure or programming caused by spurious system level singles that may exist during power transitions. During power up the device automatically resets the internal state machine in the read mode. Also, with its control register architecture, alteration of the memory content only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise.

LOW V_{CC} WRITE INHIBIT

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2V (typically 3.7V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2V.

WRITE PULSE GLITCH PROTECTION

Noise pulses of less than 5ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding anyone of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be logical zero while $\overline{\text{OE}}$ is a logical one.

POWER-UP WRITE INHIBIT

Power-up of the device with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

Write Operation Status

D7

$\overline{\text{DATA}}$ POLLING

The ACT-F128K32 features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the internal algorithms are in progress or completed.

During the program algorithm, an attempt to read the device will produce compliment data of the data last written to D7. Upon completion of the programming algorithm an attempt to read the device will produce the true data last written to D7. $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence.

During the erase algorithm, D7 will be "0" until the erase operation is completed. Upon completion data at D7 is "1". For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is Valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse.

The $\overline{\text{Data}}$ Polling feature is only active during the programming algorithm, erase algorithm, or sector erase time-out.

See Figures 6 and 10 for the Data Polling specifications.

D6

TOGGLE BIT

The ACT-F128K32 also features the "Toggle Bit" as a method to indicate to the host system that algorithms are in progress or completed.

During a program or erase algorithm cycle, successive attempts to read data from the device will result in D6 toggling between one and zero. Once the program or erase algorithm cycle is completed, D6 Will stop toggling and valid data will be read on successive attempts. During programming the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

See Figure 1 and 5.

Table 4 — Hardware Sequence Flags

	Status	D7	D6	D5	D4	D3	D2 – D0
In Progress	Auto-Programming	$\overline{D7}$	Toggle	0	0	0	Reserved for future use
	Programming in Auto Erase	0	Toggle	0	0	1	
	Erase in Auto Erase	0	Toggle	0	1	1	
Exceeding Time Limits	Auto-Programming	$\overline{D7}$	Toggle	1	0	0	Reserved for future use
	Programming in Auto Erase	T0	Toggle	1	0	1	
	Erase in Auto Erase	0	Toggle	1	1	1	

D5

EXCEEDED TIMING LIMITS

D5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions D5 will produce a "1". The Program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operation function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions by approximately 8 mA per chip. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as shown in Table 1. To reset the device, write the reset command sequence to the device. This allows the system to continue to use the other active sectors in the device.

D4 - HARDWARE SEQUENCE FLAG

If the device has exceeded the specified erase or program time and D5 is "1", then D4 Will indicate which step in the algorithm the device exceeded the limits. A "0" in D4 indicates in programming, a "1" indicates an erase. (See Table 4)

D3

SECTOR ERASE TIMER

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D3 may be used to determine if the sector erase timer window is still open. If D3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If D3 is low ("0"), the device will accept additional sector erase commands. To ensure the command has been accepted, the software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted.

Sector Protection Algorithims

SECTOR PROTECTION

The ACT-F128K32 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A16, A15, and A14. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A16, A15 and A14) define a particular sector, will produce 01H at data outputs D0 - D7, for a protected sector.

SECTOR UNPROTECT

The ACT-F128K32 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A7, and A12 should be set to V_{IH}, and A6 = V_{IL}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command. Performing a read operation at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector address, will produce 00H at data outputs (D0-D7) for an unprotected sector.

Figure 1
AC Waveforms for Toggle Bit During Embedded Algorithm Operations

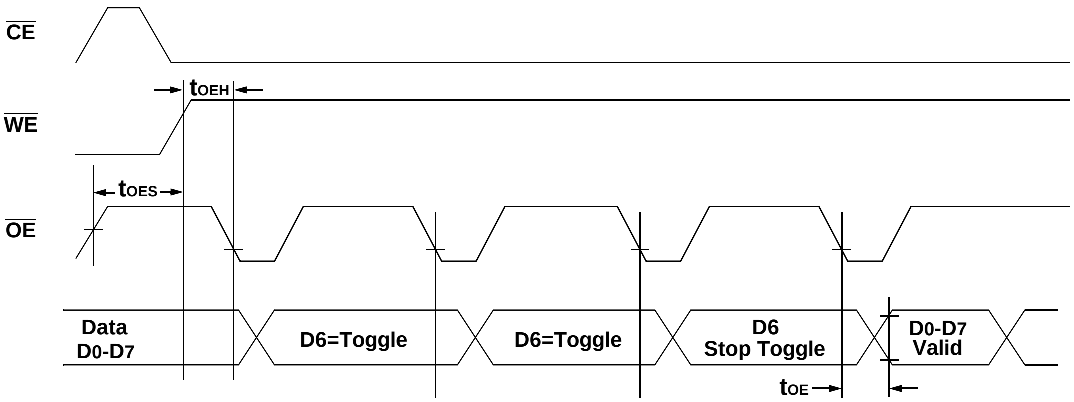
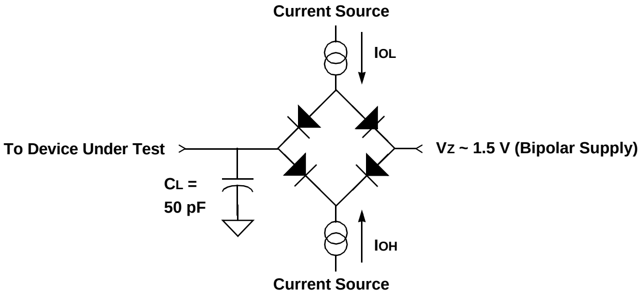


Figure 2
AC Test Circuit

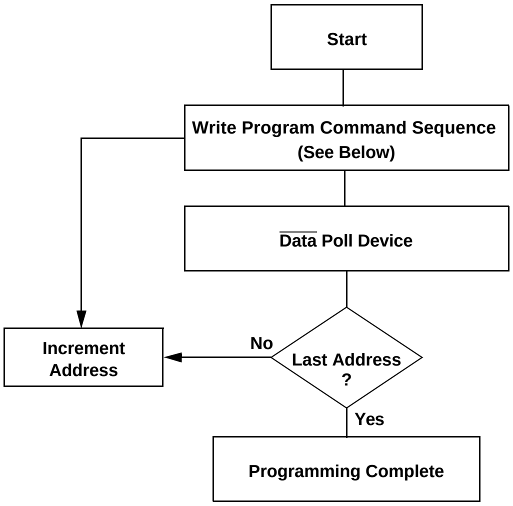


Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference	1.5	V
Output Lead Capacitance	50	pF

Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance $Z_O = 75\Omega$. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Figure 3
Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming
Standby		Compare Data Output to Data Expected



Program Command Sequence (Address/Command):

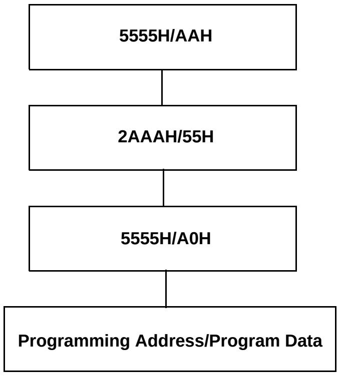
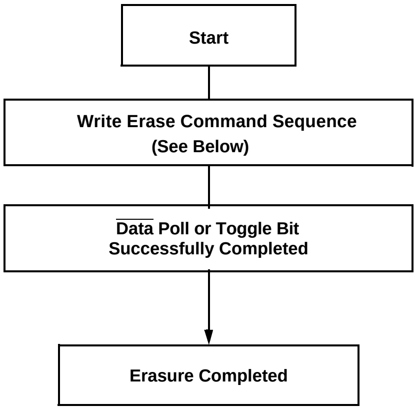
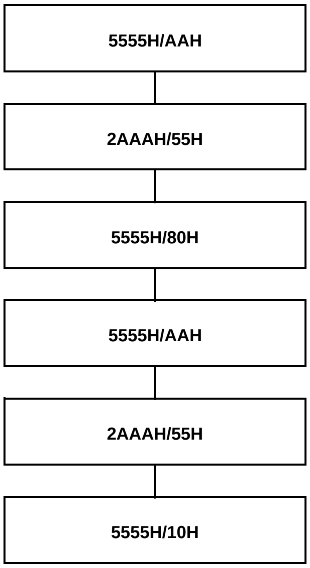


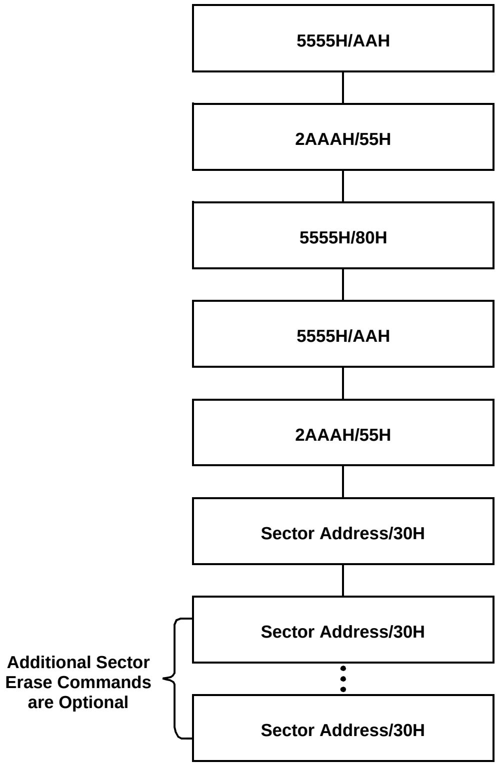
Figure 4
Erase Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby		Compare Output to FFH





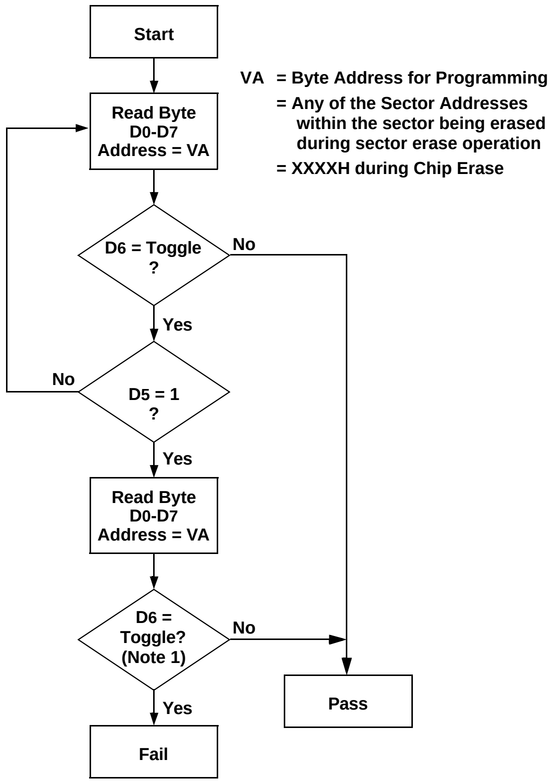
Chip Erase Command Sequence (Address/Command)



Individual Sector/Multiple Sector Erase Command Sequence (Address/Command)

Note 1. To Ensure the command has been accepted, the system software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted.

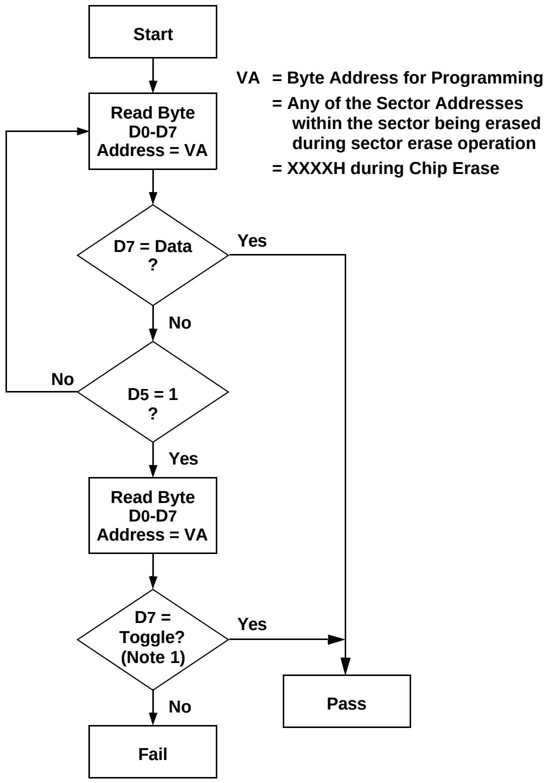
Figure 5
Toggle Bit Algorithm



VA = Byte Address for Programming
= Any of the Sector Addresses within the sector being erased during sector erase operation
= XXXXH during Chip Erase

Note 1. D6 is rechecked even if D5 = "1" because D6 may stop toggling at the same time as D5 changes to "1".

Figure 6
Data Polling Algorithm



VA = Byte Address for Programming
= Any of the Sector Addresses within the sector being erased during sector erase operation
= XXXXH during Chip Erase

Note 1. D7 is rechecked even if D5 = "1" because D7 may change simultaneously with D5.

Figure 7
AC Waveforms for Read Operations

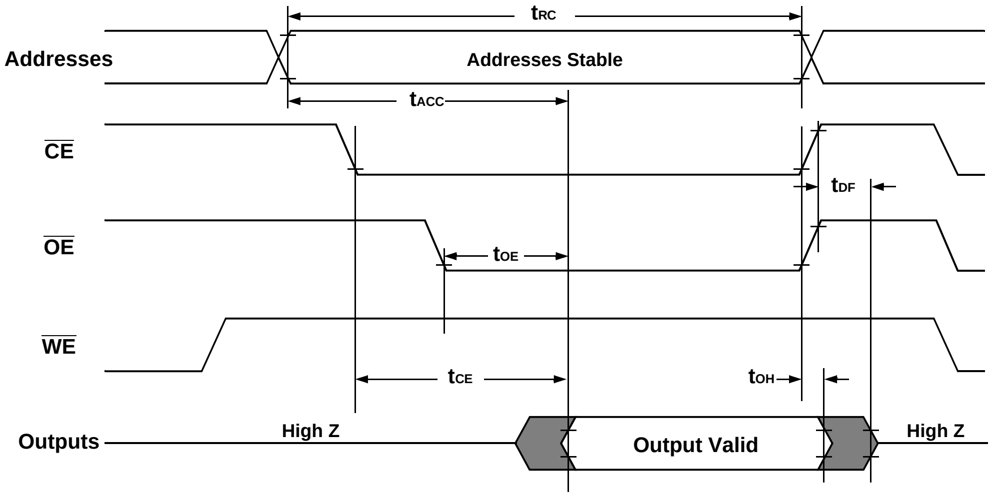
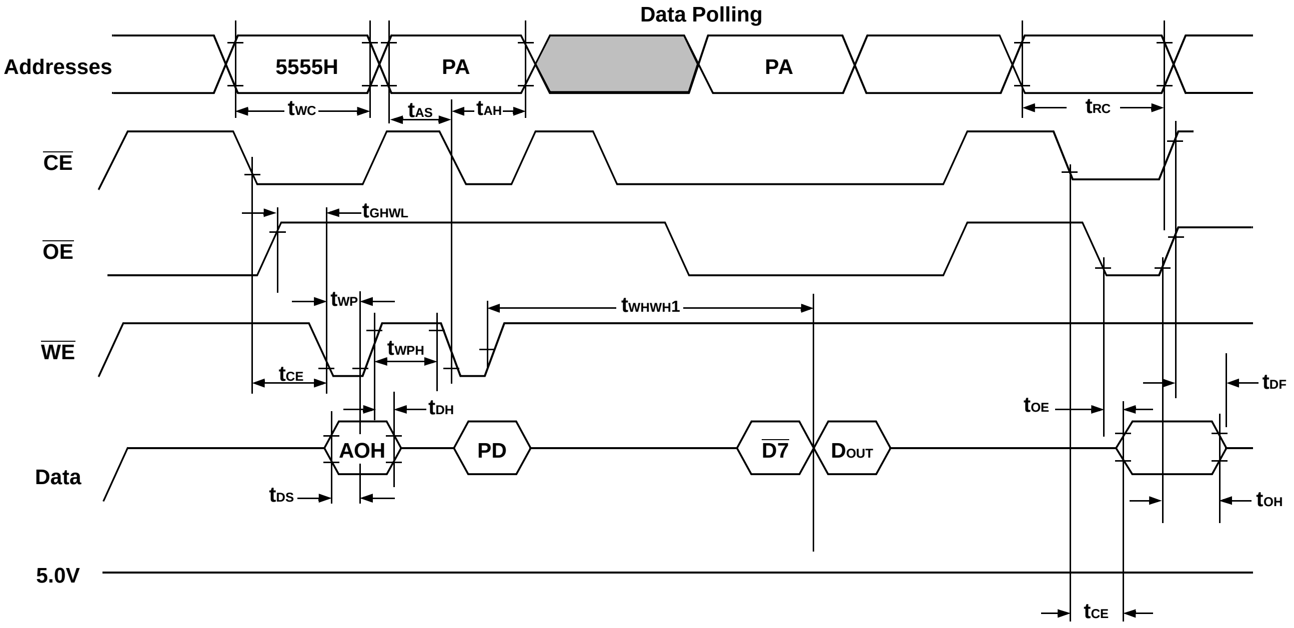
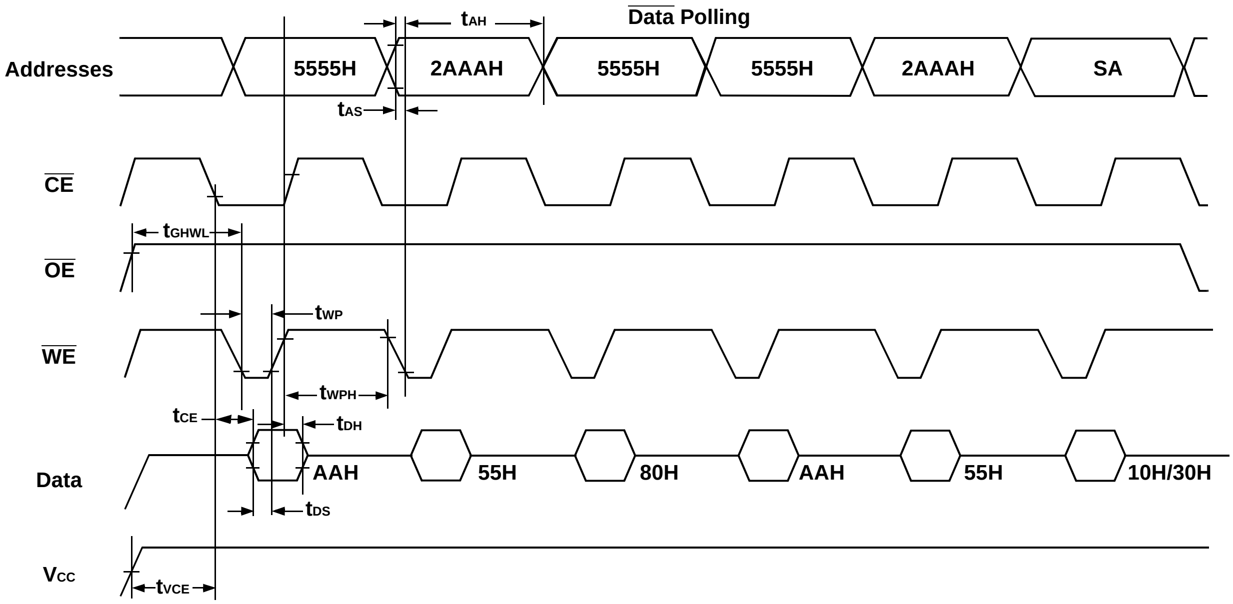


Figure 8
Write/Erase/Program Operation, $\overline{\text{WE}}$ Controlled



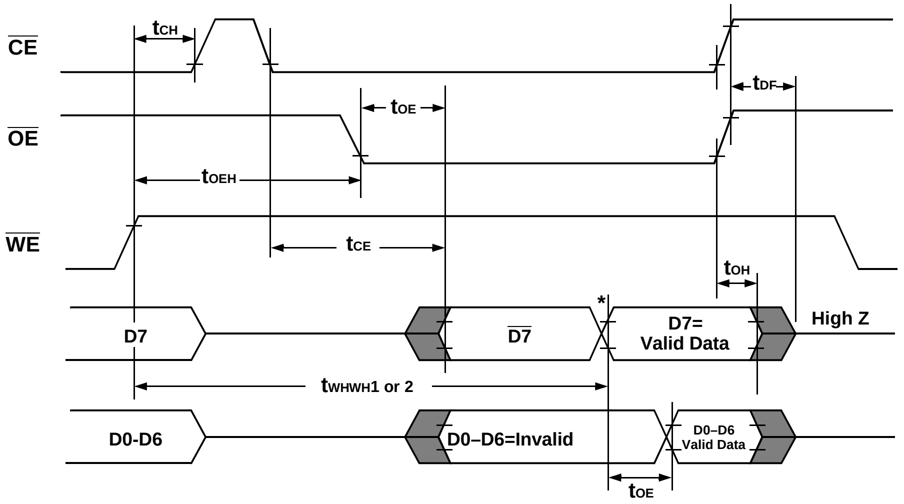
Notes:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the 0utput of the complement of the data written to the deviced.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 9
AC Waveforms Chip/Sector Erase Operations



Notes:
1. SA is the sector address for sector erase.

Figure 10
AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations



*** D7=Valid Data (The device has completed the Embedded operation).**

Figure 11
Sector Protection Algorithm

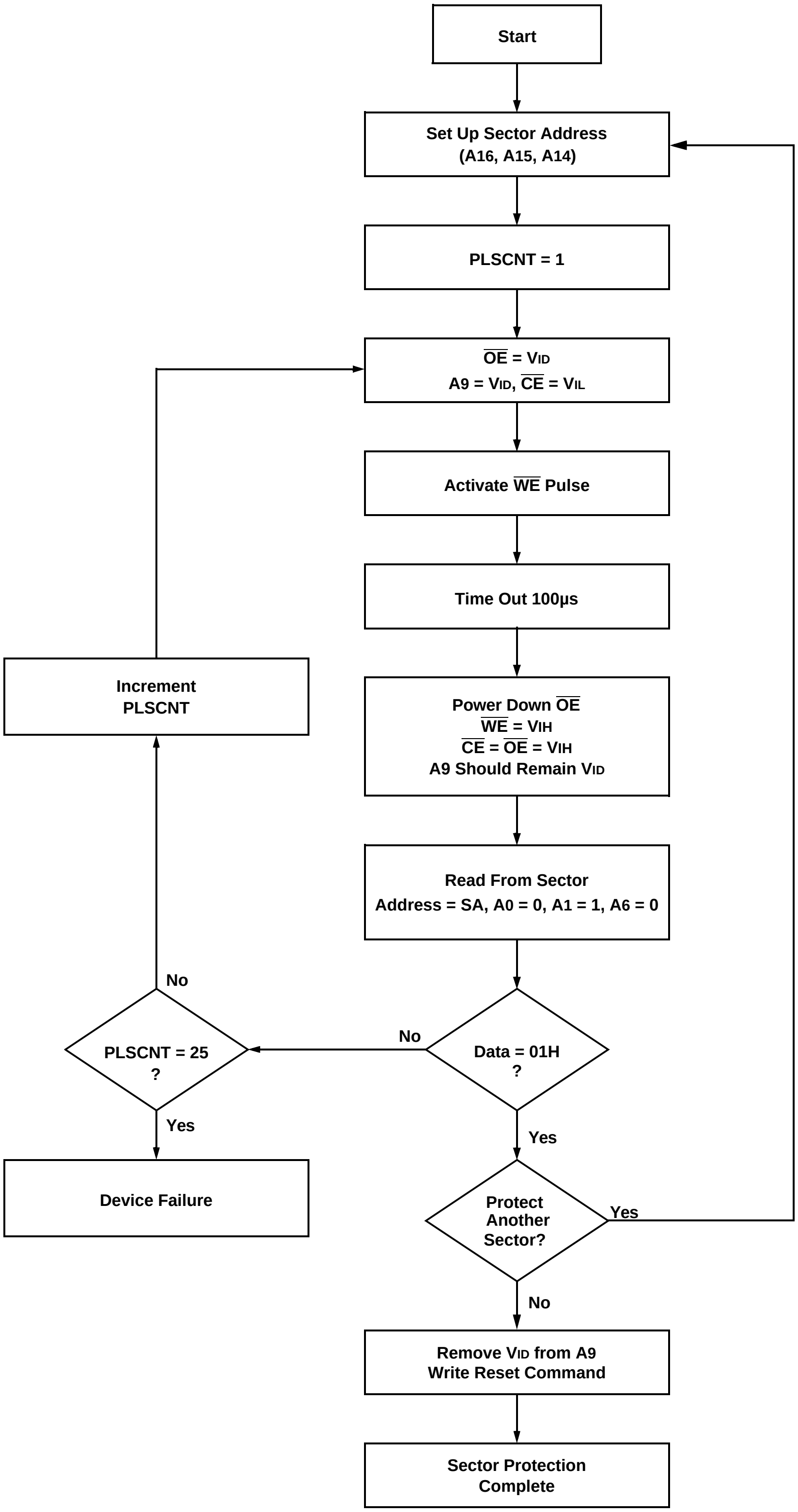
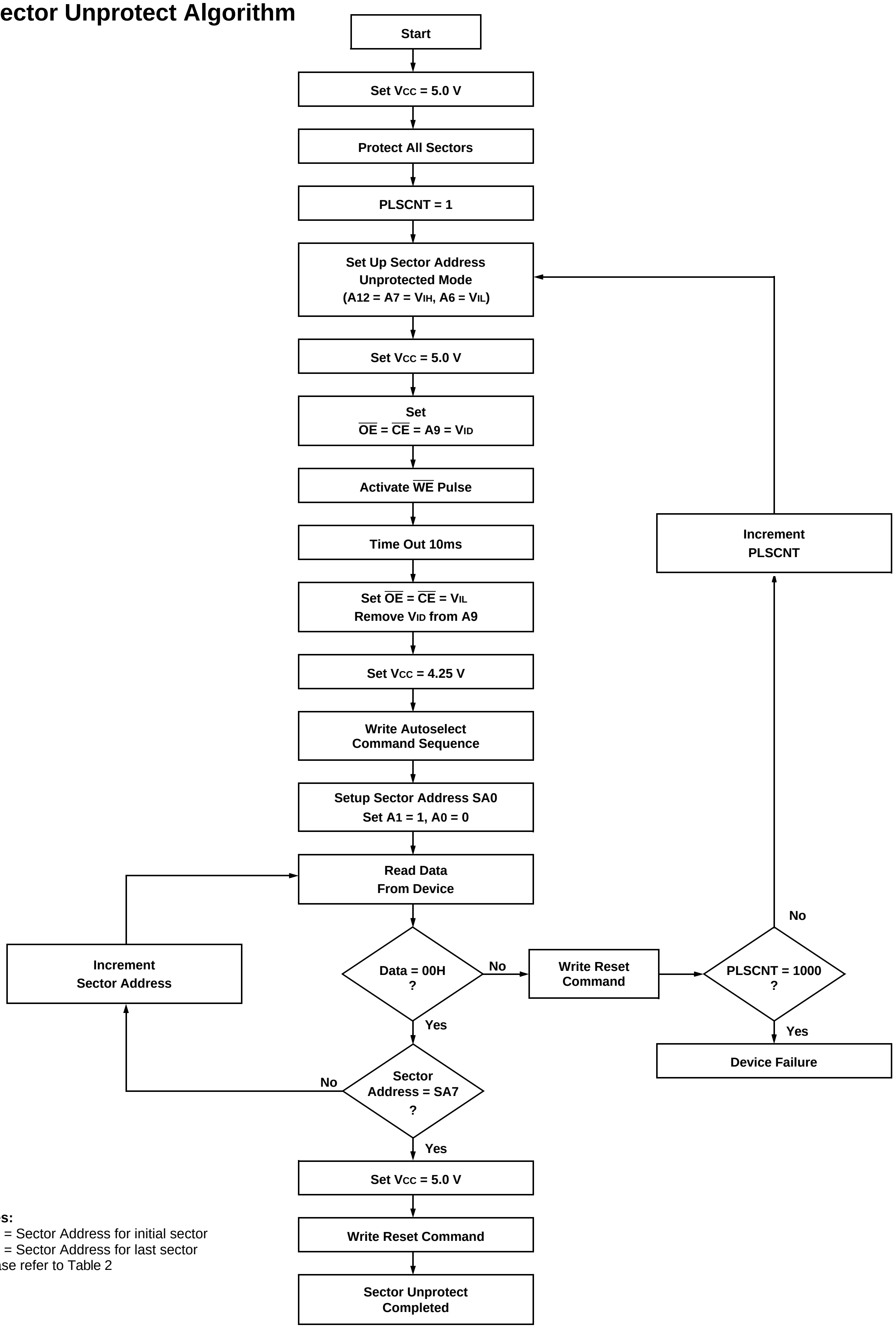
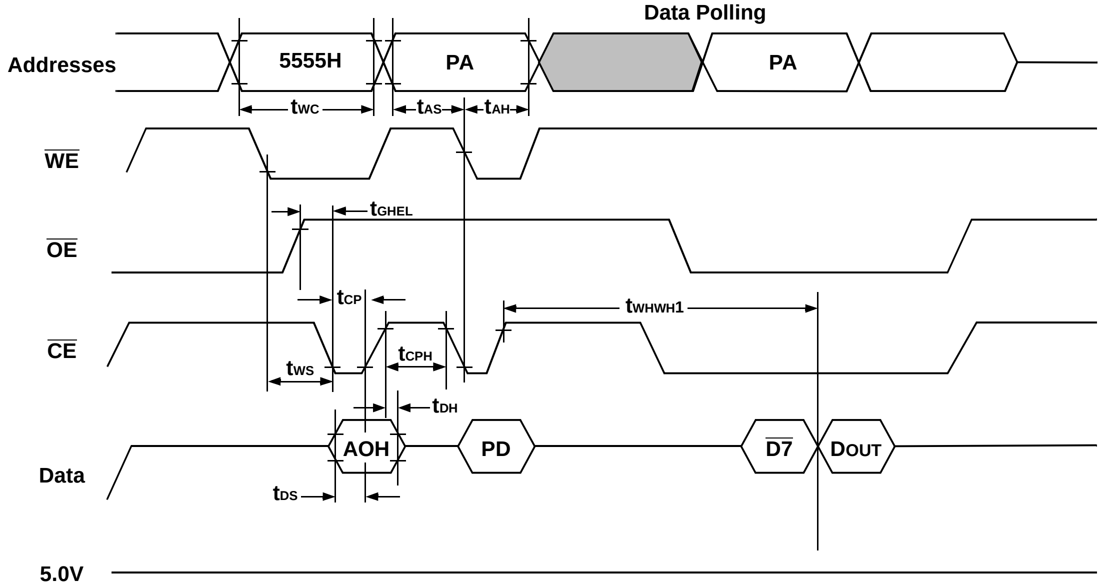


Figure 12
Sector Unprotect Algorithm



Notes:
SA0 = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 2

Figure 13
Write/Erase/Program Operation, $\overline{\text{CE}}$ Controlled



Notes:

1. PA is the address of the memory location to be programmed.
2. $\overline{\text{PD}}$ is the data to be programmed at byte address.
3. $\overline{\text{D7}}$ is the 0utput of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

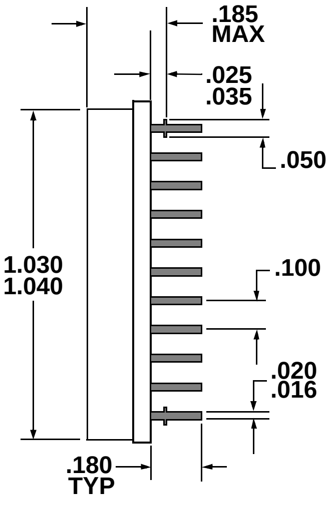
Pin Numbers & Functions

66 Pins — PGA

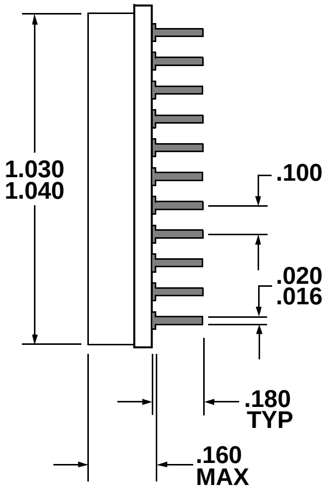
Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	I/O$_8$	18	A$_{15}$	35	I/O$_{25}$	52	$\overline{\text{WE}}_3$
2	I/O$_9$	19	Vcc	36	I/O$_{26}$	53	$\overline{\text{CE}}_3$
3	I/O$_{10}$	20	$\overline{\text{CE}}_1$	37	A$_7$	54	GND
4	A$_{14}$	21	NC	38	A$_{12}$	55	I/O$_{19}$
5	A$_{16}$	22	I/O$_3$	39	NC	56	I/O$_{31}$
6	A$_{11}$	23	I/O$_{15}$	40	A$_{13}$	57	I/O$_{30}$
7	A$_0$	24	I/O$_{14}$	41	A$_8$	58	I/O$_{29}$
8	NC	25	I/O$_{13}$	42	I/O$_{16}$	59	I/O$_{28}$
9	I/O$_0$	26	I/O$_{12}$	43	I/O$_{17}$	60	A$_1$
10	I/O$_1$	27	$\overline{\text{OE}}$	44	I/O$_{18}$	61	A$_2$
11	I/O$_2$	28	NC	45	V$_{CC}$	62	A$_3$
12	$\overline{\text{WE}}_2$	29	$\overline{\text{WE}}_1$	46	$\overline{\text{CE}}_4$	63	I/O$_{23}$
13	$\overline{\text{CE}}_2$	30	I/O$_7$	47	$\overline{\text{WE}}_4$	64	I/O$_{22}$
14	GND	31	I/O$_6$	48	I/O$_{27}$	65	I/O$_{21}$
15	I/O$_{11}$	32	I/O$_5$	49	A$_4$	66	I/O$_{20}$
16	A$_{10}$	33	I/O$_4$	50	A$_5$		
17	A$_9$	34	I/O$_{24}$	51	A$_6$		

"P3" — 1.08" SQ PGA Type (without shoulder) Package
"P7" — 1.08" SQ PGA Type (with shoulder) Package

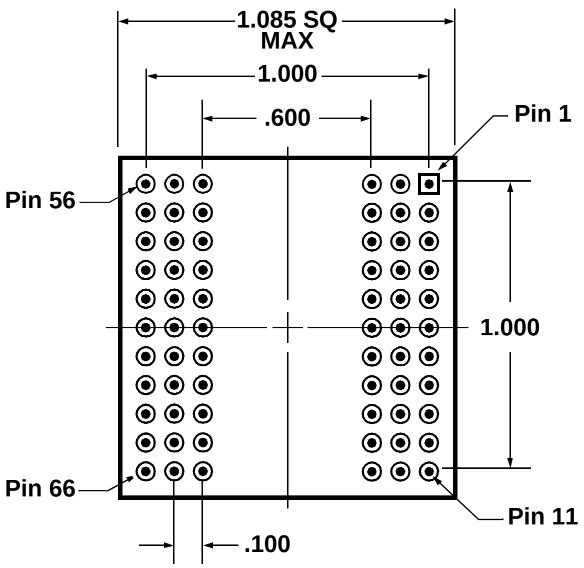
Side View (P7)



Side View (P3)



Bottom View (P7 & P3)



All dimensions in inches

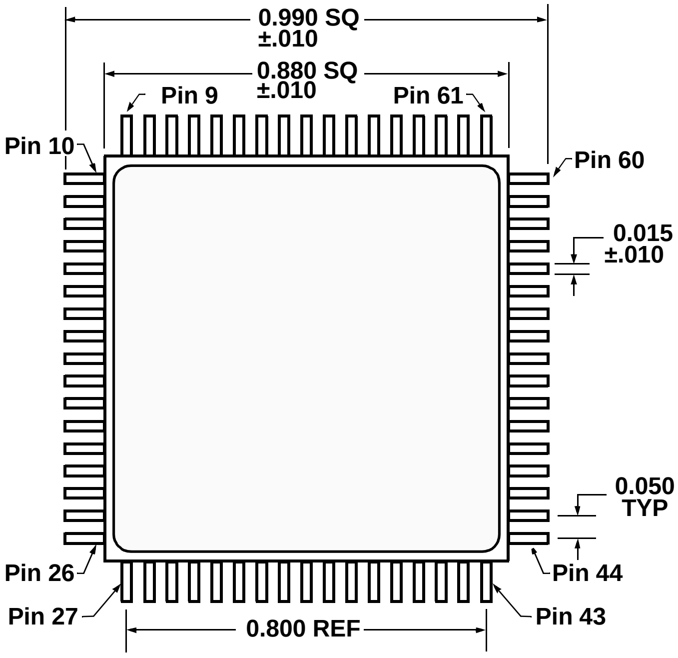
Pin Numbers & Functions

68 Pins — CQFP Package

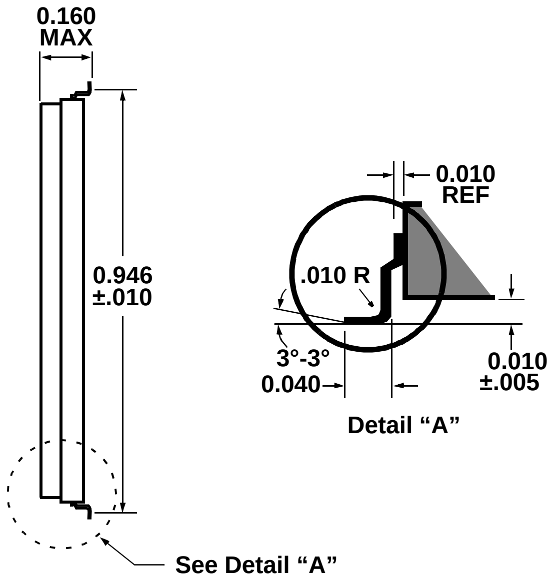
Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}_1$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

"F5" — Single-Cavity CQFP

Top View



Side View



All dimensions in inches

AEROFLEX
CIRCUIT TECHNOLOGY

Ordering Information

Model Number	DESC Drawing Number	Speed	Package
ACT–F128K32N–060P3Q	5962-9471605HZX*	60 ns	PGA
ACT–F128K32N–070P3Q	5962-9471604HZC	70 ns	PGA
ACT–F128K32N–090P3Q	5962-9471603HZC	90 ns	PGA
ACT–F128K32N–120P3Q	5962–9471602HZC	120 ns	PGA
ACT–F128K32N–150P3Q	5962–9471601HZC	150 ns	PGA
ACT–F128K32N–060P7Q	5962-9471605H8X*	60 ns	PGA
ACT–F128K32N–070P7Q	5962-9471604H8C	70 ns	PGA
ACT–F128K32N–090P7Q	5962-9471603H8C	90 ns	PGA
ACT–F128K32N–120P7Q	5962–9471602H8C	120 ns	PGA
ACT–F128K32N–150P7Q	5962–9471601H8C	150 ns	PGA
ACT–F128K32N–060F5Q	5962-9471605HNX*	60 ns	CQFP
ACT–F128K32N–070F5Q	5962-9471604HNC	70 ns	CQFP
ACT–F128K32N–090F5Q	5962-9471603HNC	90 ns	CQFP
ACT–F128K32N–120F5Q	5962–9471602HNC	120 ns	CQFP
ACT–F128K32N–150F5Q	5962–9471601HNC	150 ns	CQFP

* Pending

Part Number Breakdown

ACT– F 128K 32 N– 060 F5 Q

Aeroflex Circuit Technology

Memory Type
F = FLASH EEPROM

Memory Depth

Memory Width, Bits

Options
N = None

Memory Speed, ns

Screening
C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-STD-883 Compliant/SMD if applicable

Package Type & Size

Surface Mount Packages	*Thru-Hole Packages*
F5 = .88"SQ 68 Lead Single-Cavity CQFP	P3 = 1.075"SQ PGA 66 Pins W/O Shoulder
	P7 = 1.075"SQ PGA 66 Pins With Shoulder

*** Screened to the individual test methods of MIL-STD-883**

Specification subject to change without notice

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Plainview New York 11830

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