a6850

Asynchronous Communications Interface Adapter

September 1996, ver. 1 Data Sheet

Features

- a6850 MegaCore function implementing an asychronous communications interface adapter (ACIA)
- Optimized for FLEX® and MAX® architectures
- Programmable word lengths, stop bits, and parity
- Offers divide-by-1, -16, or -64 mode
- Includes error detection
- Uses approximately 237 FLEX logic elements (LEs)
- Functionally based on the Motorola MC6850 device, except as noted in the "Variations & Clarifications" section on page 94

General Description

The a6850 MegaCore function implements an ACIA, which is a universal asynchronous receiver/transmitter (UART). The a6850 provides an interface between a microprocessor and a serial communications channel. The a6850 receives and transmits data in a variety of configurations, including 7- or 8-bit data words, with odd, even, or no parity, and 1 or 2 stop bits. See Figure 1.

Figure 1. a6850 Symbol

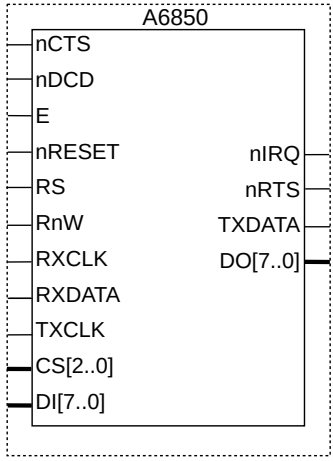


Table 1 describes the input and output ports of the a6850.

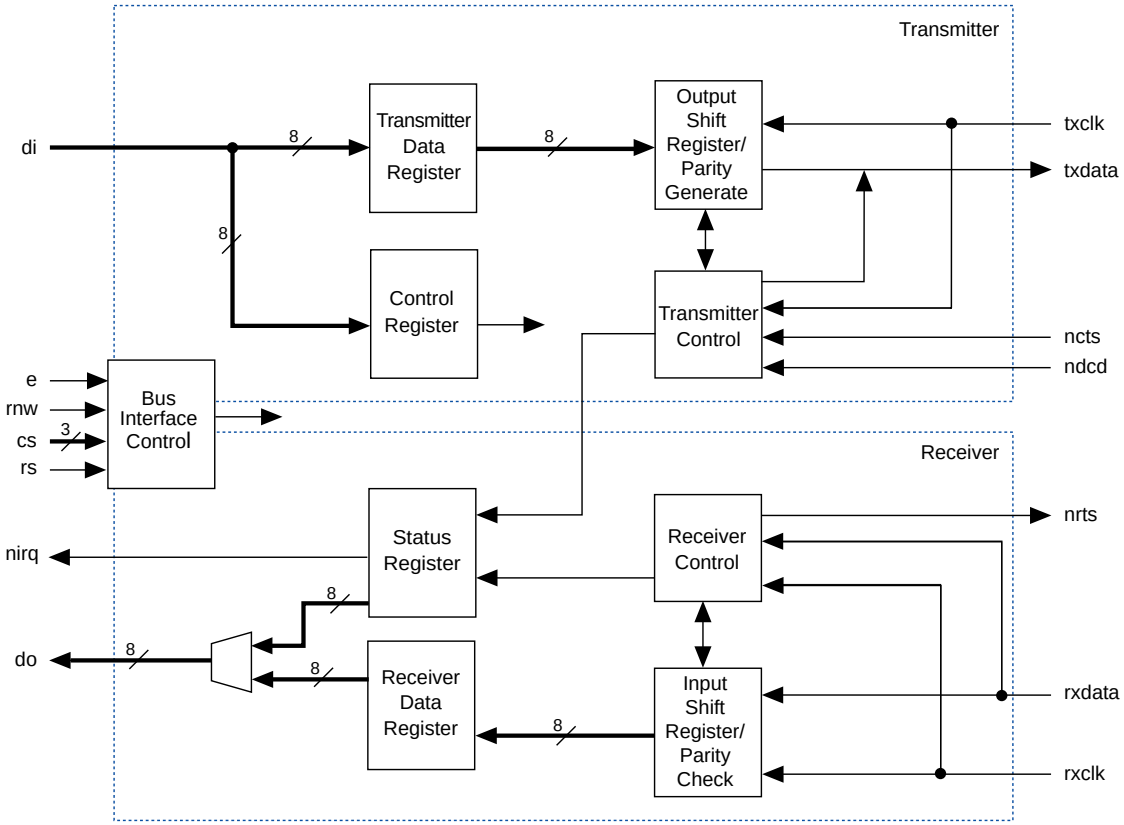
Table 1. a6850 Ports

Name	Type	Polarity	Description
ncts	Input	Low	Clear to send, a modem signal name. The ncts input inhibits the assertion of the transmit data register empty (tdre) status bit.
ndcd	Input	Low	Data carrier detect, a modem signal name. When the ndcd signal transitions from low to high, an interrupt to the microprocessor is generated.
e	Input	High	Enable for the microprocessor interface. When e is high, the microprocessor can access the registers.
nreset	Input	Low	Asynchronous reset for the registers and control logic. The nreset pin was not included in the original MC6850 device.
rs	Input	–	Register select. This input selects the register based on rnw. If rnw is high (signaling a read operation), then rs = 1 selects the receiver data register and rs = 0 selects the status register. However, if rnw is low (signaling a write operation), then rs = 1 selects the transmitter data register and rs = 0 selects the control register.
rnw	Input	Low	Read/write register controls. When rnw is high, the microprocessor reads the registers; when rnw is low, the microprocessor writes to the registers.
rxclk	Input	–	Receive clock. The receive control register samples rxdata based on rxclk and the state of the counter divide select (cds) bits in the control register.
rxdata	Input	–	Receive data. Serial data input from the modem or peripheral.
txclk	Input	–	Transmit clock. Data is asserted to txdata on the falling edge of txclk.
cs[2..0]	Input	–	Chip select from the microprocessor. Chip select must be in the 110 state for the a6850 to be selected.
di[7..0]	Input	–	Parallel data input from the microprocessor or other controlling device.
nirq	Output	Low	Interrupt request to microprocessor.
nrts	Output	Low	Request to send. Bits 5 and 6 (transmitter control bits) of the control register set the nrts bit. The nrts signal is asserted when bit 6 is low, or bits 5 and 6 are both high.
txdata	Output	–	Transmit data. Serial output to the modem or peripheral.
do[7..0]	Output	–	Parallel data output to the microprocessor or other controlling device.

Functional Description

Figure 2 shows the a6850 block diagram.

Figure 2. a6850 Block Diagram



Registers

The a6850 contains the following registers:

- Transmitter data register
- Receiver data register
- Control register
- Status register

Transmitter Data Register

The transmitter data register (TDR) is written to by the microprocessor or other controlling device. Once the existing data bits in the output shift register are completely transmitted out, the TDR transfers new data into the output shift register.

Receiver Data Register

The receiver data register (RDR) is written to by the input shift register. Once the existing data in the RDR is read, the input shift register transfers new data into the RDR. If 7-bit data is selected, bit 7 is set to a logic low.

Control Register

The control register contains the control bits shown in Table 2.

Table 2. Control Register Bits

Data Bit	Signal Name
0	Counter divide select 0 (`cds0`)
1	Counter divide select 1 (`cds1`)
2	Word select 0 (`ws0`)
3	Word select 1 (`ws1`)
4	Word select 2 (`ws2`)
5	Transmitter control 0 (`tc0`)
6	Transmitter control 1 (`tc1`)
7	Receive interrupt enable (`rie`)

Counter Divide Select

Bits 0 and 1 of the control register are the `cds` bits, which determine the ratio between the data rate and the clocks. The ratios when transmitting and receiving are identical. The `cds` bits can also be used to reset the `a6850` to a known state. See Table 3.

Table 3. Counter Divide Select Bits

cds1	cds0	Function
0	0	Divide-by-1 mode. Clock and data rate are identical. External logic is responsible for synchronizing rxdata to rxclk. The rxdata signal is sampled on the rising edge of rxclk, and the txdata signal is asserted on the falling edge of txclk.
0	1	Divide-by-16 mode. The clock rate is 16 times the data rate. After start bit detection (rxdata low), the rxdata signal is sampled on the 9th rising edge of rxclk. After writing to the transmitter data register, the txdata signal is asserted on the first falling edge of txclk and every 16 clocks thereafter.
1	0	Divide-by-64 mode. The clock rate is 64 times the data rate. After start bit detection (rxdata low), the rxdata signal is sampled on the 33rd rising edge of rxclk. After writing to the transmitter data register, the txdata signal is asserted on the first falling edge of txclk and every 64 clocks thereafter.
1	1	Master reset. When master reset is selected, the a6850 is reset to a known state; the status register is cleared, and the transmit and receive operations are halted and initialized.

Word Select

Bits 2, 3, and 4 of the control register are the ws bits, which determine the word length, parity, and number of stop bits. See Table 4.

Table 4. Word Select Bits

ws2	ws1	ws0	Word Length	Stop Bits	Parity
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	2	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

Transmitter Control

Bits 5 and 6 of the control register are the `tc` bits, (see Table 5). The `tc` bits are responsible for:

- Enabling or disabling the interrupt caused by a transmitter data register empty (`tdre`) condition.
- Controlling the request to send (`nrts`) signal.
- Transmitting a break character on the `txdata` output.

Table 5. Transmitter Control Bits

tc1	tc0	nrts	Transmit Interrupt	Break Character
0	0	Low	Disabled	No
0	1	Low	Enabled	No
1	0	High	Disabled	No
1	1	Low	Disabled	Yes

Receive Interrupt Enable

Bit 7 of the control register is the `rie` bit. When the `rie` bit is high, the `rdrf`, `ndcd`, and `ovr` bits will assert the `nirq` output. When the `rie` bit is low, `nirq` generation is disabled.

Status Register

The status register contains the status bits shown in Table 6.

Table 6. Status Register Bits

Data Bit	Bit Name
0	Receive data register full (`rdrf`)
1	Transmit data register empty (`tdre`)
2	Data carrier detect (`ndcd`)
3	Clear to send (`ncts`)
4	Framing error (`fe`)
5	Receiver overrun (`ovr`)
6	Parity error (`pe`)
7	Interrupt request (`irq`)

Receiver Data Register Full

Bit 0 of the status register is the rdrf bit. When high, the rdrf bit indicates that received data has been transferred into the receiver data register and is ready to be read by the microprocessor. If the receive interrupt is enabled, then the nirq signal is asserted.

The rdrf bit is cleared when either the nreset signal is asserted, the microprocessor reads the receiver data register, or the control register is set to master reset mode.

Transmitter Data Register Empty

Bit 1 of the status register is the tdre bit. When high, the tdre bit indicates that data has been transferred from the transmitter data register to the output shift register. At this point, the a6850 is ready to accept a new transmit data byte. However, if the ncts signal is high, the tdre bit remains low regardless of the status of the transmitter data register. Also, if transmit interrupt is enabled, the nirq output is asserted.

The tdre bit is cleared when the nreset signal is asserted, the microprocessor writes to the transmitter data register, or the control register is set to master reset mode.

Data Carrier Detect

Bit 2 of the status register is the ndcd bit, which reflects the status of the ndcd input. When the ndcd input transitions from low to high, the status bit is set to a logic high. If the receive interupts are enabled, a low on the nirq output is produced. Once the ndcd bit is set, it remains high regardless of the state of the ndcd input until one of the following conditions occurs:

- The status register is read after reading the receiver data register.
- The nreset signal is asserted.
- The control register is set to master reset mode.

Clear to Send

Bit 3 of the status register is the ncts bit, and reflects the status of the ncts input. The nreset input sets ncts bit to a logic high until the next rising edge of txclk.

Framing Error

Bit 4 of the status register is the fe bit. The fe bit is asserted when a received character does not end with the specified stop bit, which is usually caused by a transmission error. The fe bit is set when the received character is transferred to the receiver data register, and remains set until another character is written to the receiver data register.

The fe bit is cleared when either the nreset signal is asserted, a character is written to the receiver data register that does not have an fe error, or the control register is set to master reset mode.

Receiver Overrun

Bit 5 of the status register is the ovr bit. The ovr bit indicates a receiver overrun condition, i.e., one or more receiver data words have been overwritten in the input shift register. The overrun condition is considered to occur at the midpoint of the last received bit in the input shift register, when the previous word (in the RDR) has not yet been read by the microprocessor. However, the ovr bit is not set immediately when the overrun occurs, but is set when the valid word in the RDR is read.

Thus, when the overrun condition occurs, it is the input shift register data that is overwritten, not the RDR data.

The ovr bit is cleared when either the nreset signal is asserted, the data in the receiver data register is read, or the control register is set to master reset mode.

Parity Error

Bit 6 of the status register is the pe bit. When it is high, pe indicates that the parity bit received (over the rxdata input), does not match the parity calculated during the receive process. The pe bit is set when the data is written into the receiver data register. If no parity is selected, the parity error will not occur.

The pe bit is cleared when either the nreset signal is asserted, the data is read from the receiver data register, or the control register is set in master reset mode.

Interrupt Request

Bit 7 of the status register is the irq bit, the logical inverse of the nirq output. See "Interrupt Operation" on page 93 of this data sheet for more information.

Operation

This section describes the following:

- Bus interface operation
- Receiver operation
- Transmitter operation
- Interrupt operation
- Reset operation

Bus Interface Operation

A microprocessor or other controlling device accesses the a6850 through the bus interface, which provides a direct link to the transmit, receive, status, and control registers.

The microprocessor interfaces with the a6850 when the cs input is set to a logic 110 and the rnw input is set to a logic low when writing, or a logic high when reading. The rs input then chooses the appropriate register operation as shown in Table 7.

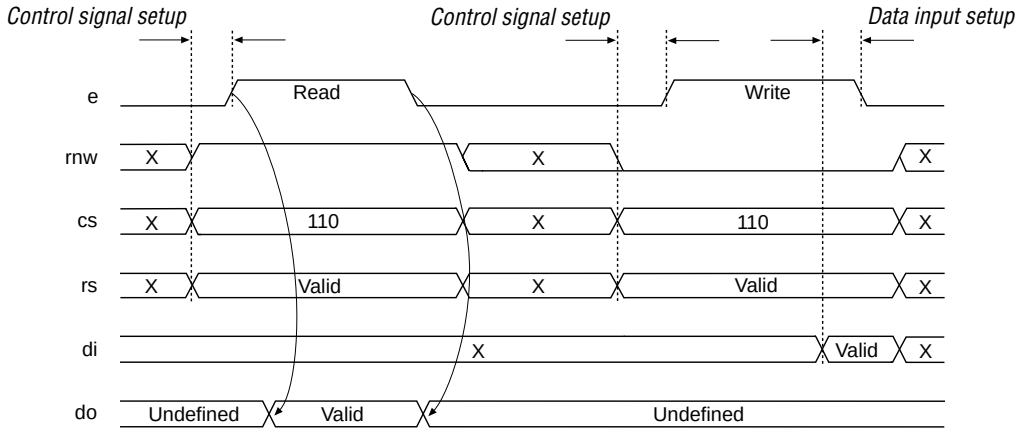
Table 7. Register Operations

rnw	rs	Register Operation
0	0	Control register write
0	1	Transmit data register write
1	0	Status register read
1	1	Receive data register read

When cs, rnw, and rs are set, access begins when the e input transitions from low to high. The e input must be high for at least one txclk cycle. In a read cycle, the data is available through the data output (do) bus on the rising edge of the e input. In a write cycle, the data is written on the falling edge of the e input. See Figure 3.

Figure 3. Read & Write Cycle Waveforms

The X indicates "don't care."



Receiver Operation

Receiver operation includes the following functions:

- Start bit detection
- Data bit sampling
- Parity & stop bit detection
- Error detection
- Receive data register transfer

Start Bit Detection

The a6850 begins receiving data when a start bit is detected. A start bit is a logic low over the rxdata input, and is sampled on each rising edge of the rxclk signal. Once the a6850 detects a logic low, it begins counting the logic low samples according to the specified divide-by mode (i.e., -1, -16, or -64).

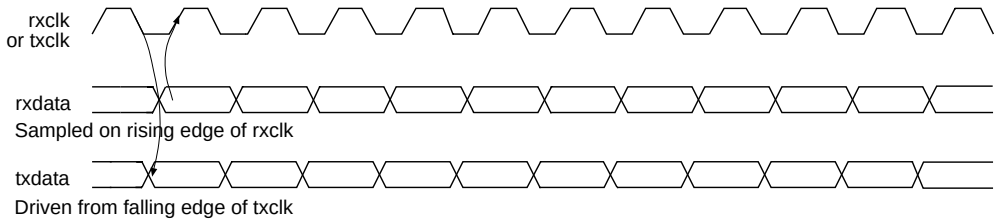
For example, after detecting a logic low in divide-by-1 mode, the a6850 assumes the next rising edge is data. After detecting a logic low in divide-by-16 mode, however, the a6850 counts 8 clock edges and samples again. The data must still be a logic low. At this point, the a6850 assumes the data and clock are synchronized, and samples data every 16 clock edges thereafter. Divide-by-64 mode is similar to divide-by-16, with the logic low sampled at the first rising edge and the 32nd rising edge of rxclk. Data is then sampled every 64 rising edges.

Data Bit Sampling

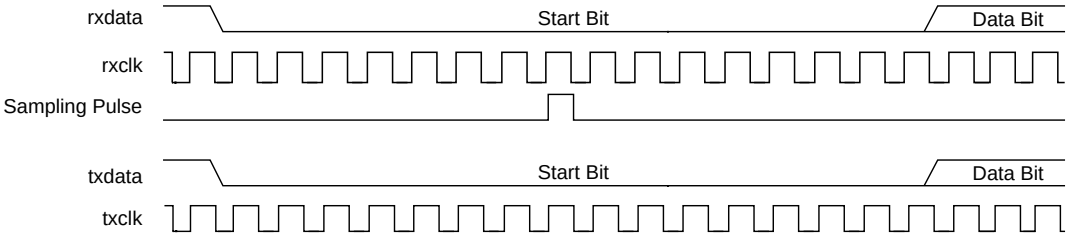
After detecting a logic low, the a6850 samples and shifts the data into the input shift register. Data bit sampling occurs on every rising edge in divide-by-1 mode, every 16 rising edges in divide-by-16 mode, and every 64 rising edges in divide-by-64 mode. Each time a bit is sampled, parity is calculated for future error detection. See Figure 4.

Figure 4. a6850 Receiver Functional Waveforms

Divide-by-1 Mode



Divide-by-16 Mode



Parity & Stop Bit Detection

The a6850 counts the number of data bits as it shifts. When the number of data bits received matches the number specified in the control register, the a6850 expects either a parity bit or a stop bit.

If parity is enabled, the a6850 samples for the parity bit, which is then processed for parity. However, if parity is not enabled, the a6850 samples for a stop bit (i.e., logic high). If a logic low is sampled, the fe bit is set in the status register.

The a6850 receives data with one or two stop bits. If one stop bit is specified in the control register, the a6850 will expect one stop bit before starting the synchronization process. Similarly, if two stop bits are specified, the synchronization process begins after detecting two stop bits.

Error Detection

Three errors can occur when receiving: framing, overrun, and parity. Refer to the status register error definitions on page 88 of this data sheet for more information.

Receive Data Register Transfer

Once the last stop bit is received or a framing error is detected, the data in the input shift register is transferred to the receiver data register. At this point, all status bits associated with this data word are set, including the rdrf bit. If receive interrupt is enabled, an interrupt on nirq is generated. The receive process concludes when the microprocessor reads data from the receiver data register.

Transmit Operation

The transmit operation includes the following functions:

- Transmit data register write/transfer
- Transmit start bit
- Transmit data
- Transmit parity bit
- Transmit stop bit

Transmit Data Register Write/Transfer

A transmit operation starts when the microprocessor writes data to the transmitter data register. In the initial write operation, if the output shift register is empty, data is immediately transferred and the shift operation begins. However, if a shift operation is underway, the data is held in the transmitter data register until the active shift operation is finished.

When data is in the transmitter data register, the tdre signal is cleared. Once the data is transferred to the output shift register, the tdre status bit is set. At this point, if transmit interrupt is enabled, an interrupt on nirq is generated.

Transmit Start Bit

After data is transferred to the output shift register, a start bit (i.e., logic low) is placed on the `txdata` output on the falling edge of `txclk`. The start bit stays active for the number of clock cycles specified by the divide-by mode (i.e., 1, 16, or 64).

Transmit Data

After the start bit, the data bits shift out of the register one at a time, from the least significant to the most significant. The cycle time for each bit starts at the beginning of the specified clock cycle (i.e., -1, -16, or -64). The number of bits shifted out corresponds to the number of bits specified in the control register.

Transmit Parity Bit

If parity is enabled, the bit following the last data bit is a parity bit. The parity bit has a value that forces all the data to have the correct parity. For example, if parity is set to odd in the control register, then the parity bit guarantees there are an odd number of 1s (i.e., data plus the parity bit). If parity is set to even in the control register, then the parity bit guarantees there is an even number of 1s (i.e., data plus the parity bit).

Transmit Stop Bit

After the parity bit is transmitted, or the last data bit if parity is not enabled, one or two stop bits are transmitted on `txdata` output. The output then stays high until the beginning of the next data word transmission.

Interrupt Operation

The `nirq` output is designed to be an interrupt to a microprocessor or other controlling device. The `nirq` outputs a variety of conditions including transmit and receive.

The transmit operation produces an interrupt (i.e., logic low on nirq) when the following conditions all occur:

- Transmit interrupts are enabled.
- The tdre flag is set.
- The ncts signal is low.

The receive operation produces an interrupt when the following conditions occur:

- Receive interrupts are enabled (i.e., the rie control signal is high).
- Any one of the following signals is set: rdrf, ovr, or ndcd.

Reset Operation

The a6850 is reset in one of two ways:

- Driving the nreset input low.
- Writing logic 1s into the cds bits of the control register.

The nreset input is used as an asynchronous clear to all internal registers. Placing the a6850 into master reset will synchronously clear the registers. However, master reset only works if both clocks are running.

Variations & Clarifications

The following characteristics distinguish the Altera® a6850 from the Motorola MC6850 device:

- The a6850 has separate input and output data buses, while the MC6850 device has a single tri-state data bus.
- The nreset (asychronous reset) input on the a6850 is not available in the Motorola MC6850 device.
- The a6850 bus interface was designed using synchronous design techniques, allowing it to operate using various part designations, speed grades, and optimization techniques.
- The a6850 requires that the txclk signal is always connected to a free running clock, and that the e signal is high for at least one txclk clock cycle when reading and writing data.