Low Voltage Voice Coil Motor Driver

Features and Benefits

- WLCSP package for minimum footprint
- Ramp control circuit
- Fixed I²C logic thresholds
- 10-bit D-to-A converter
- 100 µA resolution
- Low voltage I²C serial interface
- Low current draw sleep mode-active low
- 2.3 to 5.5 V operation

Applications:

- Camera focus motor

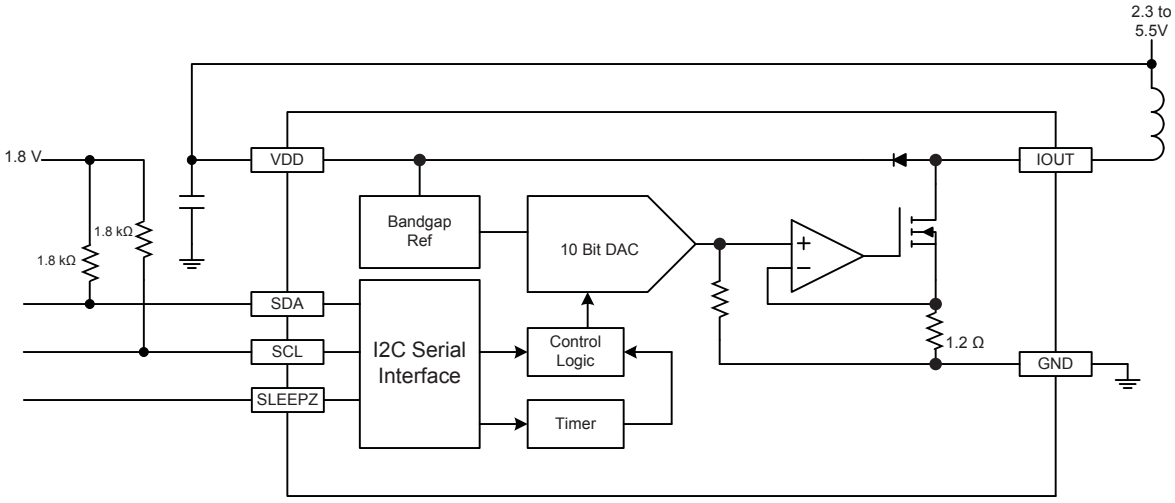
Package: 6-Bump Chip Scale Package (suffix CG)

Description

Designed for linear control of small form factor voice coil motors, the A3907 is capable of peak output currents to 102 mA and operating voltages to 5.5 V.

Internal circuit protection includes thermal shutdown with hysteresis, flyback clamp diode, and undervoltage monitoring of V_{DD}.

Functional Block Diagram



Selection Guide

Part Number	Packing	Package	Pb-free
A3907ECGTR	4000 pieces per reel	Bumped wafer-level chip-scale package (WLCSP)	Pb-free chip with high-temperature solder balls (RoHS compliant)

Absolute Maximum Ratings

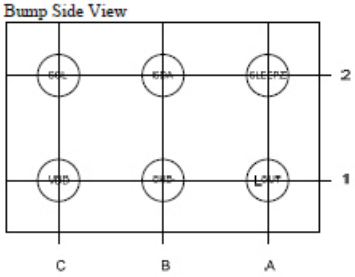
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{DD}		6	V
Logic Input Voltage Range	V_{IN}		–0.3 to V_{DD} + 0.3	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–40 to 150	ºC

Thermal Characteristics

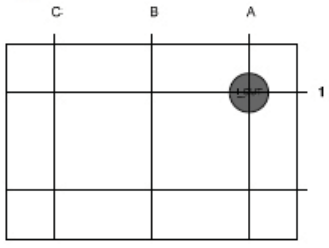
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	64	ºC/W

*Additional thermal information available on the Allegro website

Bump Side View



Top Side View



Pin Name	Pin Description	
IOUT	Sink Drive Output	A1
SLEEPZ	Standby Mode Control	A2
GND	Ground	B1
SDA	I^2C data	B2
VDD	Power Supply In	C1
SCL	I^2C clock	C2

ELECTRICAL CHARACTERISTICS Valid at T_A = 25°C, V_{DD} = 2.3 to 5.5 V; unless otherwise noted

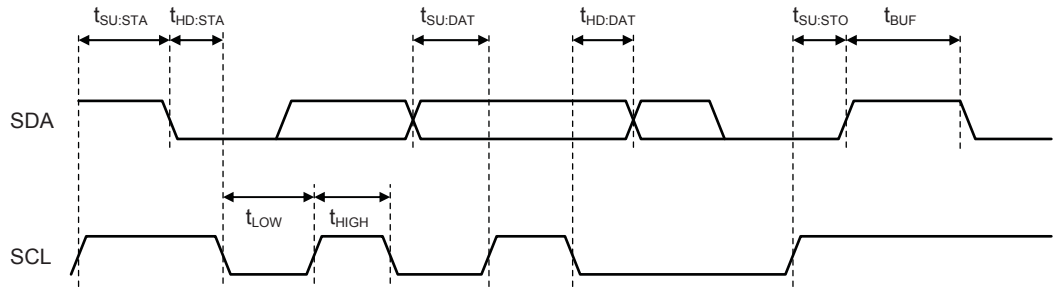
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Current	I_{DD}		–	0.5	2	mA
		Sleep Mode (SLEEPZ = low), V_{DD} = 2.3 to 3.5 V	–	< 100	500	nA
UVLO Enable Threshold	$V_{UVLO(th)}$	V_{DD} rising	–	2	2.295	V
UVLO Hysteresis	$V_{UVLO(hys)}$		–	100	–	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = T_{JTSD} - $T_{JTSD(hys)}$	–	15	–	°C
Power-Up Delay	t_{dPO}		–	10	–	µs
D-to-A Converter						
Resolution	Res	Target = 100 µA/LSB	–	10	–	bit
Relative Accuracy	err_{INL}	Code = 64 to 1023, Endpoint method	–	±4	–	LSB
Differential Nonlinearity	err_{DNL}	Guaranteed monotonic	–	–	±1	LSB
Maximum Output Current	I_{MAX}	Code = 1023	–	102.3	–	mA
Gain Error	err_A	T_J = 25°C, Code 64 to 1023, V_{DD} = 2.6 to 3.0 V	–10	< 3	10	%FS
Gain Error Drift[1]	Δerr_A	T_J = –40°C to 125°C	–	0.2	–	LSB/°C
Minimum Code Error	I_{OS1}	Code = 1	0	1	5	mA
Offset Error	I_{OS}	Code = 64	–	0.5	–	mA
Output						
Slew Rate Timer	err_{TS}	Relative to target value	–10	–	10	%
Output Voltage Range	V_{OUT}		0.35	–	V_{DD}–0.1	V
Output On Resistance	$R_{DS(on)}$	R_{SENSE} + R_{SINK}, I_{OUT} = 102.3 mA	–	2	–	Ω
I²C Interface						
Bus Free Time Between Stop and Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Repeated Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	900	–	ns

ELECTRICAL CHARACTERISTICS (continued) Valid at T_A = 25°C, V_{DD} = 2.3 to 5.5 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
I²C Interface						
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	µs
Logic Input (SDA, SCL Pins) Low Level	V_{IL}		–	–	0.84	V
Logic Input (SDA, SCL Pins) High Level	V_{IH}		1.26	–	–	V
$\overline{\text{SLEEP}}$ Pin Input Low Level	V_{SLPINL}		–	–	0.7	V
$\overline{\text{SLEEP}}$ Pin Input High Level	V_{SLPINH}		1.5	–	–	V
Input Hysteresis	V_{HYS}	SDA and SCL only	–	100	–	mV
Logic Input Current	I_{IN}	V_{IN} = 0 V to V_{DD}	–1	0	1	µA
SDA Pin Output Voltage	V_{OL}	I_{LOAD} = 1.5 mA	–	–	0.36	V
SCL Clock Frequency	f_{CLK}		–	–	400	kHz
SDA Output Fall Time	t_{OF}	V_{IH} to V_{IL}	–	–	250	ns

[1]Assured by design and characterization, not production tested.

I²C Timing Diagram



Functional Description

Output Current Level Control

The A3907 output current level, I_{OUT}, is controlled dynamically by programming the D-to-A converter (DAC) value via the I^2C serial port. A 10-bit Level Control code, having a decimal equivalent value from 0 through 1023, is clocked into the SDA pin.

The target output current can be calculated by:

$$I_{OUT} = n_{DAC} \times 100\ \mu A\ , \qquad (1)$$

where n_{DAC} is the decimal equivalent of the Level Control code. For example, a code of 5 (00000101_2) sets an output current target of 500 µA.

Programming Level Control code 0 disables the output sink drive. In addition, the DAC is automatically set to code 0 at power-up and also at a fault condition on VDD.

Output Current Slew Rate Control

When a new current level control instruction is received on the SDA input, the A3907 moves to the new target currrent level by incrementing or decrementing through each of the intermediate current levels until it arrives at the new programmed value.

The control instruction received at the SDA input includes both the 10-bit Level Control code and a 4-bit Ramp Control code. The Level Control code is used to determine the absolute value of the changes in I_{OUT} (see equation 1), and the Ramp Control code maps to a lookup table of time intervals (represented in table 1). Together, these two codes determine the shape of the current level change function.

Step or Ramp Function The A3907 can change to the new target level using either a step or a ramp slew rate function. When a step function is selected, the A3907 moves to the new target level without imposing any additional time delays between DAC updates. To select a step function, program one of the four Ramp Control codes in table 1 that disable the ramp feature.

When a ramp function is selected, the A3907 imposes time delays between each DAC update, calculated according to the particular function option selected. To select a ramp function, program one of the twelve Ramp Control codes in table 1 that enable the ramp feature.

Single or Dual Subintervals For either the step or the ramp slew rate method, the total change can be accomplished in either one continuous time interval, or divided over two sequential time subintervals. When the single-interval method is selected, the total change in I_{OUT} is accomplished over the total time interval determined by the Rate Control code in table 1, calculated as follows:

$$Code_T = |(Code_{NewTarget} - Code_{PreviousTarget})| / 2\ , \qquad (2)$$

and

$$T = Code_T \times\ t_{dT}\ , \qquad (3)$$

where t_{dT} is the delay factor, in table 1.

When the dual-subintervals method is selected, the elapsed time for each subinterval is determined separately by the Rate Control code in table 1. The time interval from initiation, T0, to the switchover point, T1, is calculated as follows:

$$Code_{Switchover} = |(Code_{NewTarget} - Code_{PreviousTarget})| / 2\ , \qquad (4)$$

and

$$T1 = Code_{Switchover} \times\ t_{dT1}\ , \qquad (5)$$

where t_{dT1} is the delay factor for the initial time subinterval, in table 1.

The current amplitude at the switchover point is calculated based on equation 1, as follows:

$$I_{Switchover} = (Code_{Low} + Code_{Switchover}) \times 100\ \mu A\ , \qquad (6)$$

where $Code_{Low}$ is the lesser of $Code_{NewTarget}$ and $Code_{PreviousTarget}$.

The time interval from the switchover point, T1, until the target current level is reached, T2, is calculated as follows:

$$T2–T1 = Code_{Switchover} \times\ t_{dT2}\ , \qquad (7)$$

where t_{dT2} is the delay factor for the second time subinterval, in table 1.

Output Function Programming

Two examples of output level and slew rate programming are shown in figure 1. Both examples are ramp slew rate functions, using the dual-subinterval method. In example A, an increment in I_{OUT} is shown, and example B shows a decrement in I_{OUT}.

Example A

- The A3907 has been previously programmed to Level Control code 100 (1100100_2), for a target I_{OUT} of 100 × 100 µA = 10 mA (equation 1).
- The new target current level is 20 mA, so Level Control code 200 (11001000_2) is programmed (invert equation 1).
- For this example, the slew rate function selected is represented by Ramp Control code 1100_2 : ramp, dual-subinterval, initial subinterval delay factor 781 ns, second subinterval delay factor 50 µs.
- The A3907 determines the switchover point, T1, as follows:

$Code_{Switchover} = |(200 – 100)|/2 = 50$ (equation 2),

$T1 = 50 \times 0.781\ \mu s = 39\ \mu s$ (equation 5),

$I_{T1} = 50 + 100 \times 100\ \mu A = 150\ \mu A$ (equation 6).

- The A3907 determines the target time final point, T2, as follows:

$Code_{Switchover} = |(200 – 100)|/2 = 50$ (equation 2) ,

$T2–T1 = 50 \times 50\ \mu s = 2.5$ ms (equation 5).

Example B

- The A3907 has been previously programmed to Level Control code 1000 (1111101000_2), for a target I_{OUT} of 1000 × 100 µA = 100 mA (equation 1).

Table 1. Slew Rate Function Table

Slew Rate Method	Timer Bits Settings				Delay Factor (µs)	
	T3	T2	T1	T0	t_{dT}	
Single Interval	0	0	0	0	0 (ramp feature disabled)	
	0	0	0	1	6.25	
	0	0	1	0	12.5	
	0	0	1	1	25	
	0	1	0	0	50	
	0	1	0	1	100	
	0	1	1	0	200	
	0	1	1	1	0 (ramp feature disabled)	
Dual Interval	T3	T2	T1	T0	t_{dT1}	t_{dT2}
	1	0	0	0	0 (ramp feature disabled)	
	1	0	0	1	0.781	6.25
	1	0	1	0		12.5
	1	0	1	1		25
	1	1	0	0		50
	1	1	0	1		100
	1	1	1	0		200
	1	1	1	1	0 (ramp feature disabled)	

- The new target current level is 30 mA, so Level Control code 300 (100101100_2) is programmed (invert equation 1).
- For this example, the slew rate function selected is represented by Ramp Control code 1101_2 : ramp, dual-subinterval, initial subinterval delay factor 781 ns, second subinterval delay factor 100 µs.
- The A3907 determines the switchover point, T2, as follows:

$Code_{Switchover} = |(1000 – 300)|/2 = 350$ (equation 2),

$T1 = 350 \times 0.781\ \mu s = 273\ \mu s$ (equation 5),

$I_{T1} = 350 + 300 \times 100\ \mu A = 65\ \mu A$ (equation 6).

- The A3907 determines the target time final point, T1, as follows:

$Code_{Switchover} = |(1000 – 300)|/2 = 350$ (equation 2) ,

$T2–T1 = 350 \times 100\ \mu s = 35$ ms (equation 5).

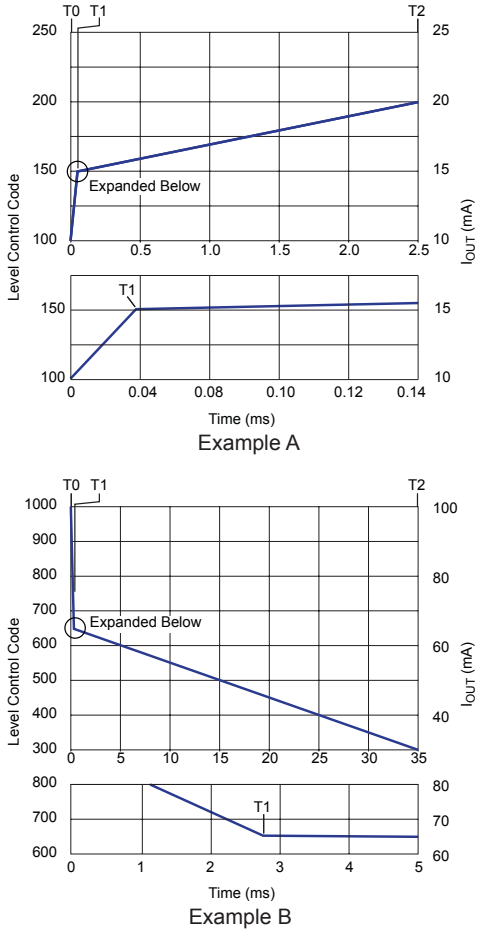


Figure 1. Examples of programmed I_{OUT} change

I²C Interface

This is a serial interface that uses two bus lines, SCL and SDA, to access the internal control registers. Data is exchanged between a microcontroller (master) and the A3907 (slave). The clock input to SCL is generated by the master, while SDA functions as either an input or an open drain output, depending on the direction of the data. The I²C input thresholds do not depend on the VDD voltage of the A3907. The levels are fixed at approximately 1V. The fixed levels allow the SDA and SCL lines to be pulled-up to a different logic level than the VDD supply of the 3907.

Timing Considerations The control sequence of the communication through the I²C interface is composed of several steps in sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.

2. Address Cycle. 7 bits of address, plus 1 bit to indicate write (0) or read(1), and an acknowledge bit. The address setting is 0x18, 0x1A, 0x1C, or 0x1E.

3. Data Cycles. Write requires 7 bits of address data selecting the internal control register, followed by an acknowledge bit.

4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A3907 always responds by resetting the data transfer sequence.

To indicate a write cycle, the Read/Write bit is set to low. Mulitple writes are allowed. If desired, the readback bit can be set to high to check what was last written.

The Acknowledge bit is used by the master to determine if the slave device is responding to its address and data transmissions. When the A3907 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A3907 pulls SDA low during the clock cycle that follows the last data byte, in order to indicate that the data has been successfully received. In both cases, the master device must release the SDA line before the ninth clock cycle, in order to allow this handshaking to occur.

Slave (A3907) Address

Device Identifier							R/W
0	0	0	1	1	X	X	0

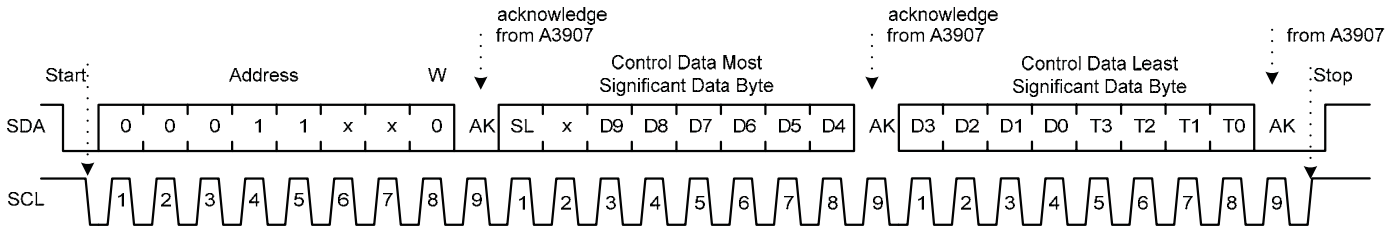
Control Register MS Byte (I²C Write register)

Bit	Name	Function
0	D4	DAC
1	D5	DAC
2	D6	DAC
3	D7	DAC
4	D8	DAC
5	D9	DAC MSB
6	T5	Not used
7	SLEEP	1=Sleep 0=Normal

Control Register MS Byte (I²C Write register)

Bit	Name	Function
0	T0	Time Setting LSB
1	T1	Time Setting Bit 1
2	T2	Time Setting Bit2
3	T3	Time Setting Bit 3
4	D0	DAC LSB
5	D1	DAC
6	D2	DAC
7	D3	DAC

Write Operation



Output Voltage Range

To guarantee the accuracy and linearity of the programmed current, the voltage on the IOUT pin, V_{OUT}, should be greater than 350 mV. The output voltage is a function of the battery voltage, motor resistance, and the programmed load current, I_{OUT}.

Clamp Diode

When the IC output is turned off, the load inductance causes the output voltage, V_{OUT}, to rise. An internal clamp diode, connected between the IOUT and VDD pins, is integrated into the IC to ensure the output voltage remains at a safe level.

$\overline{\text{SLEEP}}$ Pin

The $\overline{\text{SLEEP}}$ pin is an active low input. A logic low signal disables all of the internal circuitry and prevents the IC from draining battery power.

Applications Information

Headroom

The current may not reach the programmed level if there is not adequate headroom in the output circuit. The IC output voltage must be over 350mV to guarantee normal linear operation. V_{DD}, I_{LOAD}, and R_{LOAD} can be adjusted to ensure the device operates in the linear range. When equation 7 is not satisfied, the load current will be limited by the series impedance and may not reach the programmed level.

$$V_{DD}(\text{min}) - R_{LOAD}(\text{max}) \times I_{OUT}(\text{max}) \geq 350 \text{ mV} \quad . \qquad (7)$$

I_{OUT} Errors Defined

Relative Accuracy (INL) This error is calculated by measuring the worse case deviation from a straight line defined from endpoints. The straight line endpoints are defined by the actual measured values at Level Control code 63 and 1023 (see figure 2).

Differential Nonlinearity (DNL) A measure of the monotonicity of the DAC (see equation 8). The slope of the line must always be positive for each incremental step.

$$\text{DNL} = (I_{OUT}(n+1) - I_{OUT}(n)) / \text{LSB} \quad , \qquad (8)$$

where (n = 64 to 1023). DNL should be < 1 LSB.

Offset Error The measured output current at Level Control code 64, compared to the ideal value according to the transfer function: 6.4 mA.

Gain Error The difference between the slopes of the ideal transfer function and the actual transfer function. The gain error is calculated by subtracting the offset error at Level Control code 16 from the actual transfer function. This calculated value is compared to the ideal transfer function and reported as a percentage of the ideal full scale value: 102.3 mA (see figure 3).

Gain Error Drift The change in slope of the transfer function due to temperature, expressed as LSB / °C.

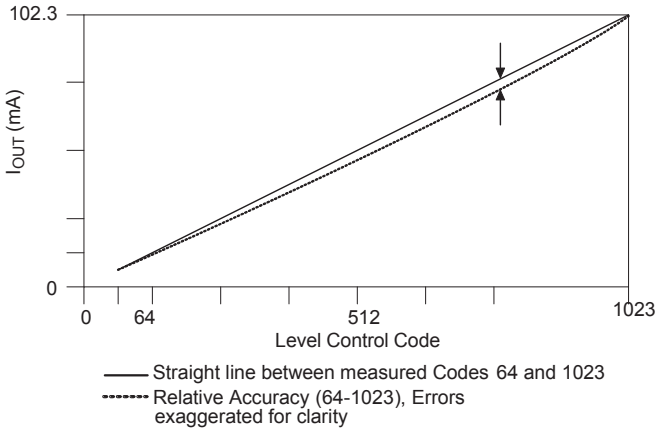


Figure 2. Relative Accuracy

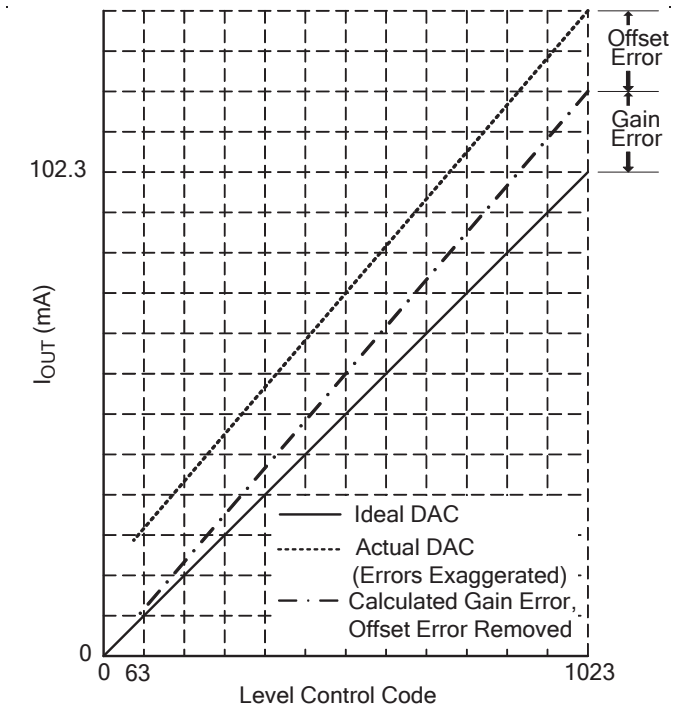
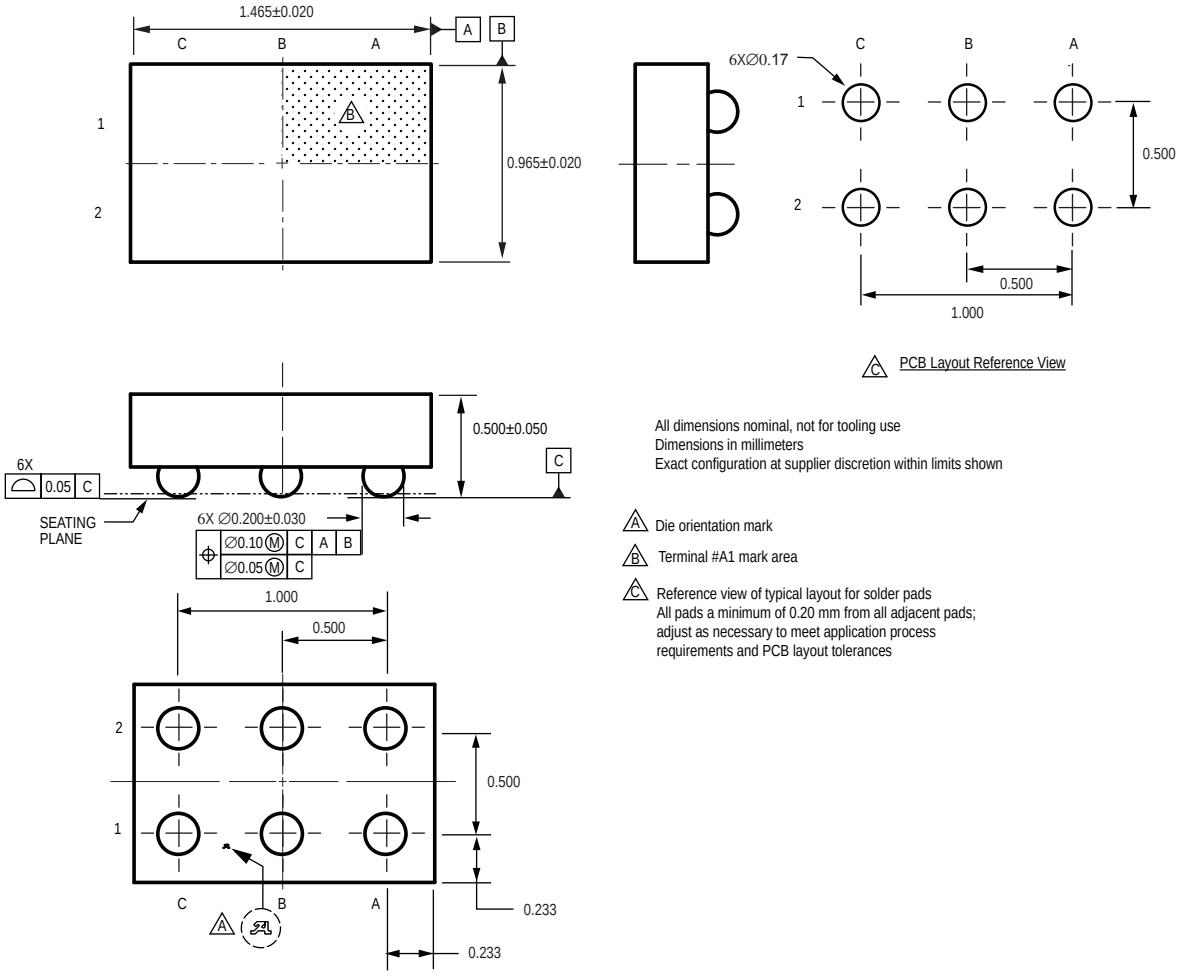


Figure 3. Gain Error

CG Package, 6-Ball WLCSP



All dimensions nominal, not for tooling use
Dimensions in millimeters
Exact configuration at supplier discretion within limits shown

A Die orientation mark

B Terminal #A1 mark area

C Reference view of typical layout for solder pads
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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