Broadband wire bondable / Embedding Silicon Capacitor
BBEC 0201M 10nF BV11

Rev. 2.00

General description

BBEC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The BBEC is suitable for DC decoupling, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.
These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 10nF in a SMT 0201M. The BBEC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
BBEC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (70ppm/K).

Assembly: Suitable for Wire bonded or embedded applications through existing laminated packages (LGA, BGA) or rigid PCB, FR4 (laminate) or flex platforms.

Pads finishing: Min 3µm Aluminium for wire bonding, other finishing available on request such as thin copper for embedding.

Key features

- Broadband performance up to 40 GHz
- Resonance free
- Phase stability
- Insertion loss < 0.5dB Typ. up to 40 GHz.
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 100 µm
- Break down voltage : 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0201 footprint

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency *(i.e.* capacitance *per unit* volume)
- Broadband test equipment

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Functional diagram

The next figure provides implementation set-up diagram.

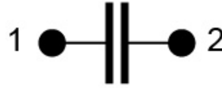

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	10	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.1	%/V_{DC}
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
Fc-3dB	Cut-off frequency at 3dB (6)	@+25°C	-	160	187	kHz
IL	Insertion loss (6)	@ 20 GHz, +25°C	-	0.35	-	dB
		@ 40 GHz, +25°C	-	0.5	-	dB
RL	Return loss (6)	Up to 40 GHz, +25°C	11	-	-	dB
ESD	HBM stress (7)	JS-001-2017	8	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request.
(2): without packaging.
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation.
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation.
(6): with wire bonding de-embedded between 2 microstrip lines
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.

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Module of S-parameters of 10nF BBEC
in transmission mode (with wire bounding de-embedded)

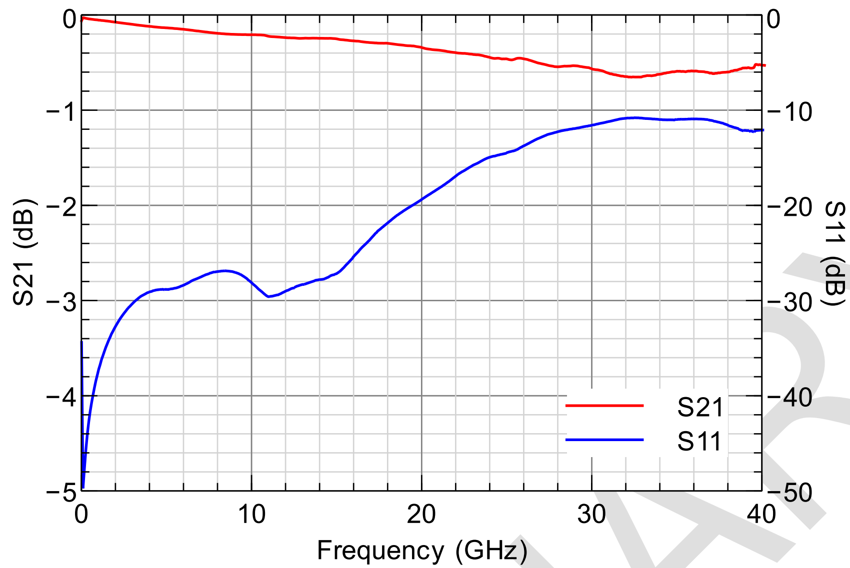

Figure 2 - 10nF BBEC measurement results (module of S-parameters)

Schematic of 10nF BBEC
in transmission mode

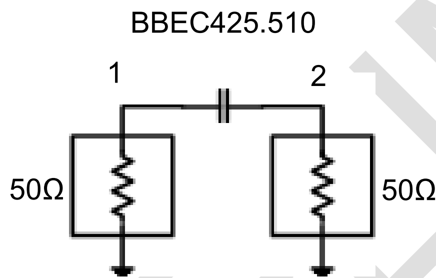

Figure 3 - 10nF BBEC measurement schematic

Example of 0201M wire bonded

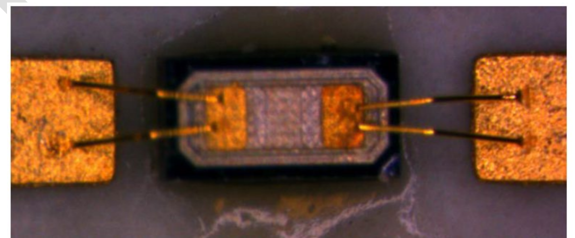

Figure 4 – micro picture of BBEC mounted on board in microstrip mode

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Pinning definition

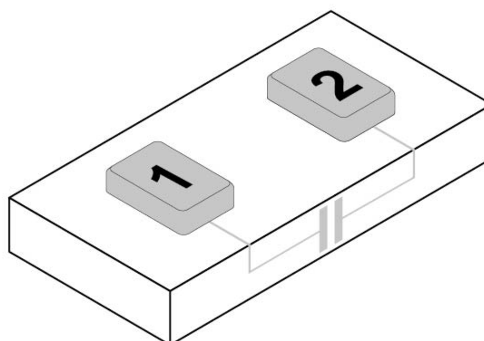

Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-150.0 / 0.0
2	Signal	150.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Regardless of packaging, Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Type number	Package		
	Packaging	Finishing	Description
939132425510-W0A	Waffle Pack 400	Al(1)	BBEC 0201M - 10nF – 2 pads – 0.6 x 0.3 mm x 0.10mm (2)

(1) Al = Min 3µm Aluminium
(2) Refer to Figure 7

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
BBEC425.510	XEM0201510	BBEC 10nF/0201M/BV11 – 2 pads – 0.6 x 0.3 x 0.10 mm

Table 4 - Die information

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Pad Metallization

This wire bonding / embedding Silicon Capacitor is delivered as standard with Aluminum pads.

Other Metallization, such as Copper or thick Gold pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

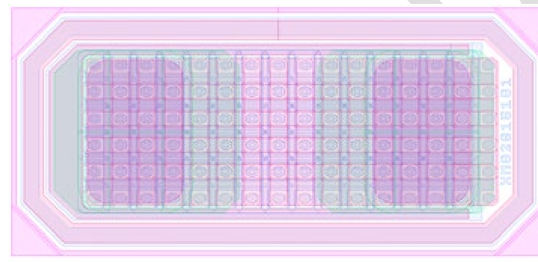

Figure 6 – Layout view

L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
0.60 ±0.02	0.30 ±0.02	0.10 ±0.01	0.10	0.20	0.15	0.003(1) 0.005(2)

(1) Standard Al for wire bonding application.
(2) Standard Cu for *embedding application*

Table 5 - Dimensions and tolerances

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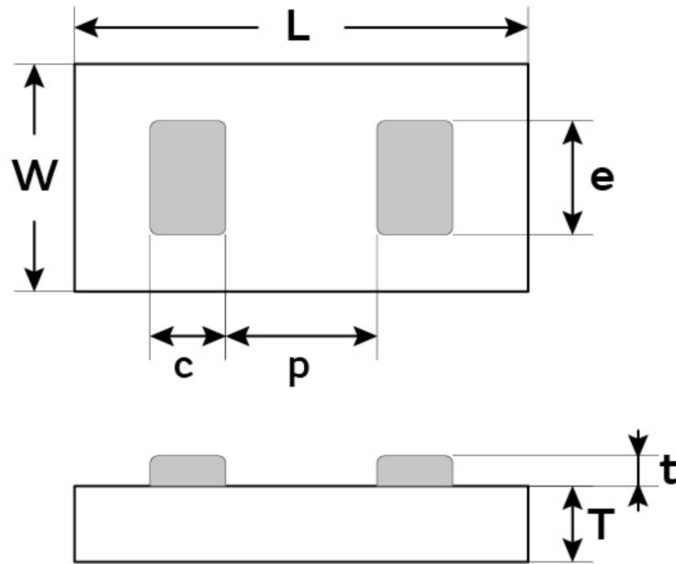

Figure 7 - Package outline drawing

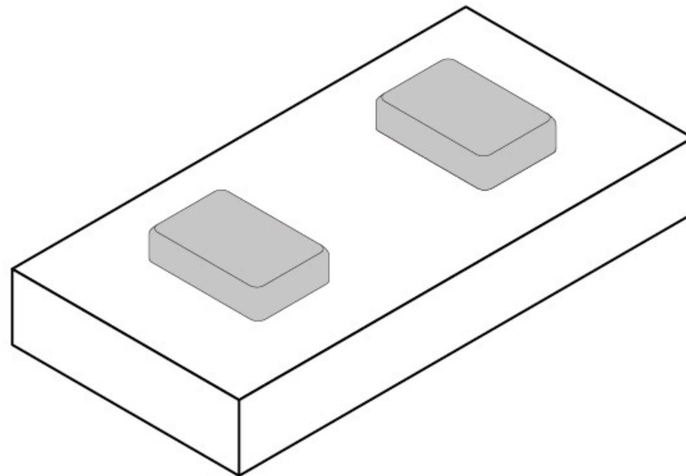

Figure 8 Isometric top view

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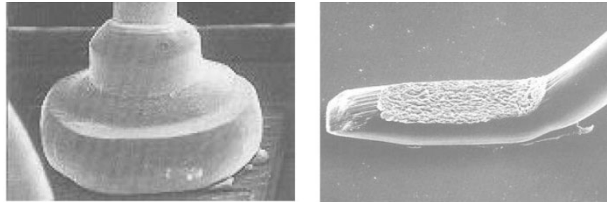
Assembly

BBEC series is compatible with standard wire bonding assembly (ball and wedge) technology. It can be directly mounted on the PCB using standard.



Ball bond Wedge bond

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page

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Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Waffle pack:

Please refer to application note 'Waffle Pack Chip Carrier Handling & Opening Procedure'. Dies are not flipped in the waffle pack cavity (wire bond pad up).

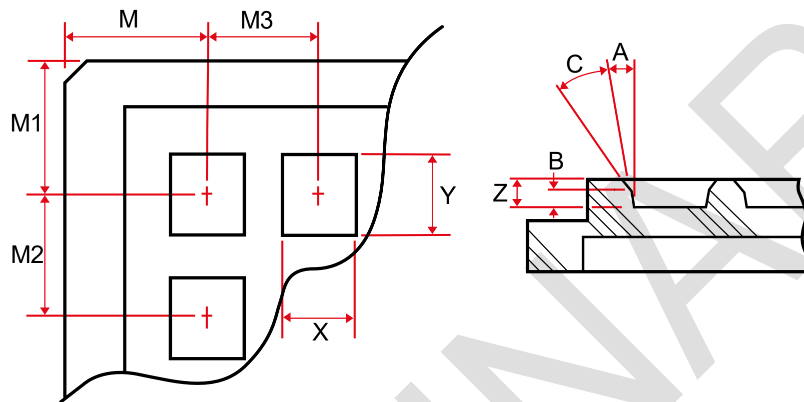

Table 6 - Waffle pack drawing

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	0.74 ±0.05	0.43 ±0.05	0.28 ±0.05

Table 7 - Waffle pack dimensions (mm)

M	M1	M2	M3	A
4.39 ±0.08	4.65 ±0.08	2.18 ±0.05	2.21 ±0.05	7° ±1/2°

Table 8 - Waffle pack dimensions (mm)

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Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values: Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information: Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author.
Release 1.01	**2021 May 10th**	**Content and Layout**	**SCA; CGU; LLE; SJA, OGA**
Release 2.00	**2021 June 18th**	**Preliminary release**	**SCA; CGU; LLE; SJA, OGA**

Disclaimer / Life support applications

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www.murata.com
mis@murata.com