NEC

MOS INTEGRATED CIRCUIT

μPD78F0988A, 78F0988A(A)

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F0988A and 78F0988A(A) are products in the μPD780988 Subseries in the 78K/0 Series that have flash memory in the place of the internal ROM of the μPD780988. Flash memory can be written or erased electrically with the device mounted on the board. Therefore, the μPD78F0988A and μPD78F0988A(A) are ideal for evaluation in system development, small-scale production, or systems likely to be upgraded frequently.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780988 Subseries User's Manual: U13029E
78K/0 Series Instruction User's Manual: U12326E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 60 KB[Note 1]
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes[Note 2]
- Operable in the same supply voltage range as the mask ROM version (V_{DD} = 4.0 to 5.5 V)

Notes 1. The capacity of the flash memory can be changed with the internal memory size switching register (IMS).
2. The capacity of the internal expansion RAM can be changed with the internal expansion RAM size switching register (IXS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0988A AND MASK ROM VERSIONS.**

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD78F0988ACW	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electrical equipment)
μPD78F0988AGC-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electrical equipment)
μPD78F0988AGC-8BS	64-pin plastic LQFP (14 × 14)	Standard (for general electrical equipment)
μPD78F0988AGC(A)-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical equipment)
μPD78F0988AGC(A)-8BS	64-pin plastic LQFP (14 × 14)	Special (for high-reliability electrical equipment)

For details of the quality grade and its application fields, refer to **Quality Grades on NEC Semiconductor Devices (C11531E)**.

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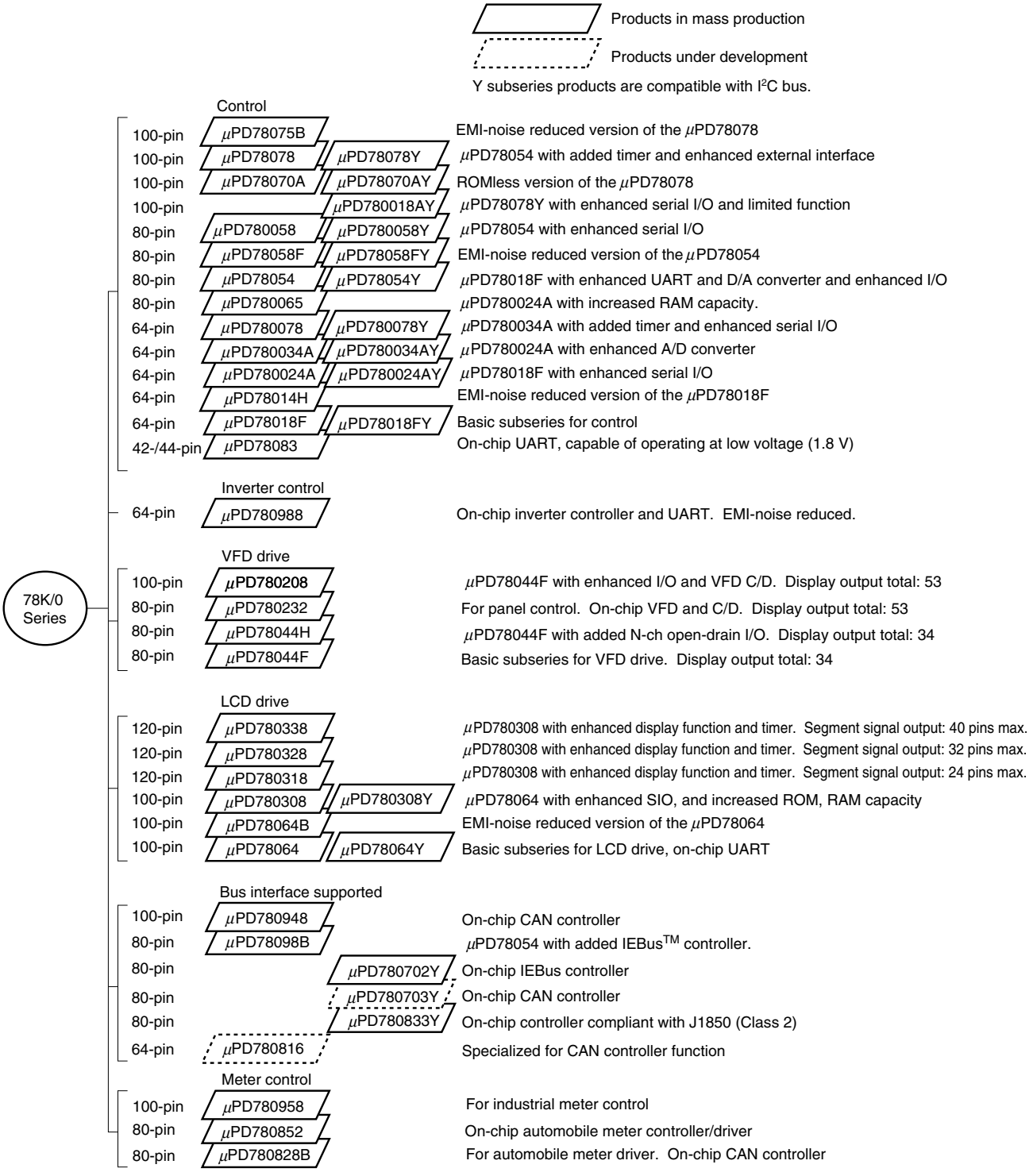
78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences between the subseries are shown below.

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K									59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	Flash memory	60 KB[Note 1]
	High-speed RAM	1024 bytes
	Expansion RAM	1024 bytes[Note 2]
Memory space		64 KB
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time variable function 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38 MHz operation with system clock)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total: 47 • CMOS inputs: 8 • CMOS I/O: 39
Real-time output ports		• 8 bits × 1 or 4 bits × 2 • 6 bits × 1 or 4 bits × 1
A/D converter		• 10-bit resolution × 8 channels • Power supply voltage: AV_{DD} = 4.0 to 5.5 V
Serial interface		• UART mode: 2 channels • 3-wire serial I/O mode: 1 channel
Timer		• 16 bit timer/event counter: 2 channels • 8-bit timer/event counter: 3 channels • 10-bit inverter control timer: 1 channel • Watchdog timer: 1 channel
Timer output		11 (general-purpose outputs: 5, inverter control outputs: 6)
Vectored interrupt sources	Maskable	Internal: 16, external: 8
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.0 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		• 64-pin plastic SDIP (19.05 mm (750))[Note 3] • 64-pin plastic QFP (14 × 14) • 64-pin plastic LQFP (14 × 14)

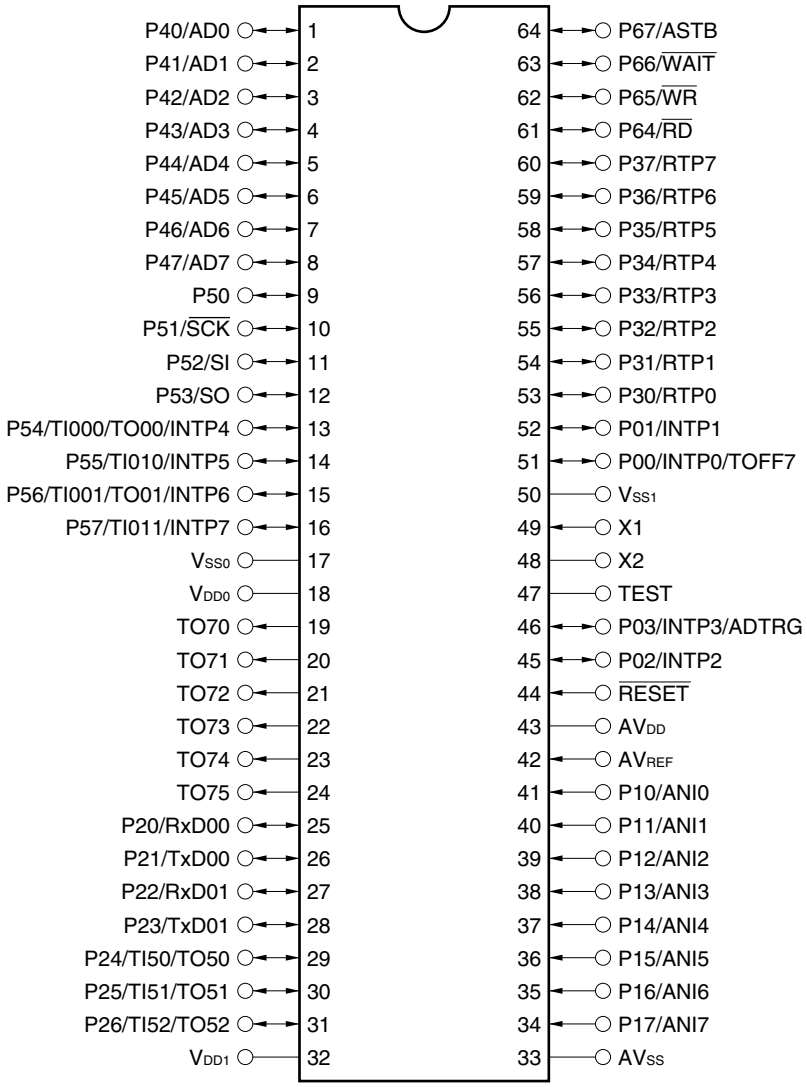
Notes 1. The capacity of the flash memory can be changed with the internal memory size switching register (IMS).

2. The capacity of the internal expansion RAM can be changed with the internal expansion RAM size switching register (IXS).

3. Standard quality grade products only.

PIN CONFIGURATION (TOP VIEW)

- **64-Pin Plastic SDIP (19.05 mm (750))**
  μPD78F0988ACW



Cautions 1. In the normal operation mode, connect the V_{PP} pin directly to V_{SS0}.

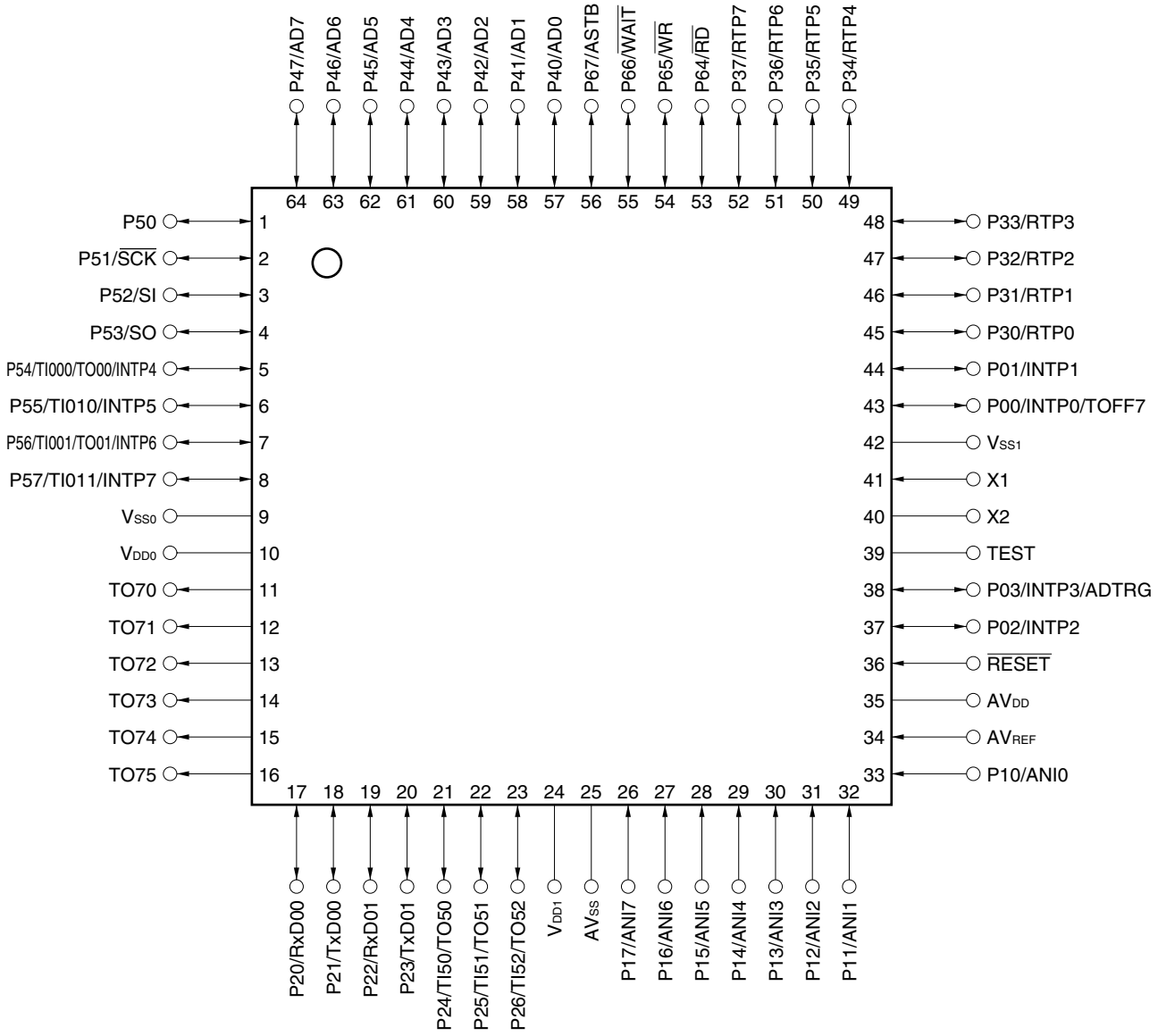
2. In the flash memory writing mode, connect the V_{PP} pin to V_{SS0} via a 10 kΩ pull-down resistor.

3. The 64-pin plastic SDIP (19.05 mm (750)) package is not provided for special quality grade products.

Remark When the μPD78F0988A and 78F0988A(A) are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-pin plastic QFP (14 × 14)**
  μPD78F0988AGC-AB8, 78F0988AGC(A)-AB8

- **64-pin plastic LQFP (14 × 14)**
  μPD78F0988AGC-8BS, 78F0988AGC(A)-8BS



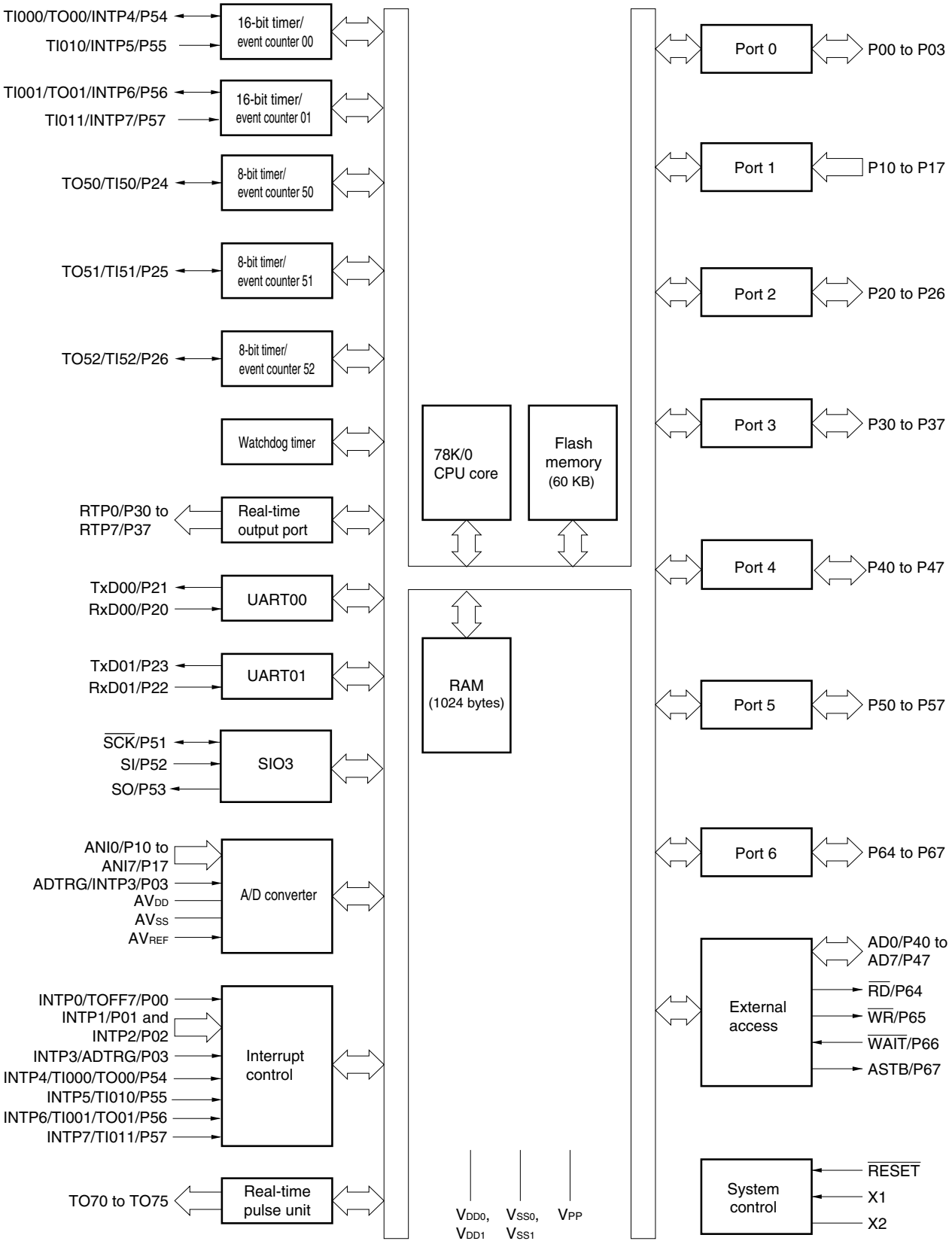
Cautions 1. In the normal operation mode, connect the V_{PP} pin directly to V_{SS0}.

2. In the flash memory writing mode, connect the V_{PP} pin to V_{SS0} via a 10 kΩ pull-down resistor.

Remark When the μPD78F0988A and 78F0988A(A) are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

AD0 to AD7: Address/data bus
ADTRG: AD trigger input
ANI0 to ANI7: Analog input
ASTB: Address strobe
AV_{DD}: Analog power supply
AV_{REF}: Analog reference voltage
AV_{SS}: Analog ground
INTP0 to INTP7: External interrupt input
P00 to P03: Port 0
P10 to P17: Port 1
P20 to P26: Port 2
P30 to P37: Port 3
P40 to P47: Port 4
P50 to P57: Port 5
P64 to P67: Port 6
$\overline{RD}$: Read strobe
$\overline{RESET}$: Reset
RTP0 to RTP7: Real-time port
RxD00, RxD01: Receive data
$\overline{SCK}$: Serial clock
SI: Serial input
SO: Serial output
TI000, TI001, TI010, TI011, TI50 to TI52: Timer input
TO00, TO01, TO50 to TO52, TO70 to TO75: Timer output
TOFF7: Timer output off
TxD00, TxD01: Transmit data
V_{DD0}, V_{DD1}: Power supply
V_{PP}: Programming power supply
V_{SS0}, V_{SS1}: Ground
$\overline{WAIT}$: Wait
$\overline{WR}$: Write strobe
X1, X2: Crystal

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78F0988A AND MASK ROM VERSIONS

The μPD78F0988A is a product with a flash memory which enables on-board writing, erasing and rewriting of programs.

Except for flash memory specifications, the same functions as those of mask ROM versions can be obtained by setting the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Table 1-1 shows the differences between the flash memory version (μPD78F0988A) and mask ROM versions (μPD780982, 780983, 780984, 780986, 780988).

Table 1-1. Differences Between μPD78F0988A and Mask ROM Versions

Item	μPD78F0988A	Mask ROM Versions
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacities	60 KB	μPD780982: 16 KB μPD780983: 24 KB μPD780984: 32 KB μPD780986: 48 KB μPD780988: 60 KB
Internal expansion RAM capacities	1024 bytes	μPD780982: None μPD780983: None μPD780984: None μPD780986: 1024 bytes μPD780988: 1024 bytes
Change of internal ROM capacity with internal memory size switching register (IMS)	Available[Note 1]	Not available
Change of internal expansion RAM capacity with internal expansion RAM size switching register (IXS)	Available[Note 2]	Not available
TEST pin	Not provided	Provided
V_{PP} pin	Provided	Not provided

Notes 1. Flash memory capacity becomes 60 KB by $\overline{\text{RESET}}$ input.

2. Internal expansion RAM capacity becomes 0 bytes by $\overline{\text{RESET}}$ input.

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM versions. In addition, when replacing the μPD78F0988 with the μPD78F0988A, be sure to also conduct sufficient evaluation with the μPD78F0988A.

2. DIFFERENCES BETWEEN μPD78F0988A AND μPD78F0988

The differences between the μPD78F0988A and μPD78F0988 (old version) are shown in Table 2-1.

Table 2-1. Differences Between μPD78F0988A and μPD78F0988

Item \ Part Number	μPD78F0988A	μPD78F0988 (Old Version)
Flash memory area	Two areas 0: 0 to 1FFFH 1: 2000H to EFFFH	Three areas 0: 0 to 1FFFH 1: 2000H to 7FFFH 2: 8000H to EFFFH
Quality grade	• Standard • Special (64-pin plastic QFP (14 × 14), 64-pin plastic LQFP (14 × 14))	• Standard

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0	Input	INTP0/TOFF7
P01		4-bit I/O port		INTP1
P02		Input/output can be specified in 1-bit units.		INTP2
P03		Use of an on-chip pull-up resistor can be specified by software setting.		INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port	Input	ANI0 to ANI7
P20	I/O	Port 2	Input	RxD00
P21		7-bit I/O port		TxD00
P22		Input/output can be specified in 1-bit units.		RxD01
P23		Use of an on-chip pull-up resistor can be specified by		TxD01
P24		software setting.		TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	AD0 to AD7
P50	I/O	Port 5	Input	—
P51		8-bit I/O port		$\overline{SCK}$
P52		Input/output can be specified in 1-bit units.		SI
P53		LEDs can be driven directly.		SO
P54		Use of an on-chip pull-up resistor can be specified by		INTP4/TI000/TO00
P55		software setting.		INTP5/TI010
P56				INTP6/TI001/TO01
P57				INTP7/TI011
P64	I/O	Port 6	Input	$\overline{RD}$
P65		4-bit I/O port		$\overline{WR}$
P66		Input/output can be specified in 1-bit units.		$\overline{WAIT}$
P67		Use of an on-chip pull-up resistor can be specified by software setting.		ASTB

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
INTP4			Input	P54/TI000/TO00
INTP5			Input	P55/TI010
INTP6			Input	P56/TI001/TO01
INTP7			Input	P57/TI011
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P24/TO50
TI51		External count clock input to 8-bit timer/event counter 51	Input	P25/TO51
TI52		External count clock input to 8-bit timer/event counter 52	Input	P26/TO52
TI000		External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture register (CR000, CR010) of 16-bit timer/event counter 00	Input	P54/INTP4/TO00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00	Input	P55/INTP5
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture register (CR001, CR011) of 16-bit timer/event counter 01	Input	P56/INTP6/TO01
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01	Input	P57/INTP7
TO50	Output	8-bit timer/event counter 50 output	Input	P24/TI50
TO51		8-bit timer/event counter 51 output	Input	P25/TI51
TO52		8-bit timer/event counter 52 output	Input	P26/TI52
TO00		16-bit timer/event counter 00 output	Input	P54/INTP4/TI000
TO01		16-bit timer/event counter 01 output	Input	P56/INTP6/TI001
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input	Input	P20
RxD01			Input	P22
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P51
SI	Input	Serial interface serial data input	Input	P52
SO	Output	Serial interface serial data output	Input	P53
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control	Hi-Z	–
TOFF7	Input	Timer output (TO70 to TO75) stop external input	Input	P00/INTP0
AD0 to AD7	I/O	Address/data bus for expanding memory externally	Input	P40 to P47
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory	Input	P65
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67
AV_{REF}	Input	A/D converter reference voltage input	–	–
AV_{DD}	–	A/D converter analog power supply	–	–

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
AV_{SS}	–	A/D converter ground potential	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2	–		–	–
V_{DD0}	–	Positive power supply for ports	–	–
V_{SS0}	–	Ground potential for ports	–	–
V_{DD1}	–	Positive power supply except for ports	–	–
V_{SS1}	–	Ground potential except for ports	–	–
V_{PP}	–	High-voltage application during program write/verify. In the normal operation mode, connect directly to V_{SS0}.	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

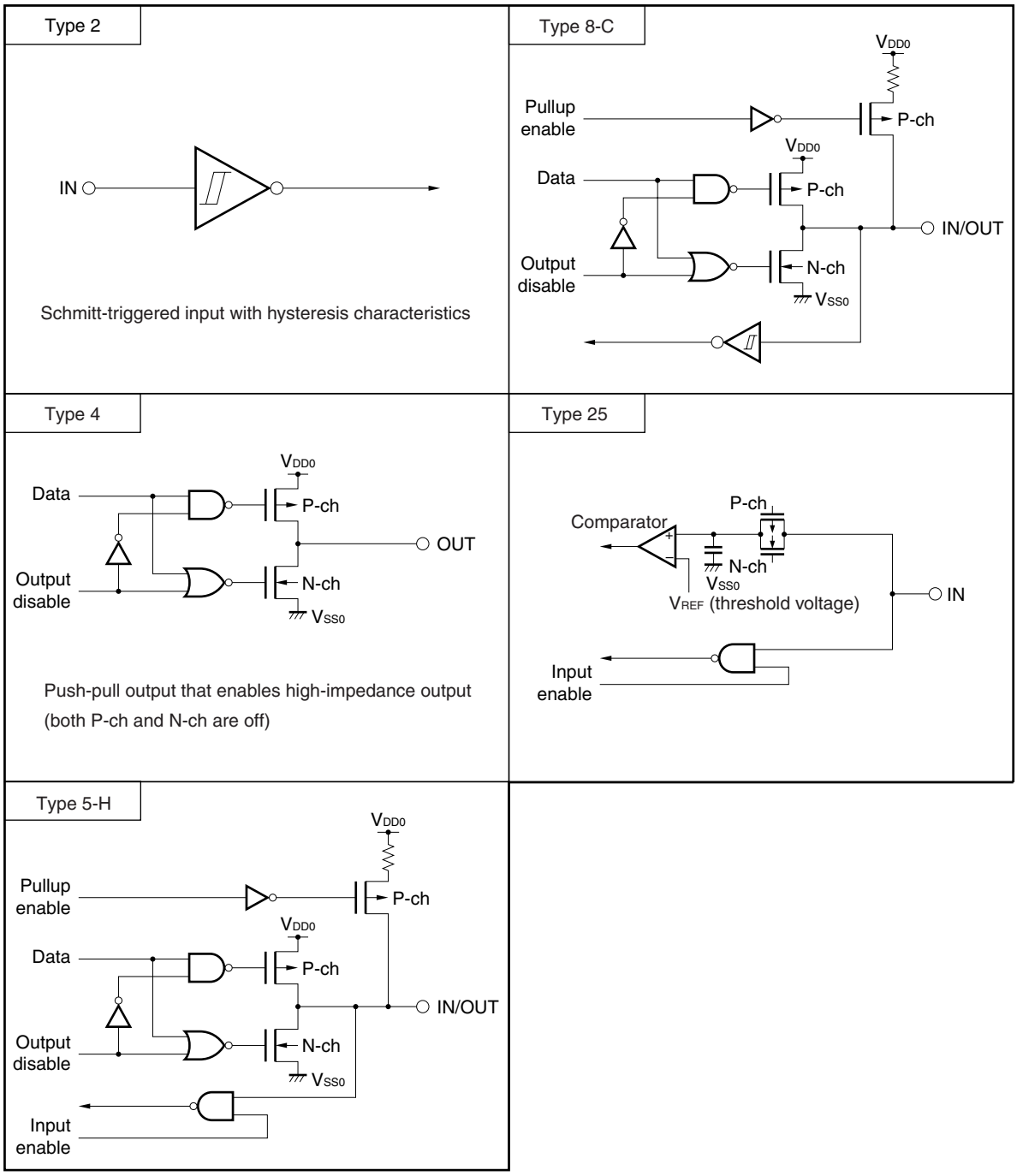
The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0/TOFF7	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open
P01/INTP1			
P02/INTP2			
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/RxD00	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/TxD00	5-H		
P22/RxD01	8-C		
P23/TxD01	5-H		
P24/TI50/TO50	8-C		
P25/TI51/TO51			
P26/TI52/TO52			
P30/RTP0 to P37/RTP7	5-H		
P40/AD0 to P47/AD7			
P50			
P51/$\overline{SCK}$	8-C		
P52/SI	5-H		
P53/SO			
P54/INTP4/TI000/TO00			
P55/INTP5/TI010			
P56/INTP6/TI001/TO01			
P57/INTP7/TI011			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
TO70 to TO75	4	Output	Leave open.
$\overline{RESET}$	2	Input	–
AV_{DD}	–	–	Connect to V_{DD0}.
AV_{REF}			Connect to V_{SS0}.
AV_{SS}			
V_{PP}			Connect directly to V_{SS0}.

Figure 3-1. Pin I/O Circuits



4. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting this register, the internal memory of the μPD78F0988A and μPD78F0988 can be mapped in the same manner as that of a mask ROM version with a different internal memory (ROM and RAM) capacity.

IMS is set with an 8-bit memory manipulation instruction.

IMS is set to CFH by $\overline{\text{RESET}}$ input.

Figure 4-1. Format of Internal Memory Size Switching Register

	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of internal ROM capacity
0	1	0	0	16 KB
0	1	1	0	24 KB
1	0	0	0	32 KB
1	1	0	0	48 KB
1	1	1	1	60 KB
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of internal high-speed RAM capacity
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 4-1 shows the IMS setting values to make the memory mapping the same as that of mask ROM versions.

Table 4-1. Setting Value of Internal Memory Size Switching Register

Target Mask ROM Versions	IMS Setting Value
μPD780982	C4H
μPD780983	C6H
μPD780984	C8H
μPD780986	CCH
μPD780988	CFH

5. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

IXS is a register that sets the internal expansion RAM capacity by software setting. By using this register, the memory of the μPD78F0988A and μPD78F0988A(A) can be mapped in the same manner as that of a mask ROM version with a different internal expansion RAM capacity.

IXS is set with an 8-bit memory manipulation instruction.

IXS is set to 0CH by $\overline{\text{RESET}}$ input.

Figure 5-1. Format of Internal Expansion RAM Size Switching Register

	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of internal expansion RAM capacity
0	1	0	1	0	1024 bytes
0	1	1	0	0	No internal expansion RAM
Other than above					Setting prohibited

Table 5-1 shows the IXS setting values to make the memory mapping the same as that of mask ROM versions.

Table 5-1. Setting Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Versions	IXS Setting Value
μPD780982	0CH
μPD780983	
μPD780984	
μPD780986	0AH
μPD780988	

6. FLASH MEMORY PROGRAMMING

On-board writing of flash memory (with device mounted on target system) is supported. On-board writing is done after connecting a dedicated flash programmer (Flashpro III (part numbers FL-PR3 and PG-FP3)) to the host machine and target system. Moreover, writing to flash memory can also be performed using a flash memory writing adapter connected to Flashpro III.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

6.1 Selection of Communication Mode

Writing to flash memory is performed using Flashpro III with a serial communication mode. Select the communication mode for writing from Table 6-1. For the selection of the communication mode, a format like the one shown in Figure 6-1 is used. The communication modes are selected using the V_{PP} pulse numbers shown in Table 6-1.

Table 6-1. Communication Mode List

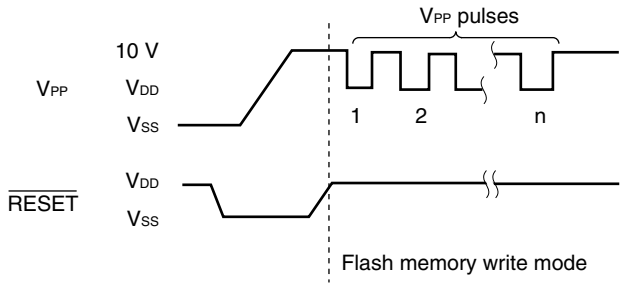
Communication Mode	Number of Channels	Pin Used[Note 1]	Number of V_{PP} Pulses
3-wire serial I/O	1	$\overline{SCK}$/P51 SI/P52 SO/P53	0
3-wire serial I/O + HS	1	P50 (HS) $\overline{SCK}$/P51 SI/P52 SO/P53	3
UART	1	RxD00/P20 TxD00/P21	8
Pseudo 3-wire serial I/O mode[Note 2]	1	P24/TI50/TO50 (Serial data input) P25/TI51/TO51 (Serial data output) P26/TI52/TO52 (Serial clock input)	12

Notes 1. Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as that immediately after reset. If the external device connected to each port does not acknowledge the state immediately after reset, pin handling such as connecting to V_{DD} or V_{SS} via a resistor is required.

2. Serial transfer is performed by controlling ports using software.

Caution Always select the communication mode according to the number of V_{PP} pulses shown in Table 6-1.

Figure 6-1. Communication Mode Selection Format



6.2 Flash Memory Programming Functions

Flash memory writing is performed via command and data transmit/receive operations using the selected communication mode. The main functions are listed in Table 6-2.

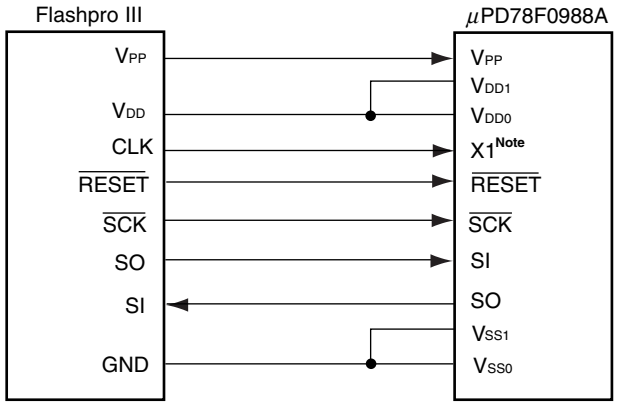
Table 6-2. Main Functions of Flash Memory Programming

Function	Description
Batch erase	Erases the contents of the entire memory.
Batch blank check	Checks that the entire memory has been erased.
Data write	Performs writing to flash memory according to the write start address and the number of the data to be written (the number of bytes).
Batch verify	Compares the contents of the entire memory and the input data.
Write back	Countermeasure for the over-erase state of the flash memory.

6.3 Connection of Flashpro III

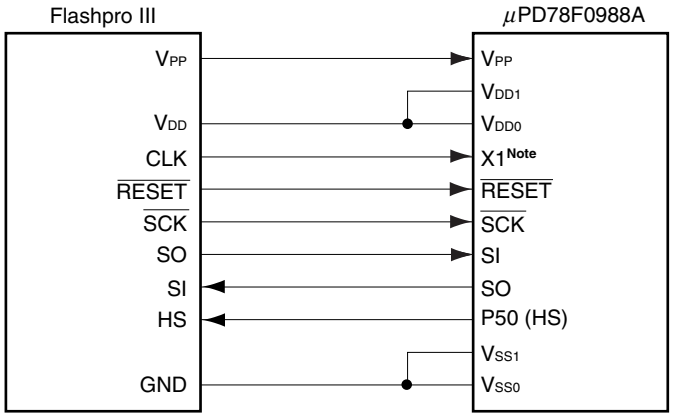
The connection of the Flashpro III and the μPD78F0988A differs depending on the communication mode. The types of connections are shown in Figures 6-2, 6-3, and 6-4.

Figure 6-2. Connection of Flashpro III Using 3-Wire Serial I/O Mode



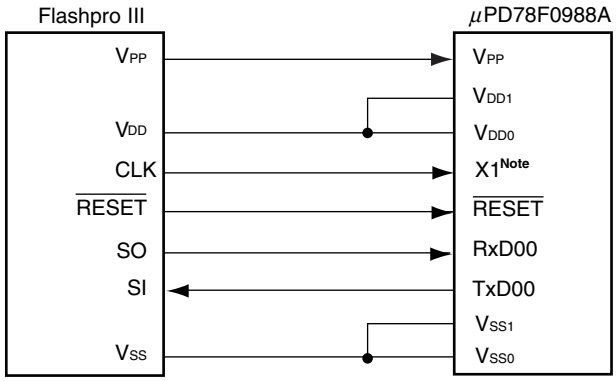
Note For input to X1, a normal oscillator can also be used instead of CLK.

Figure 6-3. Connection of Flashpro III Using 3-Wire Serial I/O Mode (When Using Handshake)



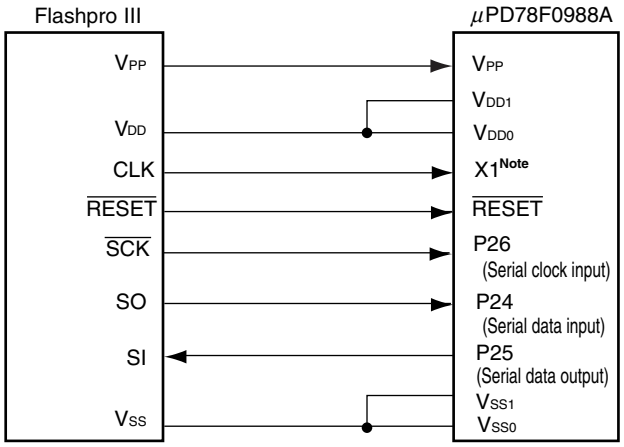
Note For input to X1, a normal oscillator can also be used instead of CLK.

Figure 6-4. Connection of Flashpro III Using UART



Note For input to X1, a normal oscillator can also be used instead of CLK.

Figure 6-5. Connection of Flashpro III Using Pseudo 3-Wire Serial I/O Mode



Note For input to X1, a normal oscillator can also be used instead of CLK.

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P50 to P57, P64 to P67, TO70 to TO75, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3 and –0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		P00, P01, P30 to P37, P40 to P47, P50 to P57, P64 to P67 total		–15	mA
		P02, P03, P20 to P26, TO70 to TO75 total		–15	mA
Output current, low	I_{OL}[Note]	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P64 to P67 per pin	Peak value	20	mA
			rms value	10	mA
		P50 to P57, TO70 to TO75 per pin	Peak value	30	mA
			rms value	15	mA
		P00, P01, P30 to P37, P40 to P47, P64 to P67 total	Peak value	100	mA
			rms value	70	mA
		P02, P03, P20 to P26 total	Peak value	30	mA
			rms value	15	mA
		TO70 to TO75 total	Peak value	100	mA
			rms value	70	mA
		P50 to P57 total	Peak value	100	mA
			rms value	70	mA
Operating ambient temperature	T_A	In normal operating mode		–40 to +85	°C
		In flash memory programming mode		+10 to +40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

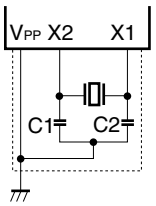
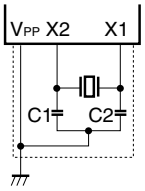
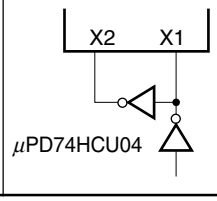
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P03, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75			15	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		8.38	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		8.38	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			10	ms
External clock		X1 input frequency (f_X)Note 1		1.0		8.38	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		50		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	4.0	5.5
	CST2.00MG040	2.00	On-chip	On-chip	4.0	5.5
	CSA3.58MG	3.58	30	30	4.0	5.5
	CST3.58MGW	3.58	On-chip	On-chip	4.0	5.5
	CSA4.00MG	4.00	30	30	4.0	5.5
	CST4.00MGW	4.00	On-chip	On-chip	4.0	5.5
	CSA4.19MG	4.19	30	30	4.0	5.5
	CST4.19MGW	4.19	On-chip	On-chip	4.0	5.5
	CSA4.91MG	4.91	30	30	4.0	5.5
	CST4.91MGW	4.91	On-chip	On-chip	4.0	5.5
	CSA5.00MG	5.00	30	30	4.0	5.5
	CST5.00MGW	5.00	On-chip	On-chip	4.0	5.5
	CSA7.37MTZ	7.37	30	30	4.0	5.5
	CST7.37MTW	7.37	On-chip	On-chip	4.0	5.5
	CSA8.00MTZ	8.00	30	30	4.0	5.5
	CST8.00MTW	8.00	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ	8.38	30	30	4.0	5.5
	CST8.38MTW	8.38	On-chip	On-chip	4.0	5.5

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P37, P40 to P47, P50, P53, P64 to P67			0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P00 to P03, P20, P22, P24 to P26, P51, P52, P54 to P57			0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2			V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P37, P40 to P47, P50, P53, P64 to P67			0		0.3V_{DD}	V
	V_{IL2}	$\overline{RESET}$, P00 to P03, P20, P22, P24 to P26, P51, P52, P54 to P57			0		0.2V_{DD}	V
	V_{IL3}	X1, X2			0		0.4	V
Output voltage, high	V_{OH1}	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA			V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P50 to P57, TO70 to TO75	5.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA			0.4	2.0	V
		P00 to P03, P20 to P26, P30 to P37, P40 to P47, P64 to P67	5.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA				0.4	V
	V_{OL2}	I_{OL} = 400 μA					0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75, $\overline{RESET}$				3	μA
	I_{LIH2}		X1, X2				20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75, $\overline{RESET}$				–3	μA
	I_{LIL2}		X1, X2				–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}					3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V					–3	μA
Software pull-up resistor	R_2	V_{IN} = 0 V P00 to P03, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	30	90	kΩ
Power supply current[Note 1]	I_{DD1}	8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 2]	When A/D converter stopped		15	30	mA
				When A/D converter operating		16	32	mA
	I_{DD2}	8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 2]	When peripheral function stopped		1.3	2.6	mA
				When peripheral function operating			7.3	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ±10%			0.1	30	μA
V_{PP} supply voltage	V_{PP1}	In normal operation mode			0		0.2V_{DD}	V

Notes 1. Refers to the total current flowing to the internal power supply (V_{DD0} and V_{DD1}). The peripheral operation current is included, but the current flowing to the pull-up resistors of ports and the AV_{REF} pin is not.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

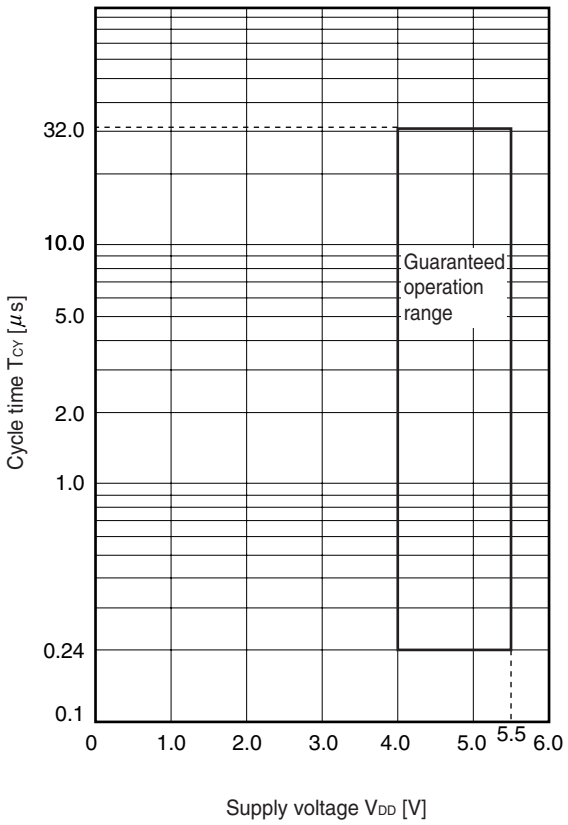
AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with system clock	0.24		32	μs
TI000, TI001, TI010, TI011 input frequency	f_{TI0}		0		f_X/64	MHz
TI000, TI001, TI010, TI011 input high-/low-level width	t_{TIH0} t_{TIL0}		$2/f_{sam}$ + 0.1 Note			μs
TI50, TI51, TI52 input frequency	f_{TI5}	8-/16-bit precision	0		4	MHz
TI50, TI51, TI52 input high-/low-level width	t_{TIH5} t_{TIL5}	8-/16-bit precision	100			ns
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0 to INTP7	1			μs
TOFF input high-/low-level width	t_{TOFFH} t_{TOFFL}		2			μs
$\overline{RESET}$ input low-level width	t_{RSL}		10			μs

Note Selection of $f_{sam} = f_X$, $f_X/4$, $f_X/32$ is possible with bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00) or with bits 0 and 1 (PRM010, PRM011) of prescaler mode register 01 (PRM01). Note that when selecting TI000 (TM00) or TI001 (TM01) valid edge as the count clock, $f_{sam} = f_X/16$.

T_{CY} vs V_{DD} (System clock operation)



(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$0.5t_{CY}$ – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL}		$(1.5 + 2n)t_{CY}$ – 15		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 15		ns
Delay time from $\overline{RD}\uparrow$ at external fetch to ASTB↑	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}		954			ns
$\overline{SCK}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(b) 3-wire serial I/O mode ($\overline{SCK}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(c) UART mode (UART00) (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					125000	bps

(d) UART mode (UART00) (Infrared data transfer mode)

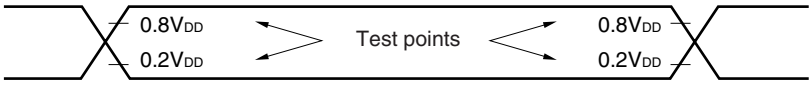
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					115200	bps
Bit rate allowable error					±0.87	%
Output pulse width			1.2		0.24/fbr[Note]	μs
Input pulse width			4/fx			μs

Note fbr: Set baud rate

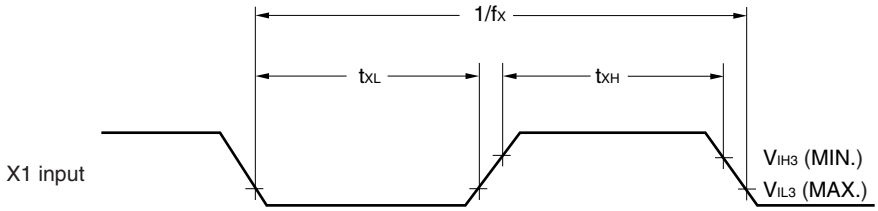
(e) UART mode (UART01) (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38400	bps

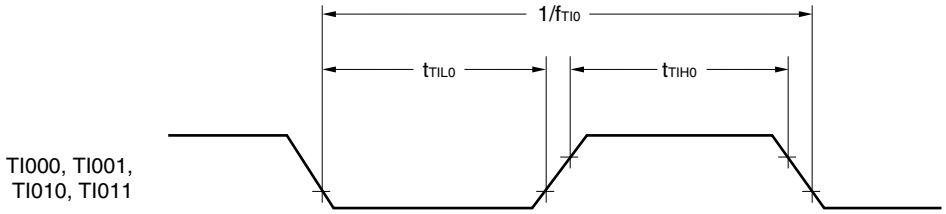
AC Timing Test Points (Excluding X1 Input)

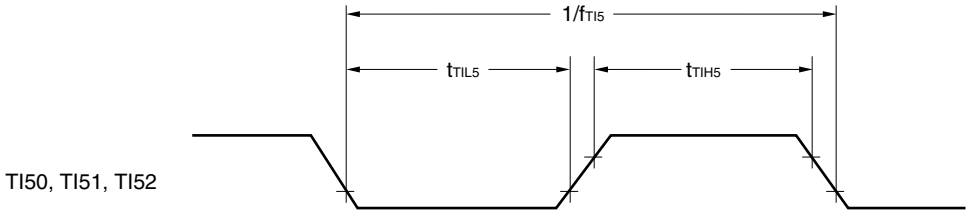


Clock Timing

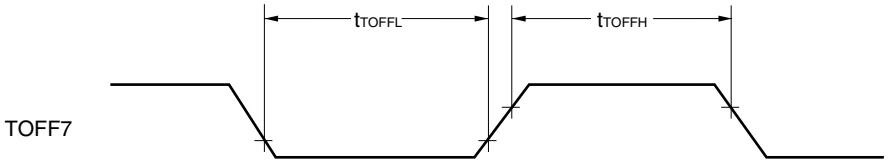


TI Timing



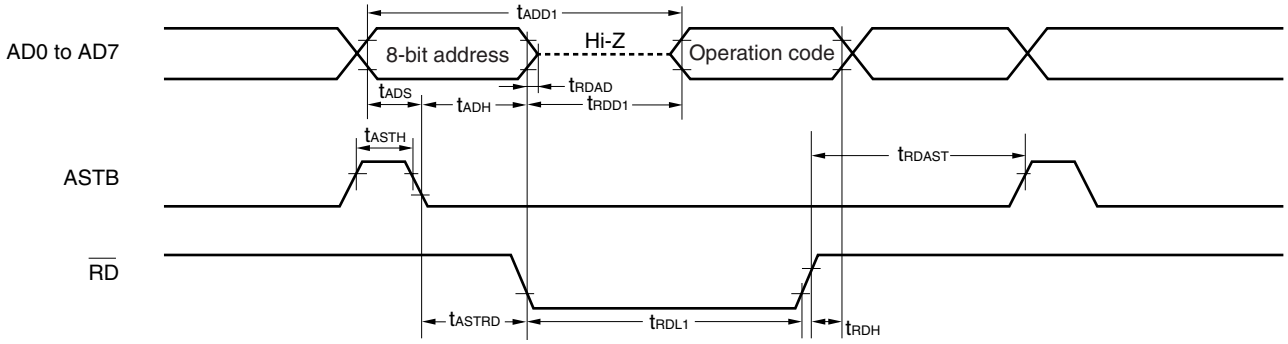


TOFF Timing

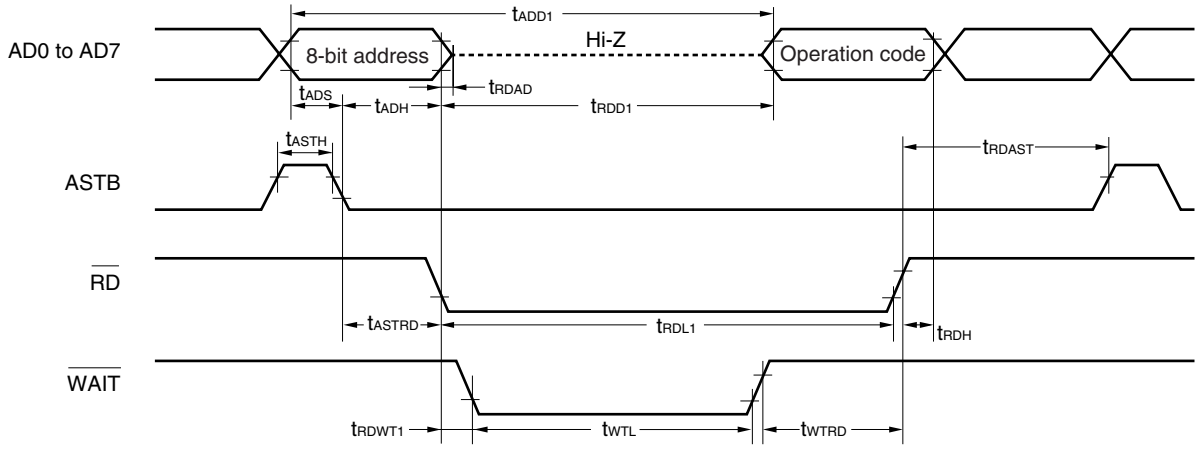


Read/Write Operation

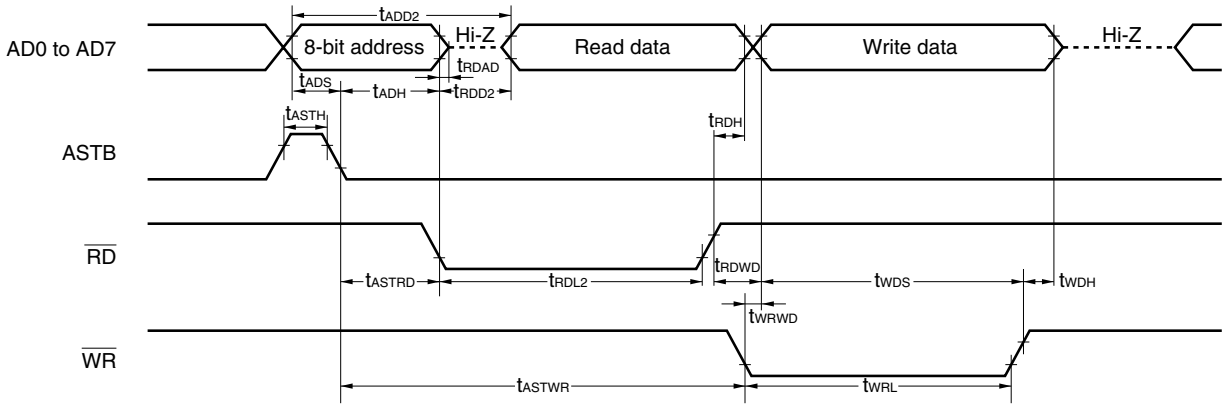
External fetch (no wait):



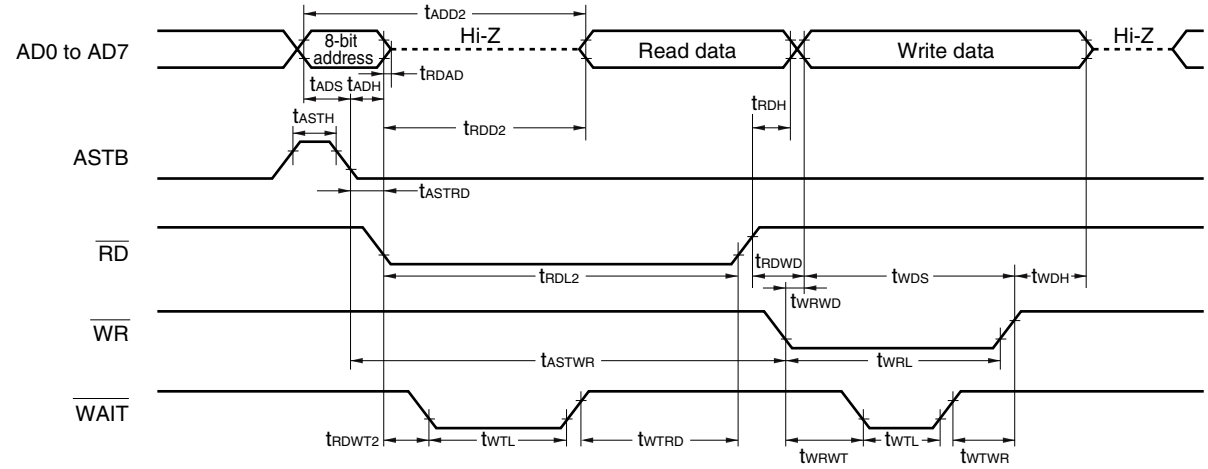
External fetch (wait insertion):



External data access (no wait):

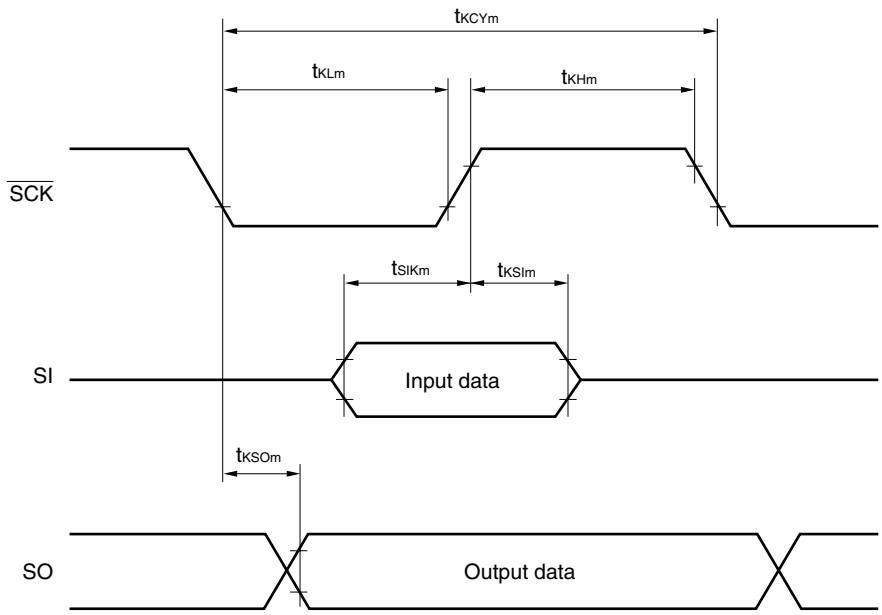


External data access (wait insertion):



Serial Transfer Timing

3-wire serial I/O mode:



m = 1, 2

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV_{REF} < 4.0 V	19		96	μs
Zero-scale error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
Full-scale error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
Non-linearity error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
Differential non-linearity error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	When A/D converter is not operating	20	40		kΩ

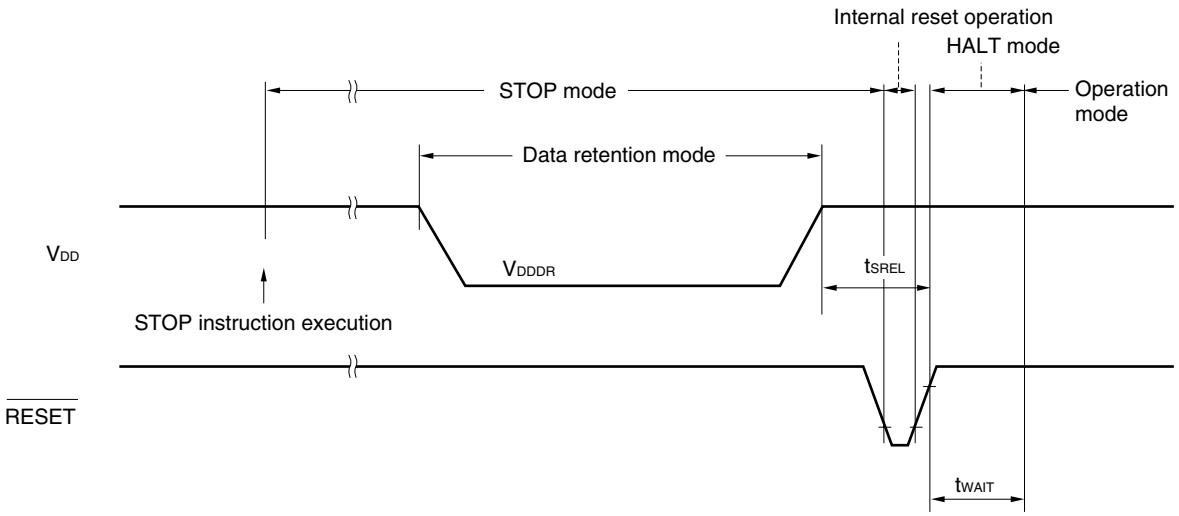
Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio (%FSR) to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

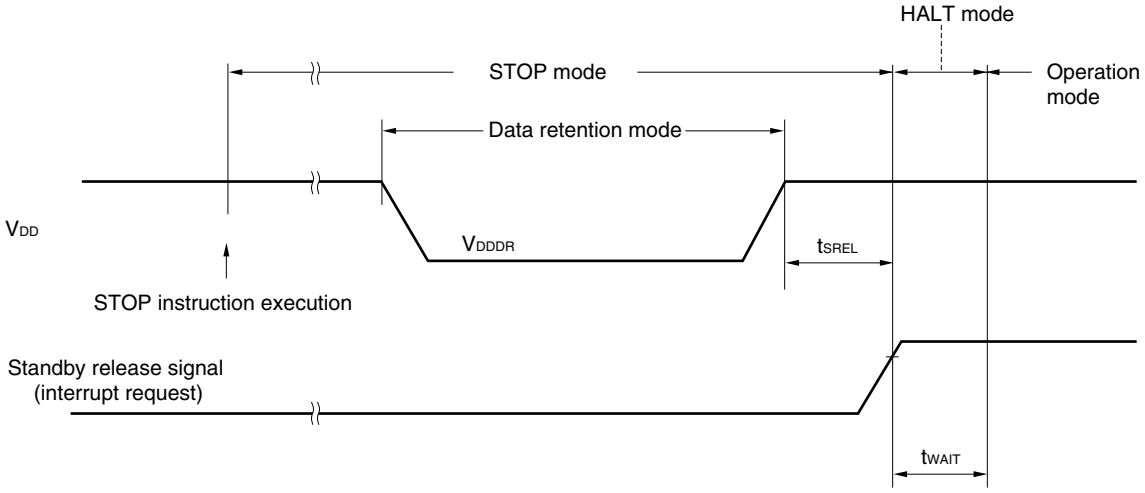
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

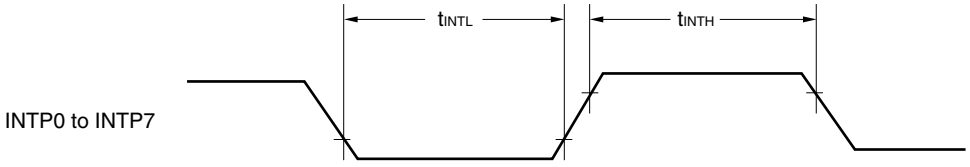
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



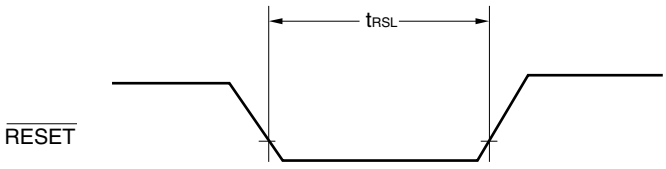
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



Flash Memory Programming Characteristics

(T_A = 10 to 40°C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	f_X		1.0		8.38	MHz
Supply voltage	V_{DD}		4.0		5.5	V
	V_{PPL}	When V_{PP} low-level is detected	0		$0.2V_{DD}$	V
	V_{PP}	When V_{PP} high-level is detected	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PPH}	When V_{PP} high-voltage is detected	9.0	10.0	10.5	V
		When programming	9.7	10.0	10.3	V
Number of rewrites	C_{WRT}		20[Note]			Times
Programming temperature	T_{PRG}		10		40	°C

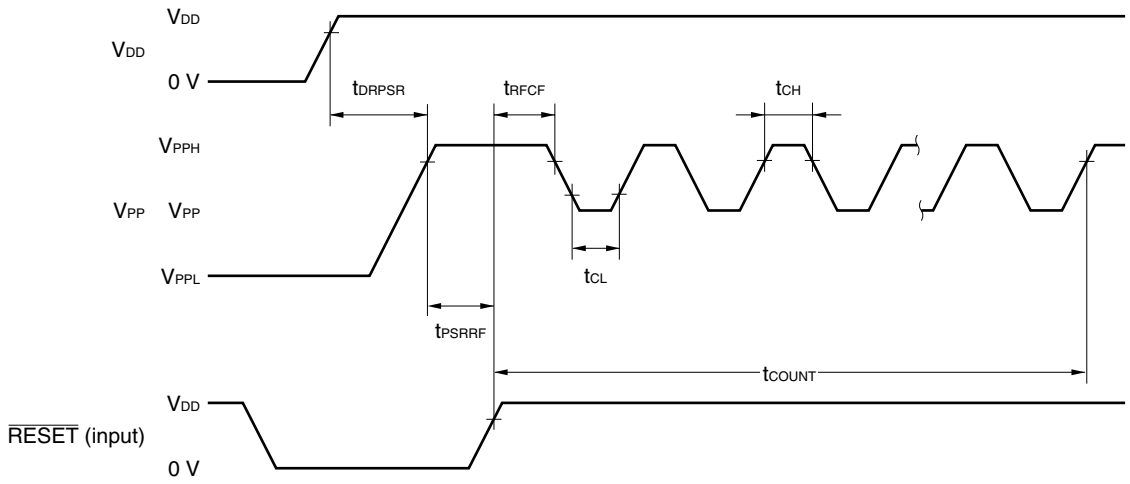
Note Operation is not guaranteed for over 20 rewrites.

Remark After execution of the program command, execute the verify command and check that the writing has been completed normally.

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Set time from V_{DD}↑ to V_{PP}↑	t_{DRPSR}	V_{PP} high voltage	0			μs
Set time from V_{PP}↑ to $\overline{RESET}$↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}	V_{PP} high voltage	1.0			μs
Count execution time	t_{COUNT}				20	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

Flash Write Mode Setting Timing



(3) Write erase characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} supply voltage	V_{PP2}	During flash memory programming	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}	When $V_{PP} = V_{PP2}$, f_{XX} = 8.38 MHz			40	mA
V_{PP} supply current	I_{PP}	When $V_{PP} = V_{PP2}$			100	mA
Step erase time	T_{er}	**Note 1**	0.199	0.2	0.201	s
Overall erase time per area	T_{era}	When step erase time = 0.2 s**Note 2**			20	s/area
Write-back time	T_{wb}	**Note 3**	49.4	50	50.6	ms
Number of write-backs per write-back command	C_{wb}	When write-back time = 50 ms**Note 4**			60	Times/ write-back command
Number of erase/ write-backs	C_{erwb}				16	Times
Step write time	T_{wr}	**Note 5**	48	50	52	μs
Overall write time per word	T_{wrw}	When step write time = 50 μs (1 word = 1 byte)**Note 6**	48		520	μs/ word
Number of rewrites per area	C_{erwr}	1 erase + 1 write after erase = 1 rewrite**Note 7**		20		Times/ area

Notes 1. The recommended setting value for the step erase time is 0.2 s.

2. The prewrite time before erasure and the erase verify time (write-back time) is not included.

3. The recommended setting value for the write-back time is 50 ms.

4. Write-back is executed once by the issuance of the write-back command. Therefore, the number of retries must be the maximum value minus the number of commands issued.

5. Recommended step write setting value is 50 μs.

6. The actual write time per word is 100 μs longer. The internal verify time during or after a write is not included.

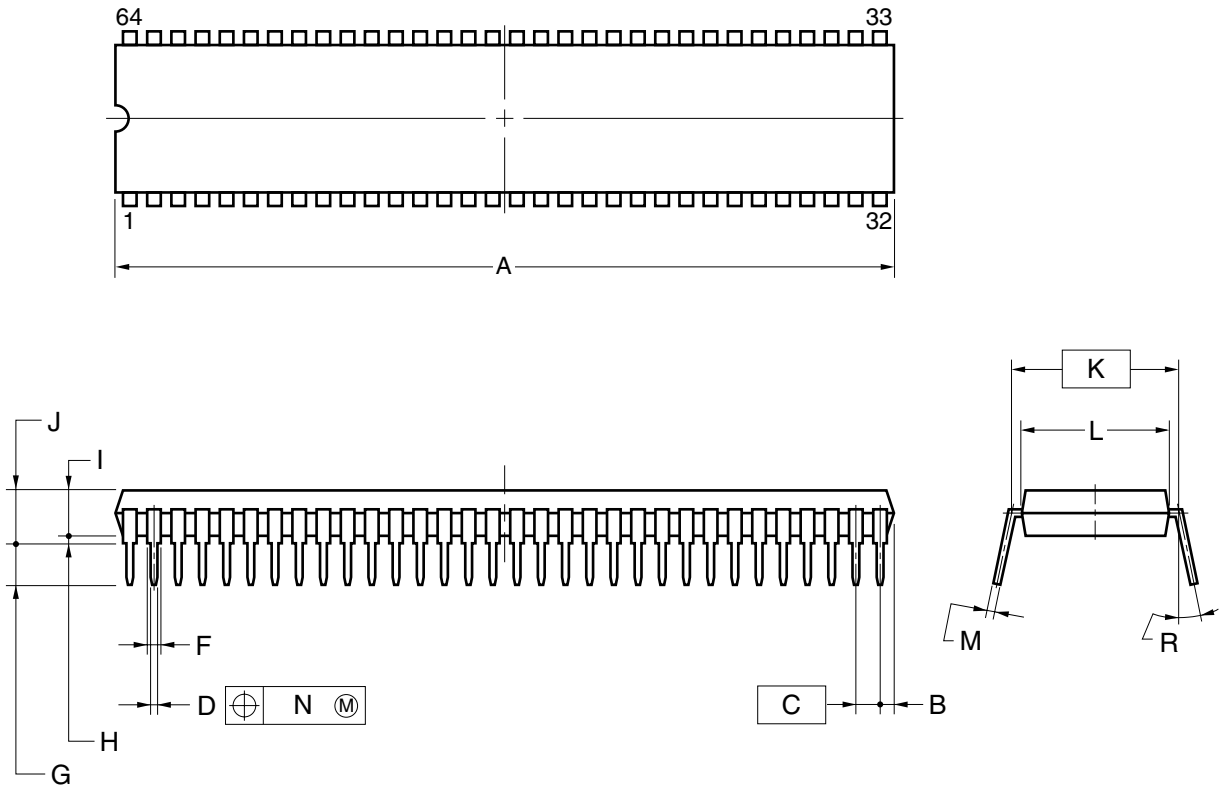
7. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.
Example: P: Write, E: Erase
Shipped product → P → E → P → E → P: 3 rewrites
Shipped product → E → P → E → P → E → P: 3 rewrites

Remarks 1. The range of the operating clock during flash memory programming is the same as the range during normal operation.

2. When using the PG-FP3, the time parameters that need to be downloaded from the parameter files for write/erase are automatically set. Unless otherwise directed, do not change the set values.

8. PACKAGE DRAWINGS

64-PIN PLASTIC SDIP (19.05mm(750))



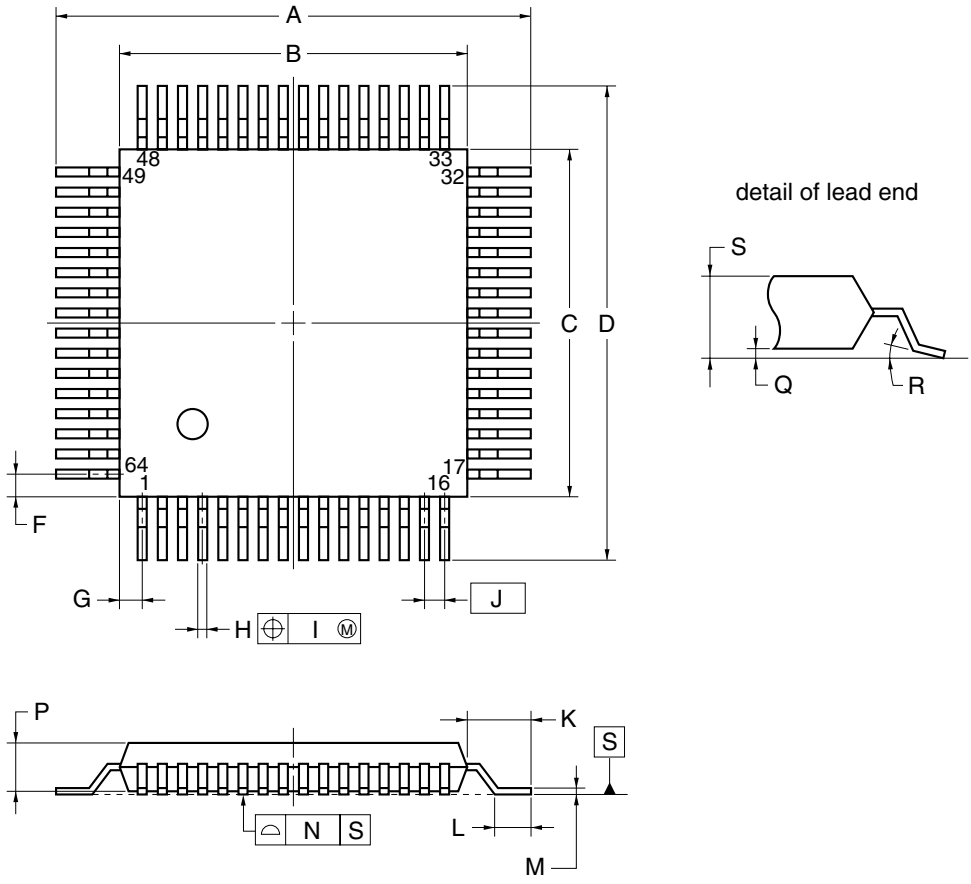
NOTES

1. Each lead centerline is located within 0.17 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	$58.0^{+0.68}_{-0.20}$
B	1.78 MAX.
C	1.778 (T.P.)
D	0.50±0.10
F	0.9 MIN.
G	3.2±0.3
H	0.51 MIN.
I	$4.05^{+0.26}_{-0.20}$
J	5.08 MAX.
K	19.05 (T.P.)
L	17.0±0.2
M	$0.25^{+0.10}_{-0.05}$
N	0.17
R	0 ~ 15°

P64C-70-750A,C-4

64-PIN PLASTIC QFP (14x14)



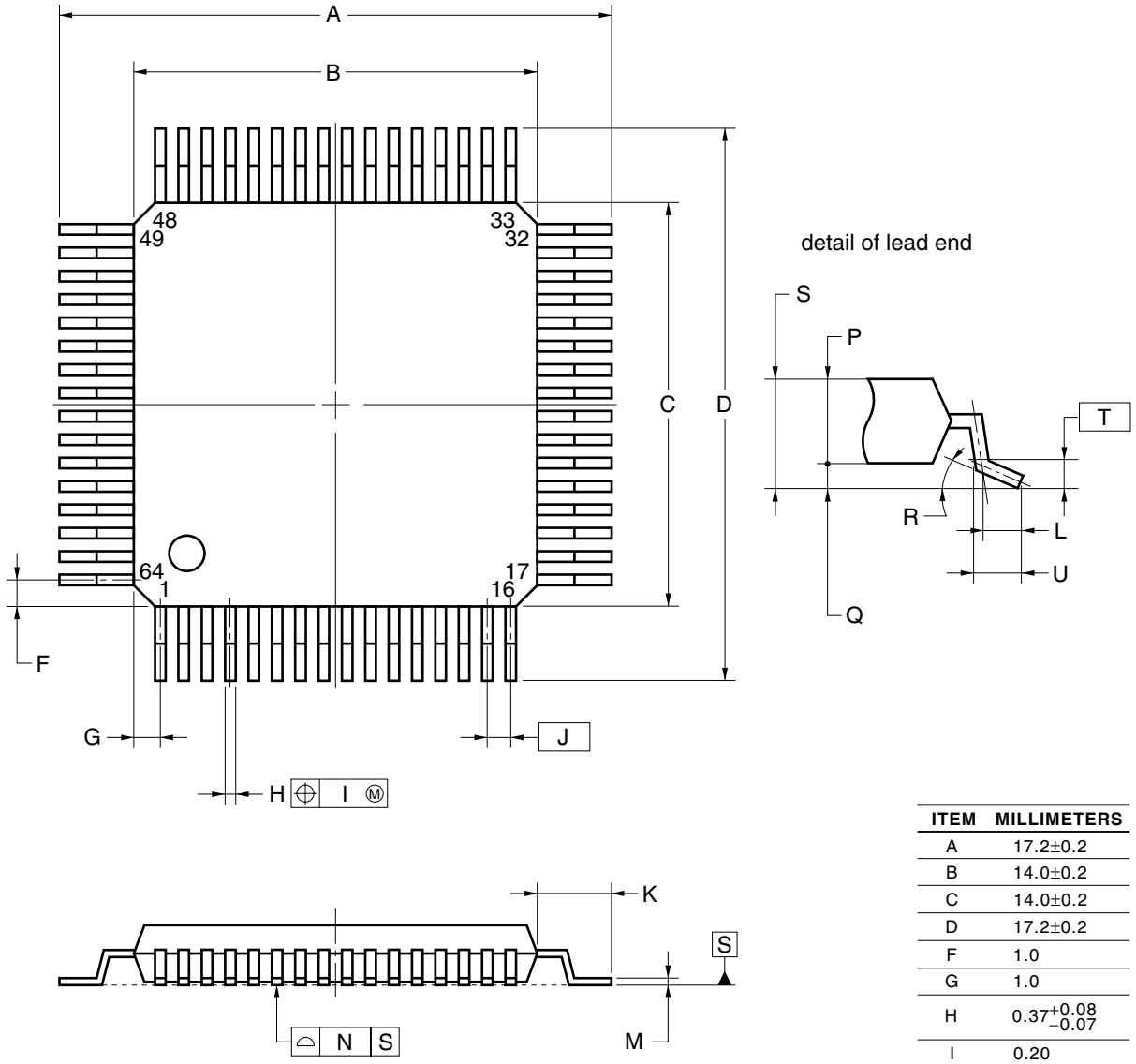
NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.6±0.4
B	14.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.55±0.1
Q	0.1±0.1
R	5°±5°
S	2.85 MAX.

P64GC-80-AB8-5

64-PIN PLASTIC LQFP (14x14)



ITEM	MILLIMETERS
A	17.2±0.2
B	14.0±0.2
C	14.0±0.2
D	17.2±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.20
J	0.8 (T.P.)
K	1.6±0.2
L	0.8
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.1
Q	0.127±0.075
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.
T	0.25
U	0.886±0.15

P64GC-80-8BS

NOTE

Each lead centerline is located within 0.20 mm of its true position (T.P.) at maximum material condition.

9. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Table 9-1. Surface Mounting Type Soldering Conditions

(1) μPD78F0988AGC-AB8: 64-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD78F0988AGC(A)-AB8: 64-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

Table 9-2. Insertion Type Soldering Conditions

μPD78F0988ACW: 64-pin plastic SDIP (19.05 mm (750))

Soldering Method	Soldering Condition
Wave soldering (only for pins)	Solder bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780988 Subseries.
Also refer to **(5) Cautions on Using Development Tools**.

(1) Software package

SP78K0	Software package common to 78K/0 Series

(2) Language processing software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(3) Flash memory writing tools

Flashpro III (part No. FL-PR3, PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64CW FA-64GC FA-64GC-8BS-A	Adapter for flash memory writing. Used connected to Flashpro III. • FA-64CW: for 64-pin plastic SDIP (CW type) • FA-64GC: for 64-pin plastic QFP (GC-AB8 type) • FA-64GC-8BS-A: for 64-pin plastic LQFP (GC-8BS type)

(4) Debugging tools

- **When IE-78K0-NS, IE-78K0-NS-A in-circuit emulator is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-78K0-NS-PA	Performance board for enhancement and expansion of IE-78K0-NS functions
IE-78K0-NS-A	Combination of IE-78K0-NS and IE-78K0-NS-PA
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter necessary when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using PCI bus incorporated personal computer as host machine
IE-780988-NS-EM4, IE-78K0-NS-P01	Emulation board and I/O board to emulate μPD780988 Subseries
NP-64CW	Emulation probe for 64-pin plastic SDIP (CW type)
NP-64GC NP-64GC-TQ NP-H64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type)
EV-9200GC-64	Conversion socket to connect the NP-64GC and a target system board on which the 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type) can be mounted
TGC-064SAP	Conversion adapter to connect the NP-64GC-TQ or NP-H64GC-TQ and a target system board on which the 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries

- **When IE-78001-R-A in-circuit emulator is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Adapter necessary when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Adapter necessary when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using PCI bus incorporated personal computer as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780988-NS-EM4, IE-78K0-NS-P01	Emulation board and I/O board to emulate μPD780988 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780988-NS-EM4 and IE-78K0-NS-P01 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic SDIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type)
EV-9200GC-64	Socket to connect target system board made for mounting 64-pin plastic QFP (GC-AB8 type) or 64-pin plastic LQFP (GC-8BS type) and EP-78240GC-R
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries

(5) Real-time OS

RX78K0	Real-time OS for 78K/0 Series

(6) Cautions on using development tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780988.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 or DF780988.
- The FL-PR3, FA-64CW, FA-64GC, NP-64CW, NP-64GC, NP-64GC-TQ, and NP-H64GC-TQ are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).
- The TGC-064SAP is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact: Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL +81-3-3820-7112)
  Osaka Electronics Department (TEL +81-6-6244-6672)
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machine and OS suitable for each software are as follows.

Host Machine [OS] / Software	PC PC-9800 series [Japanese Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	–
ID78K0	√	–
SM78K0	√	–
RX78K0	√Note	√

Note DOS-based software

(7) Cautions on designing target system

The connection condition diagrams for an emulation probe, conversion connector, and conversion socket or conversion adapter are shown below. Design the system taking into consideration the dimension or shape, etc. of the parts to be mounted on the target system.

Table A-1. Distance Between In-Circuit Emulator and Conversion Socket

Emulation Probe	Conversion Adapter, Conversion Socket	Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter
NP-64GC	EV-9200GC-64	170 mm
NP-64GC-TQ	TGC-064SAP	170 mm
NP-H64GC-TQ		370 mm
NP-64CW	–	160 mm

Figure A-1. Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter (1)

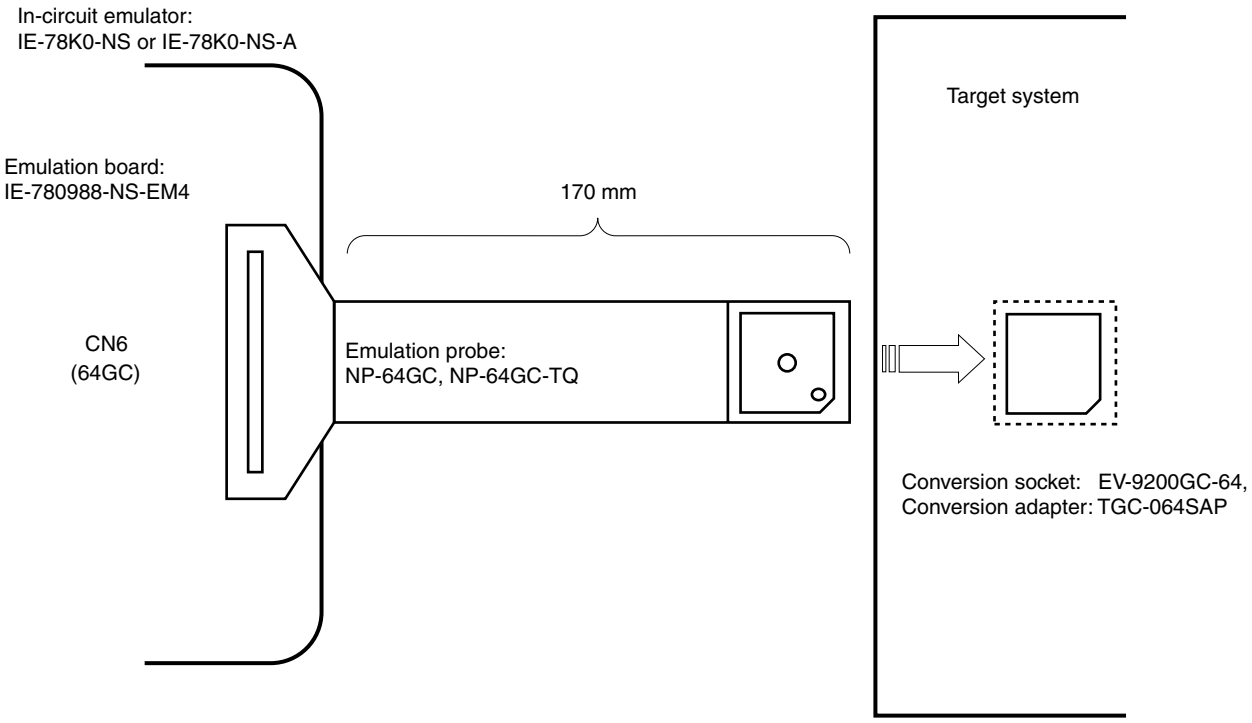


Figure A-2. Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter (2)

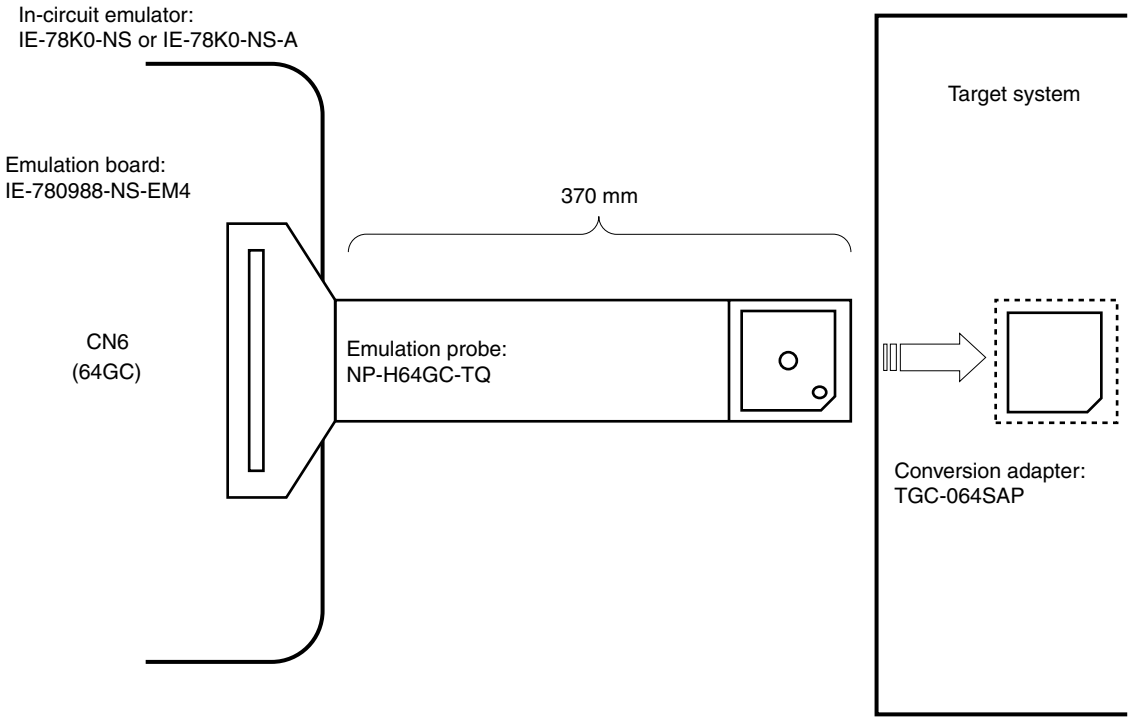


Figure A-3. Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter (3)

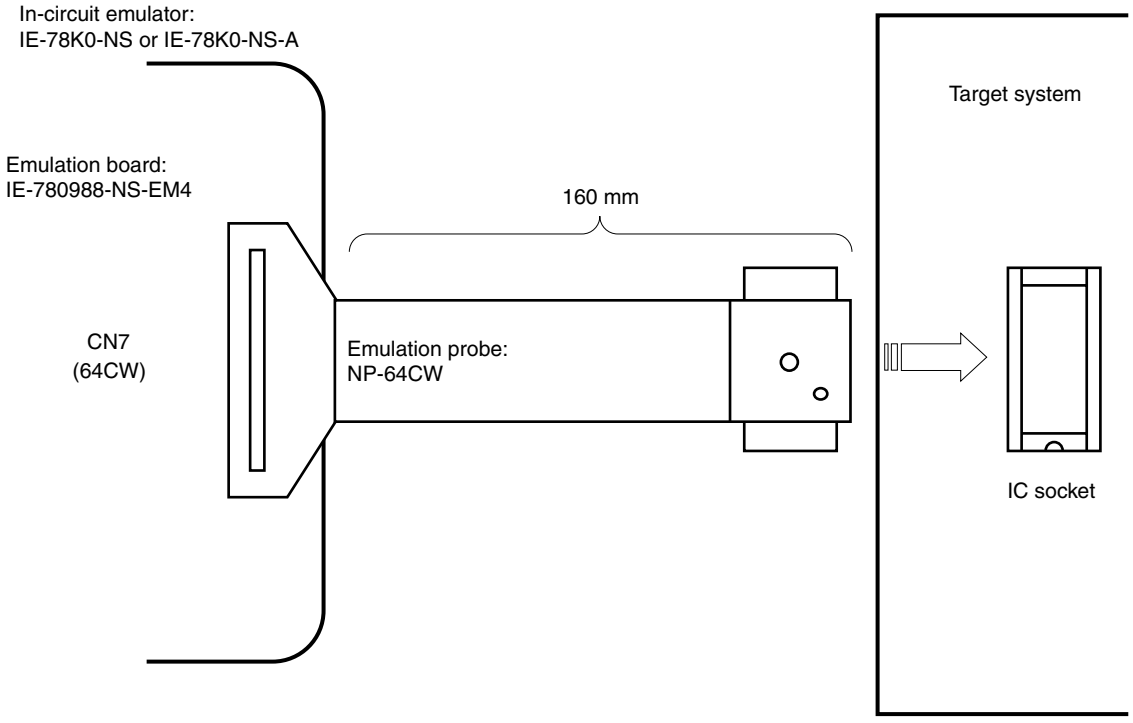


Figure A-4. Connection Condition of Target System (1)

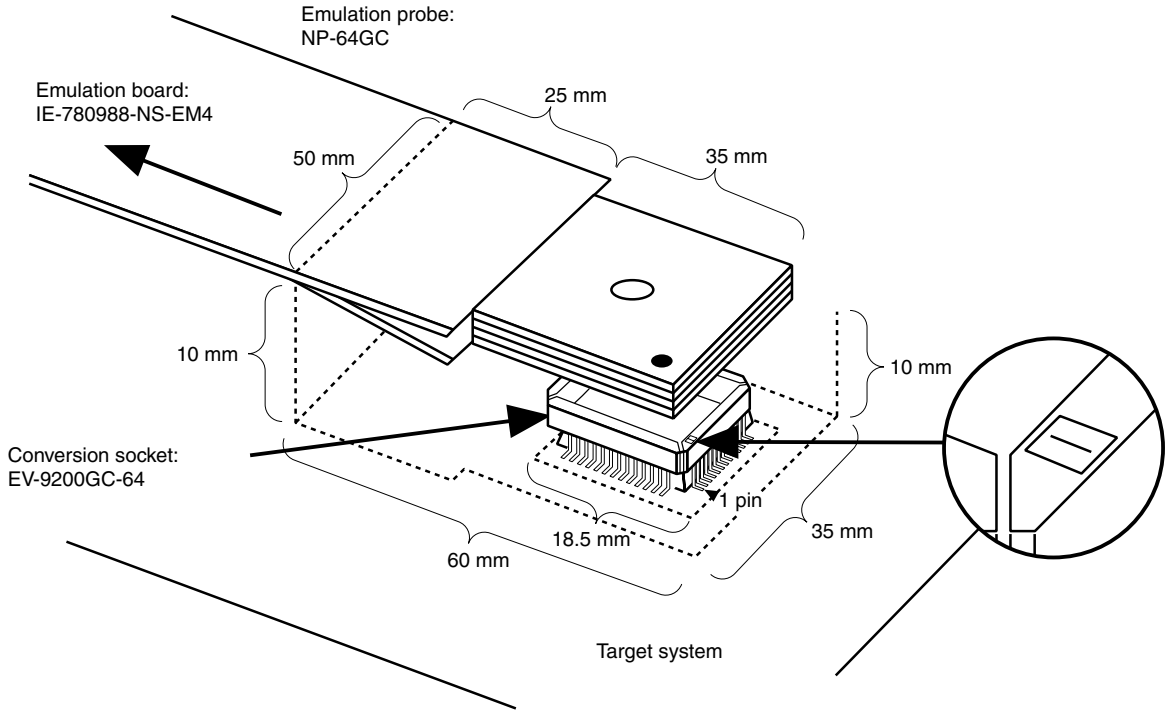


Figure A-5. Connection Condition of Target System (2)

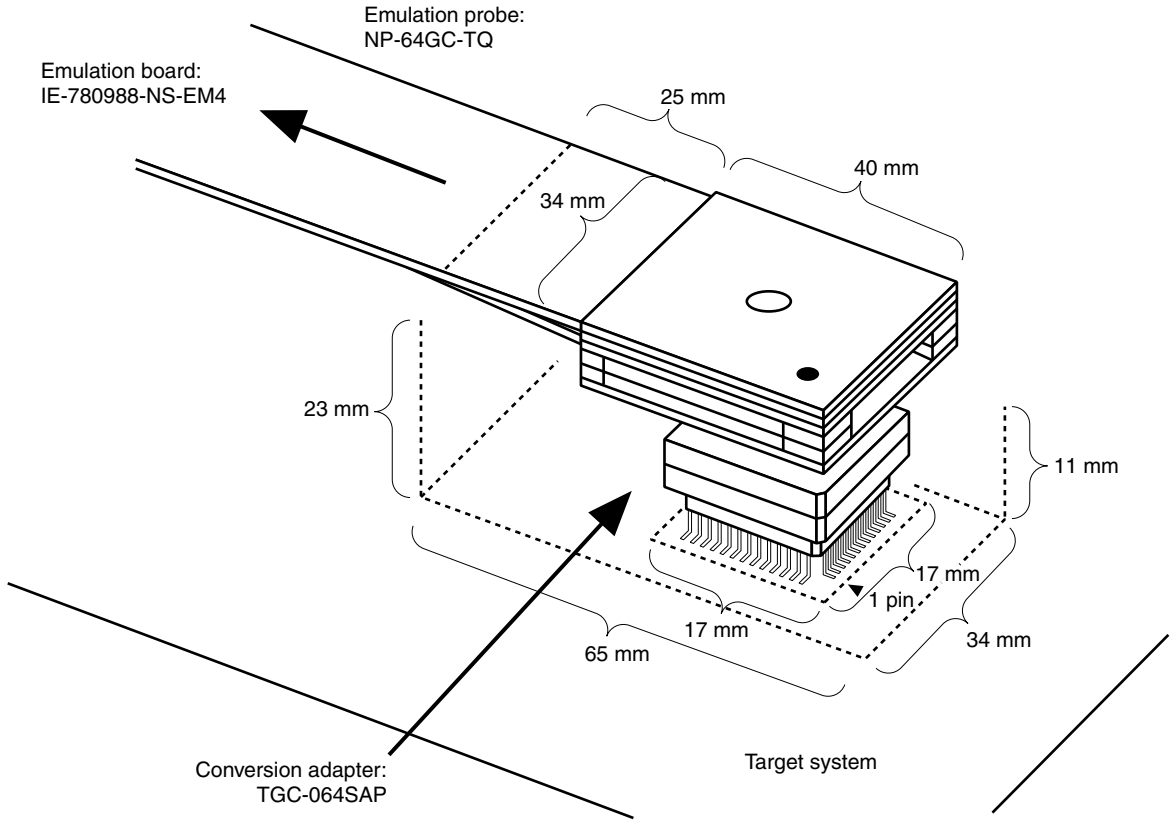


Figure A-6. Connection Condition of Target System (3)

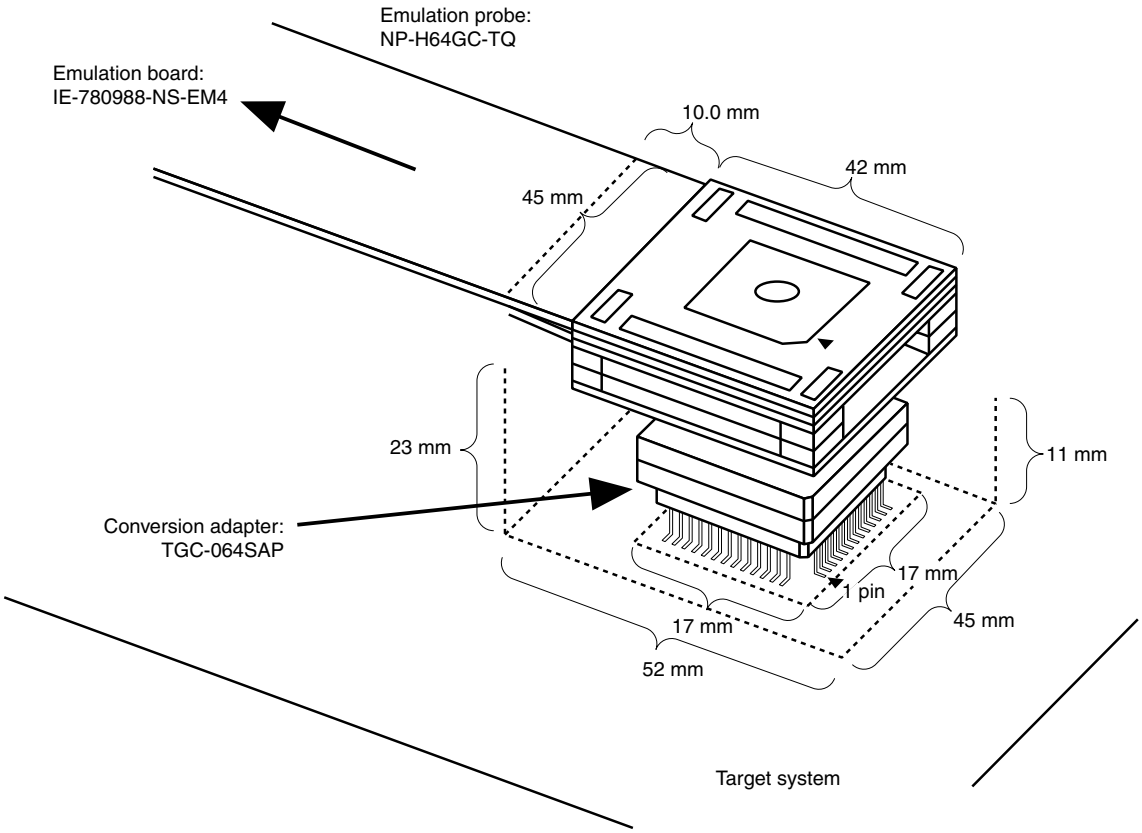
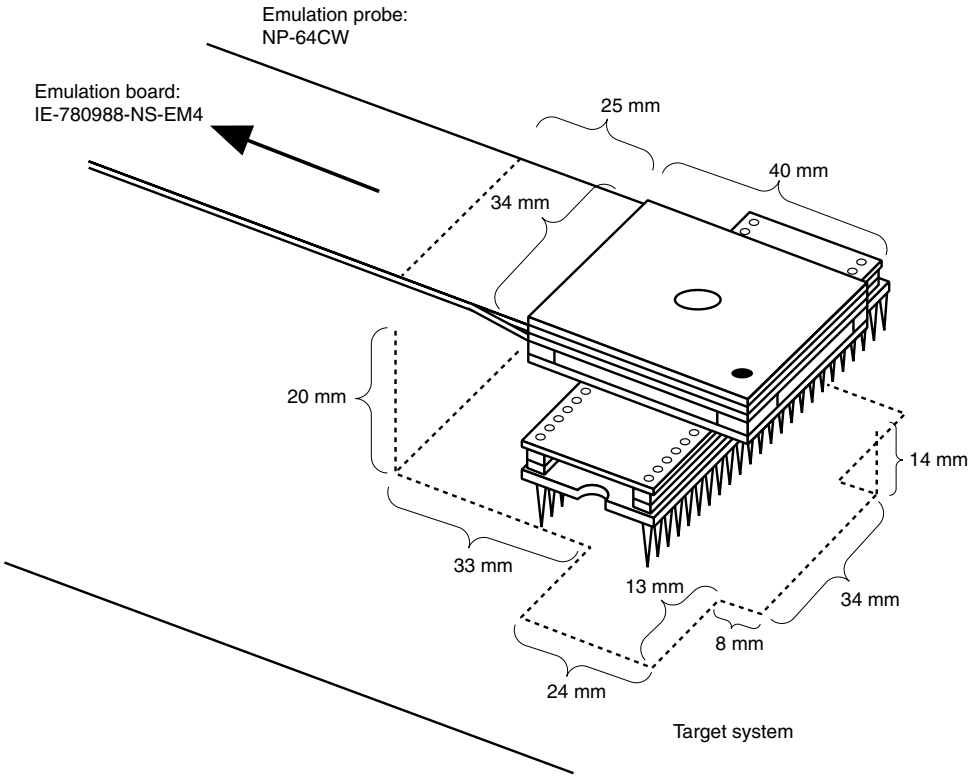


Figure A-7. Connection Condition of Target System (4)



APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- **Documents related to devices**

Document Name	Document No.
μPD780988 Subseries User's Manual	U13029E
μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), 780988(A) Data Sheet	U12804E
μPD78F0988A, 78F0988A(A) Data Sheet	This manual
μPD780988 Subseries Inverter Control Application Note	U13119E
78K/0 Series Instructions User's Manual	U12326E

- **Documents related to development software tools (user's manuals)**

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later	Operation (Windows Based)	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later	Operation (Windows Based)	U14379E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E
RX78K0 Real-Time OS	Fundamentals	U11537E
	Installation	U11536E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

- **Documents related to development hardware tools (user's manuals)**

Document Name	Document No.
IE-78K0-NS In-Circuit Emulator	U13731E
IE-78K0-NS-A In-Circuit Emulator	U14889E
IE-78001-R-A In-Circuit Emulator	U14142E
IE-78K0-R-EX1 In-Circuit Emulator	To be prepared

- **Documents related to flash memory writing**

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E

- **Other related documents**

Document Name	Document No.
SEMICONDUCTORS SELECTION GUIDE - Products & Packages -	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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