Single 8-Ch/Differential 4-Ch CMOS Analog Multiplexers

(Obsolete for non-hermetic. Use DG408/409 as pin-for-pin replacements.)

FEATURES

- Low On-Resistance: 240 Ω
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

BENEFITS

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

APPLICATIONS

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

DESCRIPTION

The DG508A_MIL, an 8-channel single-ended analog multiplexer, is designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2).

The DG509A_MIL, a dual 4-channel analog multiplexer, is designed to connect one of four differential inputs to a common output as determined by its 2-bit binary address (A_0, A_1) logic. Break-before-make switching action protects against momentary shorting of the input signals.

A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

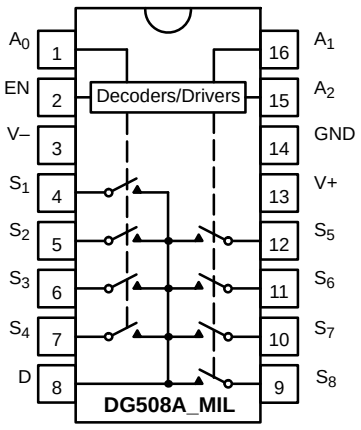
Fabricated in the Vishay Siliconix Plus-40 process, the absolute maximum voltage rating is extended to 44 V, allowing increased operating headroom for standard ±15-V signal swings and operation with ±20-V supplies. An epitaxial layer prevents latch up.

The DG508A_MIL/509A_MIL are available in hermetic packages. For plastic packages, use the DG408/409 as pin-for-pin replacements.

For applications requiring address data latching, the DG528/529 is recommended. DG408/409 is recommended for higher precision applications. For wideband/video routing and multiplexing, the DG538A is recommended.

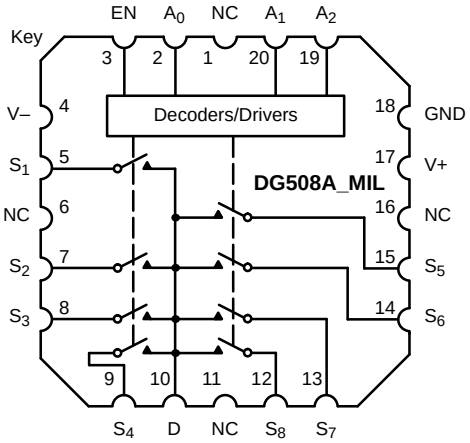
FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

Dual-In-Line



Top View

LCC



Top View

FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

ORDERING INFORMATION - DG508A_MIL

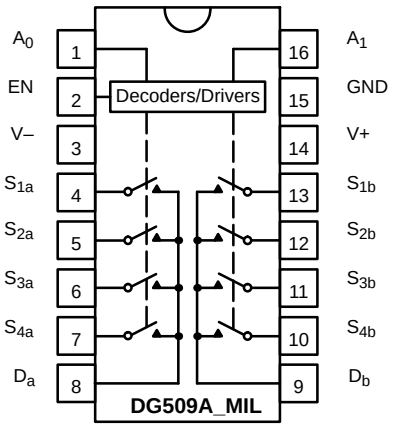
Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG508ACJ
–25 to 85°C	16-Pin CerDIP	DG508ABK
–40 to 85°C	16-Pin Narrow SOIC	DG508ADY
–55 to 125°C	16-Pin CerDIP	DG508AAK
		DG508AAK/883
	LCC-20	DG508AAZ/883
	16-Pin Sidebraze	7705201EA
		7705201EC
	16-Pin Flat Pack	7705201FA
		7705201FC
	16-Pin Sidebraze	JM38510/19007BEA
		JM38510/19007BEC

TRUTH TABLE - DG508A_MIL

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

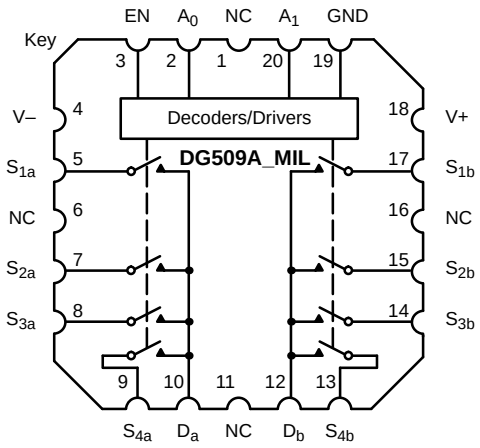
Logic “0” = $V_{AL} \leq 0.8$ V
Logic “1” = $V_{AH} \geq 2.4$ V
X = Don’t Care

Dual-In-Line and SOIC



Top View

LCC



Top View

ORDERING INFORMATION - DG509A_MIL

Temp Range	Package	Part Number
–55 to 125°C	16-Pin CerDIP	DG509AAK
		DG509AAK/883
	LCC-20	DG509AAZ/883
	16-Pin Sidebraze	JM38510/19008BEA
		JM38510/19008BEC

TRUTH TABLE - DG509A_MIL

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic “0” = $V_{AL} \leq 0.8$ V
Logic “1” = $V_{AH} \geq 2.4$ V
X = Don’t Care

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V–
V+ . . . . . 44 V
GND . . . . . 25 V
Digital Inputs[a], V_S, V_D . . . . . (V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) . . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 40 mA

Storage Temperature (K Suffix) . . . . . –65 to 150°C
(J and Y Suffix) . . . . . –65 to 125°C

Power Dissipation (Package)[b]
16-Pin CerDIP[c] . . . . . 900 mW
LCC-20[c] . . . . . 900 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 12 mW/°C above 75°C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	A Suffix –55 to 125°C Min[d]	Typ[c]	Max[d]	Unit
Analog Switch								
Analog Signal Range[e]	V_{ANALOG}			Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = –200 µA		Room Full		240	400 500	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$	–10 V < V_S < 10 V		Room		6		%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_S = ±10 V V_D = ∓10 V		Room Full	–1 –50		1 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ±10 V V_S = ∓10 V	DG508A_MIL	Room Full	–10 –200		10 200	
			DG509A_MIL	Room Full	–10 –100		10 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V	DG508A_MIL	Room Full	–10 –200		10 200	
			DG509A_MIL	Room Full	–10 –100		10 100	
Digital Control								
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Room Full	–10 –30	–0.002		µA
		V_A = 15 V		Room Full		0.006	10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Full	–10 –30	–0.002		
Dynamic Characteristics								
Transition Time	t_{TRANS}	See Figure 2		Room		0.6	1.0	µs
Break-Before-Make Time	t_{OPEN}	See Figure 4		Room		0.2		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room		1	1.5	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room		0.4	1.0	
Charge Injection	Q	See Figure 5		Room		6		pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room		68		dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room		8		pF
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 140 kHz		Room		6		
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 140 kHz	DG508A_MIL	Room		25		
			DG509A_MIL	Room		12		

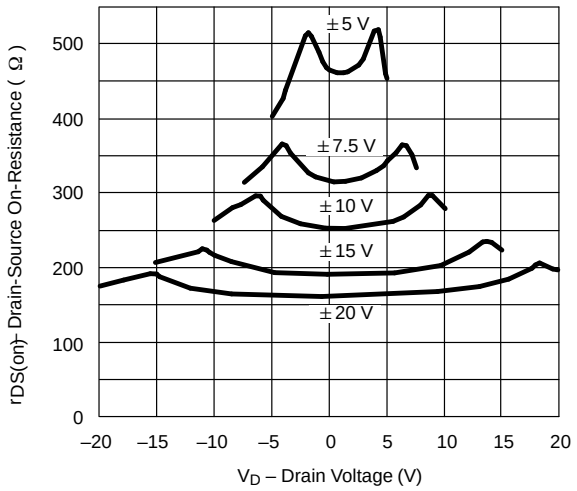
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	A Suffix –55 to 125°C Min[d]	Typ[c]	Max[d]	Unit
Power Supplies							
Positive Supply Current	I+	V_{EN} = 0 V or 2.4 V	Room		1.3	2.4	mA
Negative Supply Current	I–		Room	–1.5	–0.7		

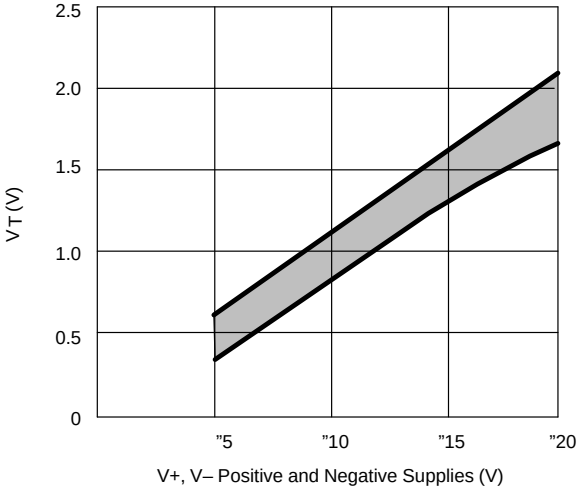
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

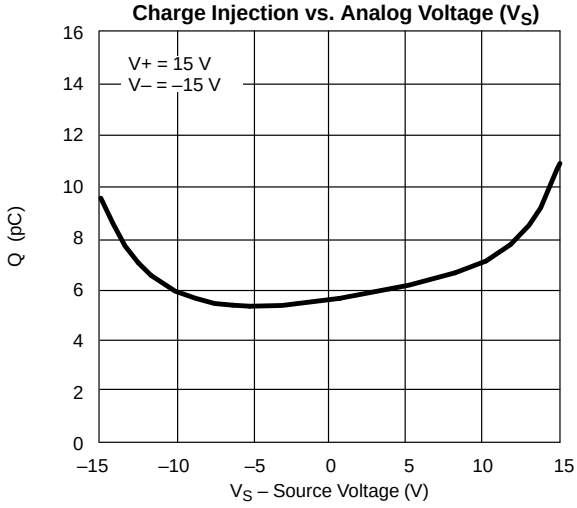
$r_{DS(on)}$ vs. V_D and Power Supply



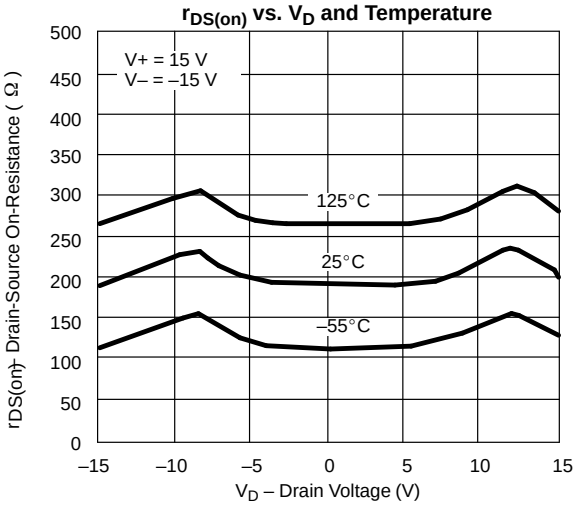
Input Switching Threshold vs. V+ and V– Supply Voltages



Charge Injection vs. Analog Voltage (V_S)

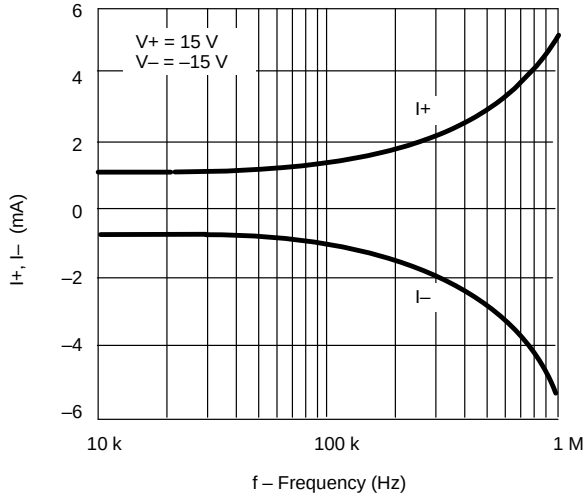


$r_{DS(on)}$ vs. V_D and Temperature

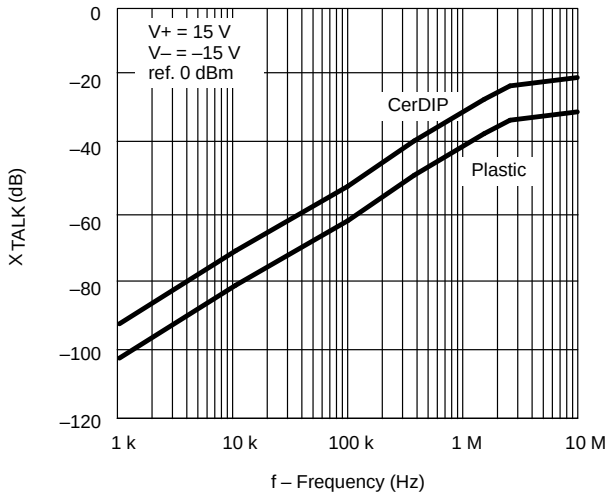


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

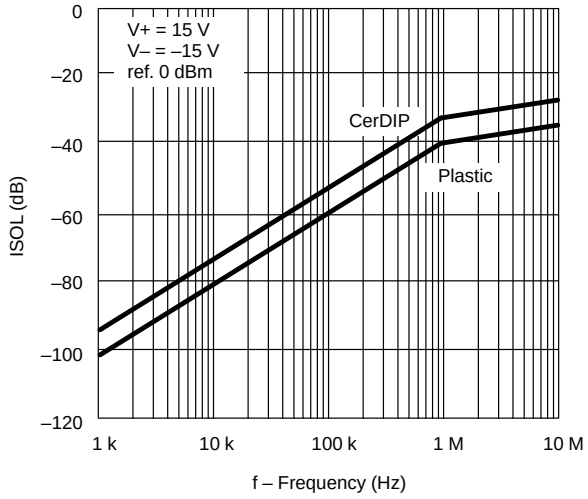
Supply Current vs. Switching Frequency



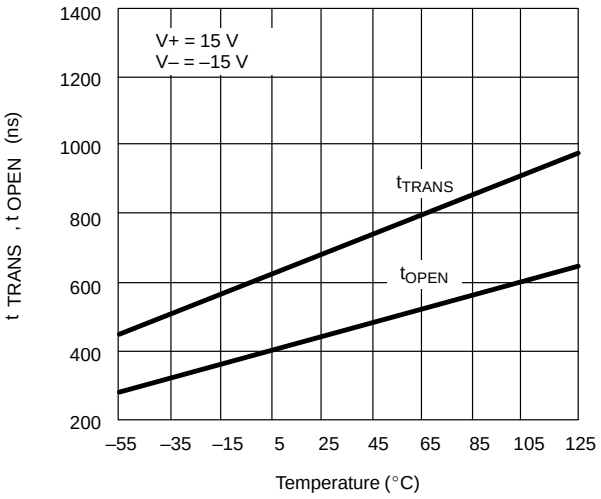
Crosstalk vs. Frequency



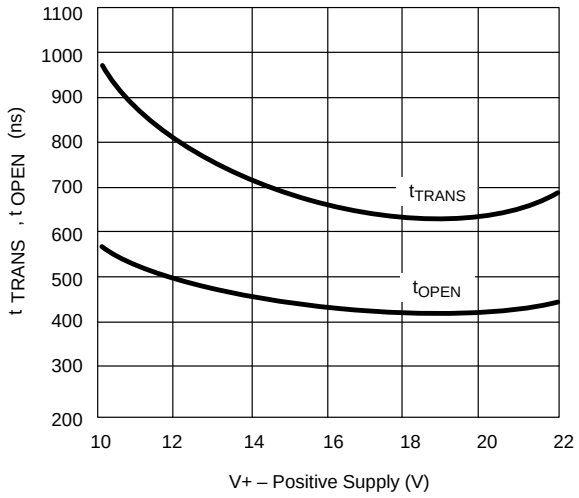
Off Isolation vs. Frequency



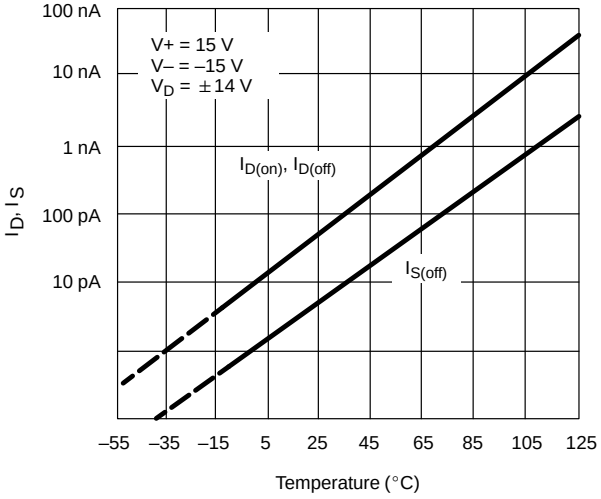
Switching Time vs. Temperature



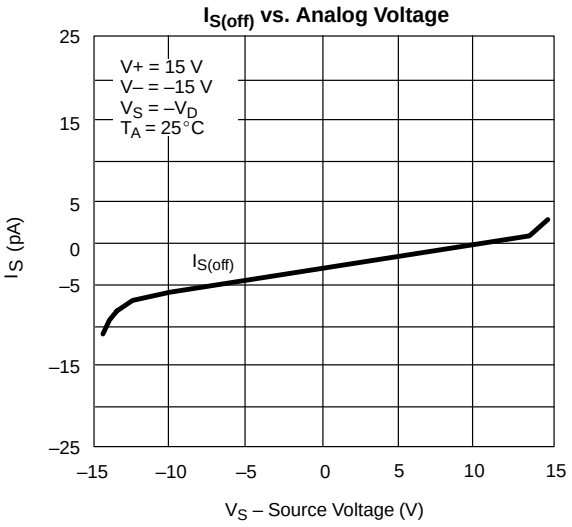
Switching Time vs. Positive Supply Voltage

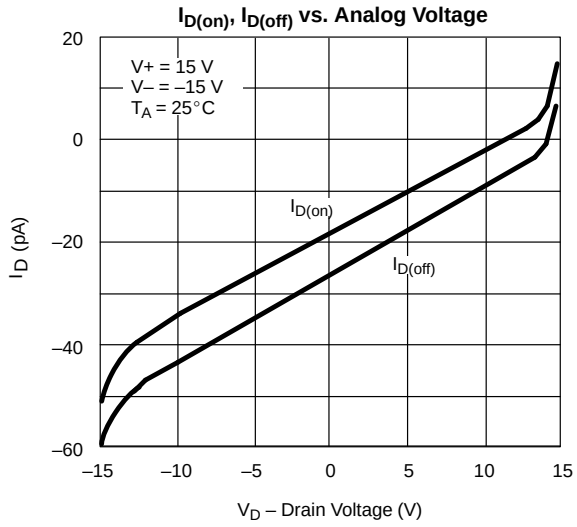


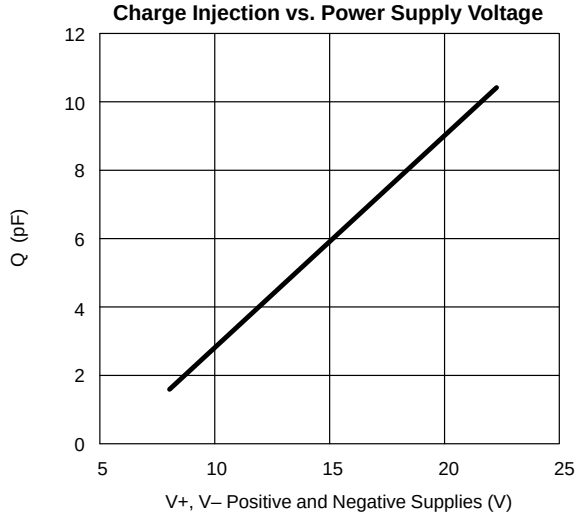
Leakages vs. Temperature



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)







SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

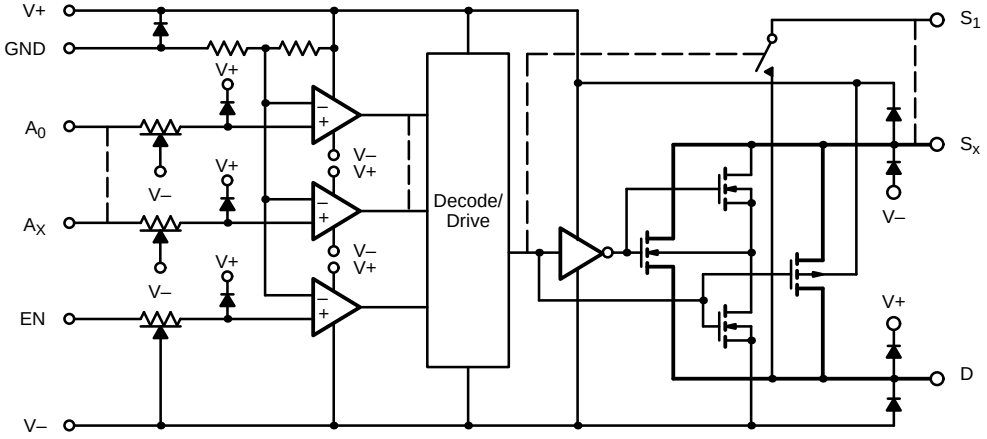


FIGURE 1.

TEST CIRCUITS

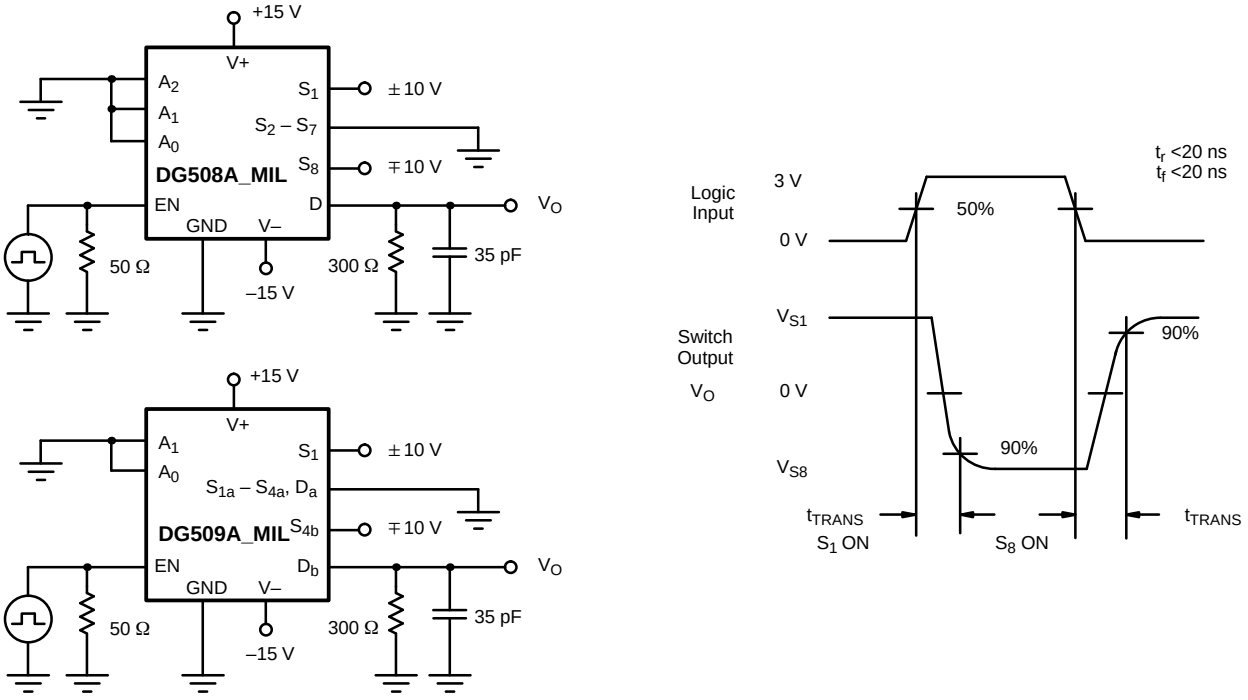


FIGURE 2. Transition Time

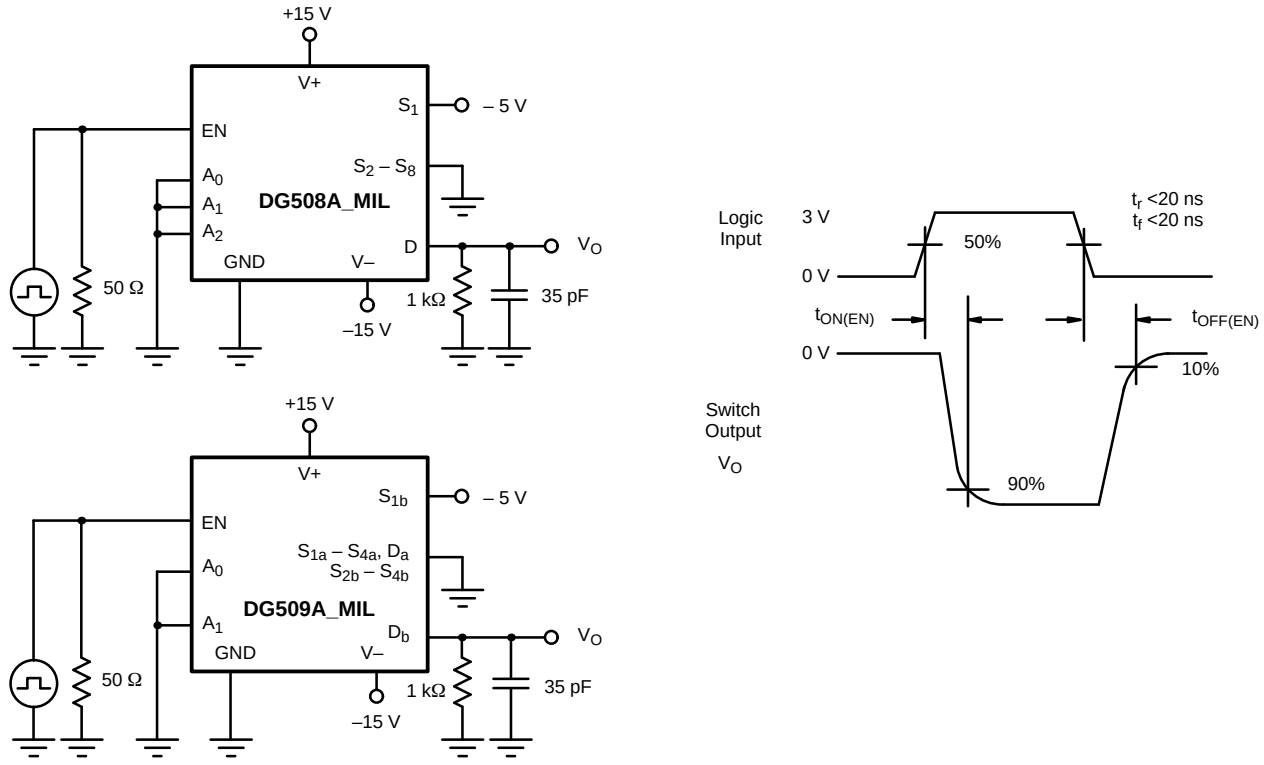


FIGURE 3. Enable Switching Time

TEST CIRCUITS

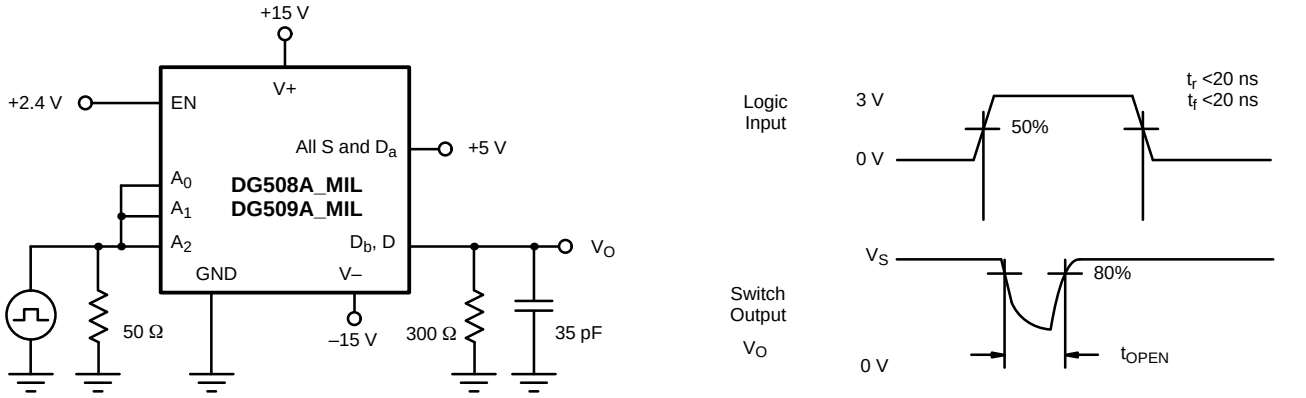


FIGURE 4. Break-Before-Make Interval

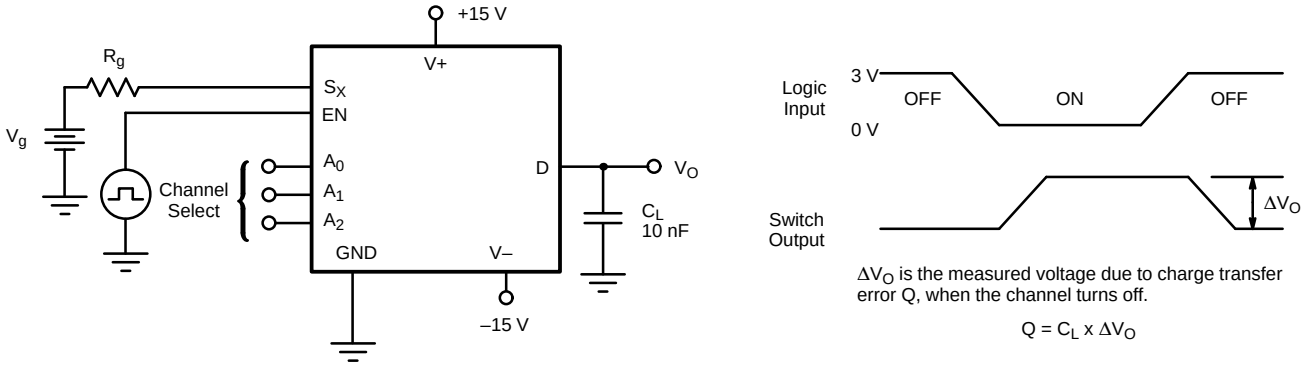


FIGURE 5. Charge Injection

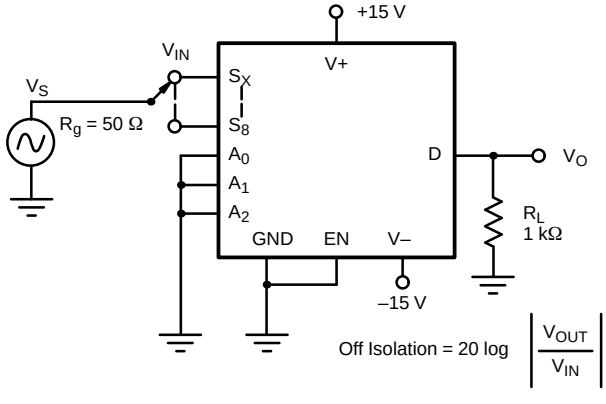


FIGURE 6. Off Isolation

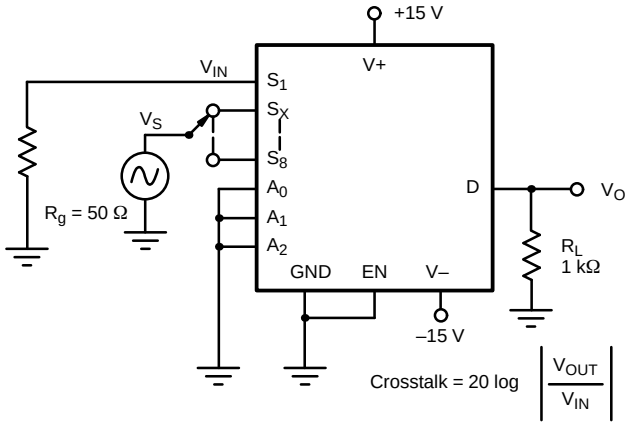


FIGURE 7. Crosstalk

TEST CIRCUITS

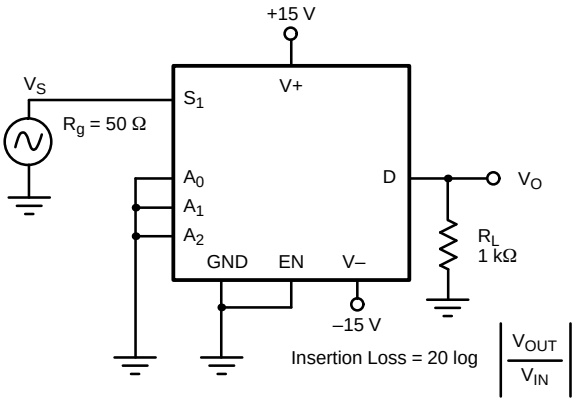


FIGURE 8. Insertion Loss

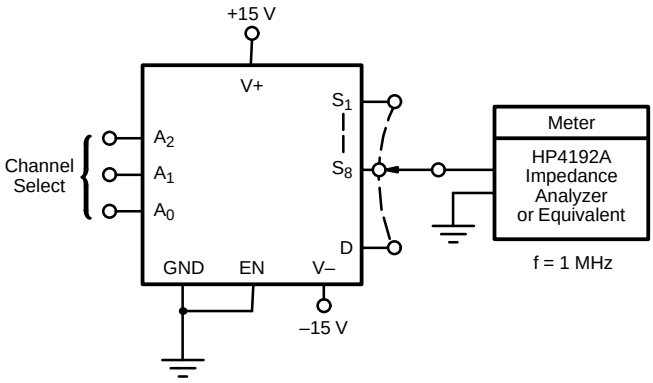


FIGURE 9. Source Drain Capacitance

APPLICATIONS[a]			
V+ Positive Supply Voltage (V)	**V– Negative Supply Voltage (V)**	**V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)**	**V_S or V_D Analog Voltage Range (V)**
15	–15	2.4/0.8	–15 to 15
10	–12	2.4/0.8	–12 to 12
12	–10	2.4/0.6	–10 to 10
8[b]	–8	2.4/0.4	–8 to 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 11). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V– value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V– rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V–, but it preserves the low channel resistance and low leakage characteristics.

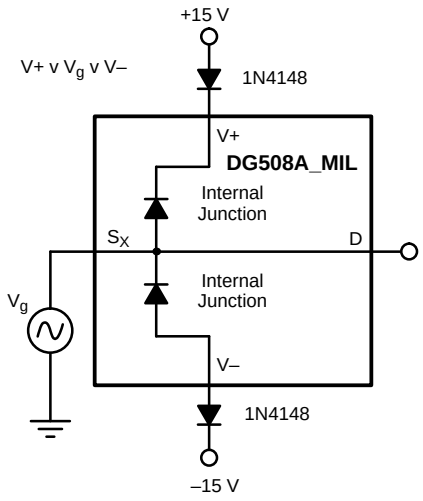


FIGURE 10. Overvoltage Protection Using Blocking Diodes

APPLICATIONS

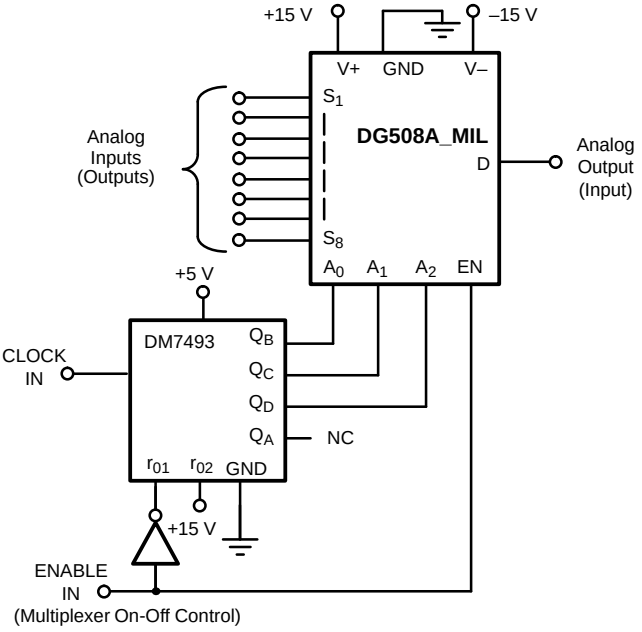


FIGURE 11. 8-Channel Sequential Multiplexer/ Demultiplexer

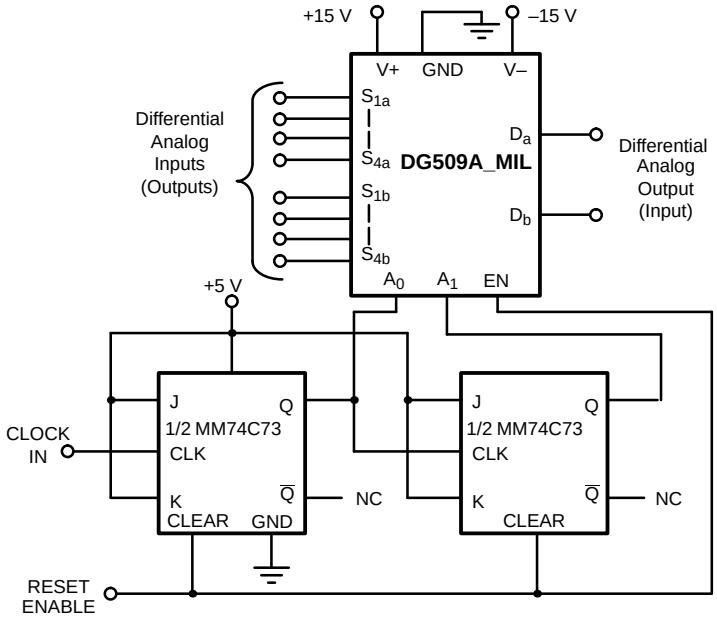


FIGURE 12. Differential 4-Channel Sequential Multiplexer/ Demultiplexer

Notice

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