FAIRCHILD SEMICONDUCTOR®

March 1993
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74VHC393
Dual 4-Bit Binary Counter

General Description

The VHC393 is an advanced high speed CMOS 4-bit Binary Counter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. It contains two independent counter circuits in one package, so that counting or frequency division of 8 binary bits can be achieved with one IC. This device changes state on the negative going transition of the CLOCK pulse. The counter can be reset to "0" (Q_0–Q_3 = "L") by a HIGH at the CLEAR input regardless of other inputs.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: f_{MAX} = 170 MHz (typ) at T_A = 25°C
- Low power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC393

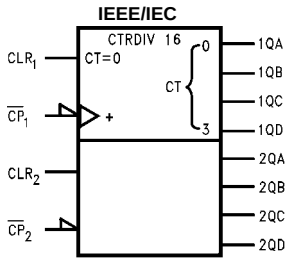
Ordering Code:

Order Number	Package Number	Package Description
74VHC393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC393SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC393MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC393MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC393N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

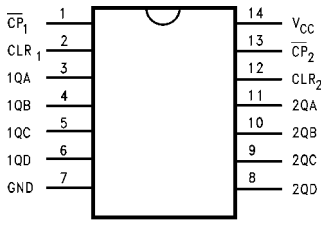
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Pin Descriptions

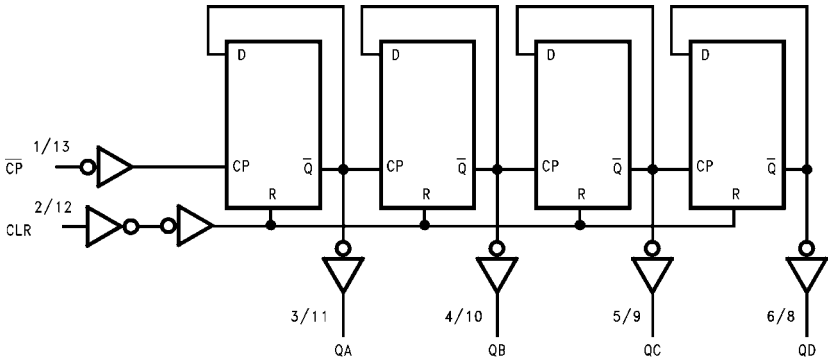
Pin Names	Description
CLR1, CLR2	Clear Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs
QA, QB, QC, QD	Outputs

Truth Table

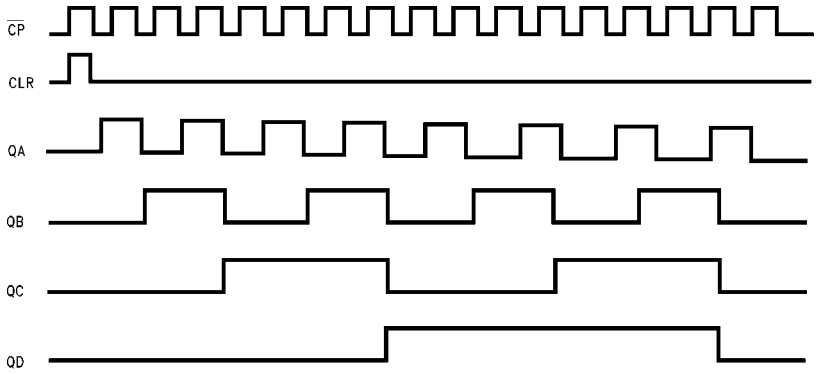
Inputs		Outputs			
$\overline{CP}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	Count Up			
↑	L	No Change			

X: Don't Care

System Diagram



Timing Chart



Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 2: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level	2.0	1.50			1.50		V		
	Input Voltage	3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level	2.0			0.50		0.50	V		
	Input Voltage	3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
	Output Voltage	3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
	Output Voltage	3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

AC Electrical Characteristics

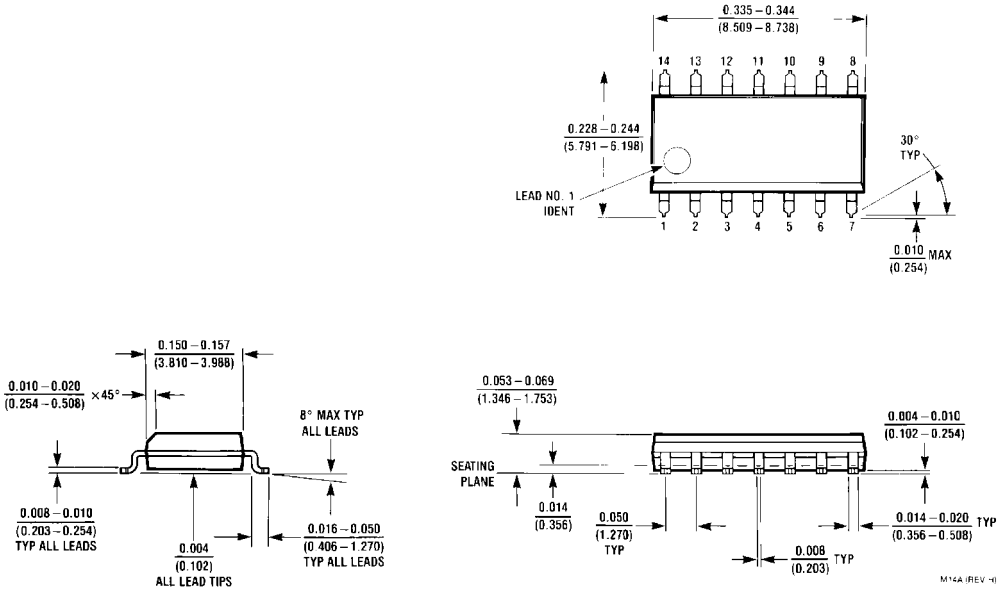
Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation	3.3 ± 0.3		8.6	13.2	1.0	15.5	ns		C_L = 15 pF
t_{PHL}	Delay Time			11.1	16.7	1.0	19.0			C_L = 50 pF
	($\overline{CP}$ -QA)	5.0 ± 0.5		5.8	8.5	1.0	10.0	ns		C_L = 15 pF
				7.3	10.5	1.0	12.0			C_L = 50 pF
t_{PLH}	Propagation	3.3 ± 0.3		10.2	15.8	1.0	18.5	ns		C_L = 15 pF
t_{PHL}	Delay Time			12.7	19.3	1.0	22.0			C_L = 50 pF
	($\overline{CP}$ -QB)	5.0 ± 0.5		6.8	9.8	1.0	11.5	ns		C_L = 15 pF
				8.3	11.8	1.0	13.5			C_L = 50 pF
t_{PLH}	Propagation	3.3 ± 0.3		11.7	18.0	1.0	21.0	ns		C_L = 15 pF
t_{PHL}	Delay Time			14.2	21.5	1.0	24.5			C_L = 50 pF
	($\overline{CP}$ -QC)	5.0 ± 0.5		7.7	11.2	1.0	13.0	ns		C_L = 15 pF
				9.2	13.2	1.0	15.0			C_L = 50 pF
t_{PLH}	Propagation	3.3 ± 0.3		13.0	19.7	1.0	23.0	ns		C_L = 15 pF
t_{PHL}	Delay Time			15.5	23.2	1.0	26.5			C_L = 50 pF
	($\overline{CP}$ -QD)	5.0 ± 0.5		8.5	12.5	1.0	14.5	ns		C_L = 15 pF
				10.0	14.5	1.0	16.5			C_L = 50 pF
t_{PLH}	Propagation	3.3 ± 0.3		7.9	12.3	1.0	14.5	ns		C_L = 15 pF
t_{PHL}	Delay Time			10.4	15.8	1.0	18.0			C_L = 50 pF
	(CLR-Q_n)	5.0 ± 0.5		5.4	8.1	1.0	9.5	ns		C_L = 15 pF
				6.9	10.1	1.0	11.5			C_L = 50 pF
f_{MAX}	Maximum	3.3 ± 0.3	75	120		65		MHz		C_L = 15 pF
	Clock		45	65		35				C_L = 50 pF
		5.0 ± 0.5	125	170		105				C_L = 15 pF
			85	115		75				C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{PD}	Power Dissipation Capacitance			23				pF	(Note 4)	

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load Average operating current can be obtained by the equation: $I_{CC}(opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC/2}$ (per Counter)

AC Operating Requirements

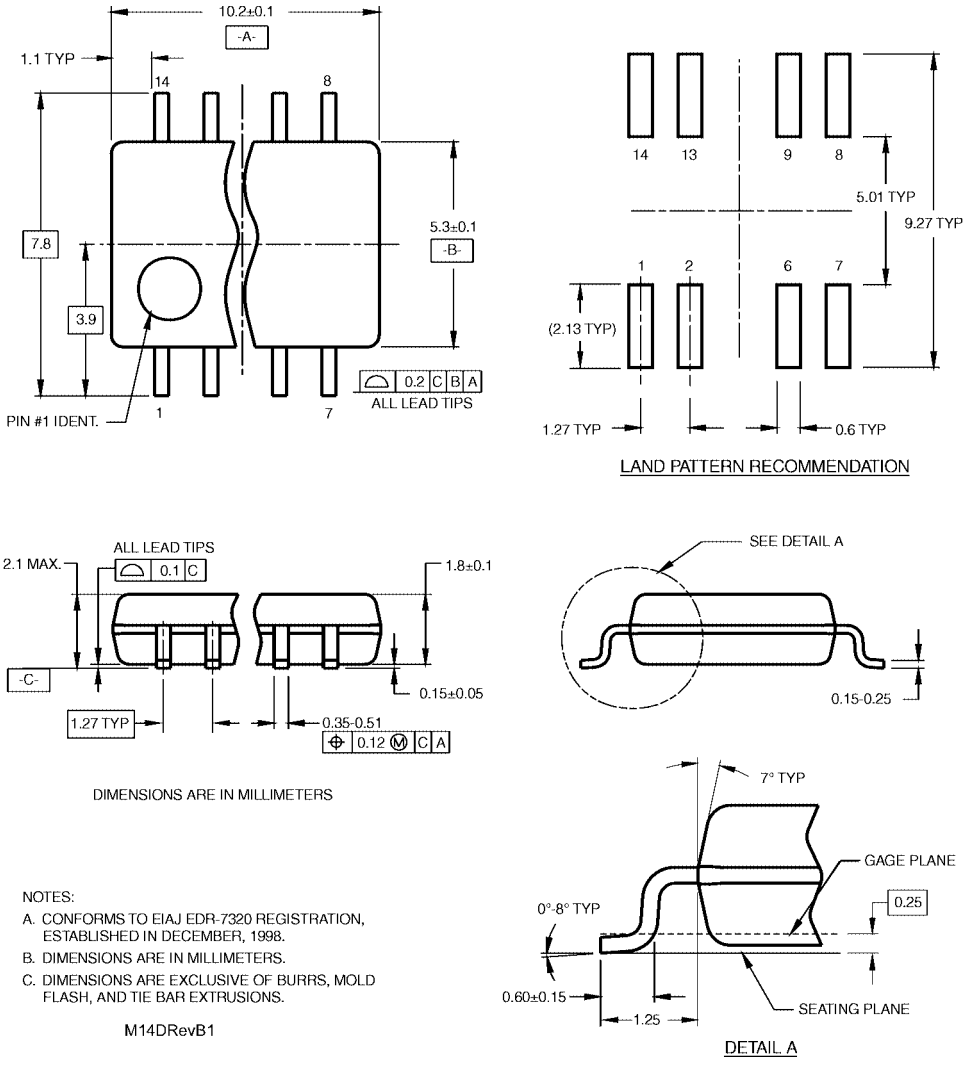
Symbol	Parameter	V_{CC} (V)	T_A = 25°C	T_A = −40°C to +85°C	Units
			Typ	Guaranteed Minimum	
$t_W(L)$	Minimum Pulse	3.3 ± 0.3		5.0	5.0	ns
$t_W(H)$	Width ($\overline{CP}$)	5.0 ± 0.5		5.0	5.0	
$t_W(H)$	Minimum Pulse	3.3 ± 0.3		5.0	5.0	ns
	Width (CLR)	5.0 ± 0.5		5.0	5.0	
t_{REM}	Minimum Removal	3.3 ± 0.3		5.0	5.0	ns
	Time	5.0 ± 0.5		4.0	4.0	

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

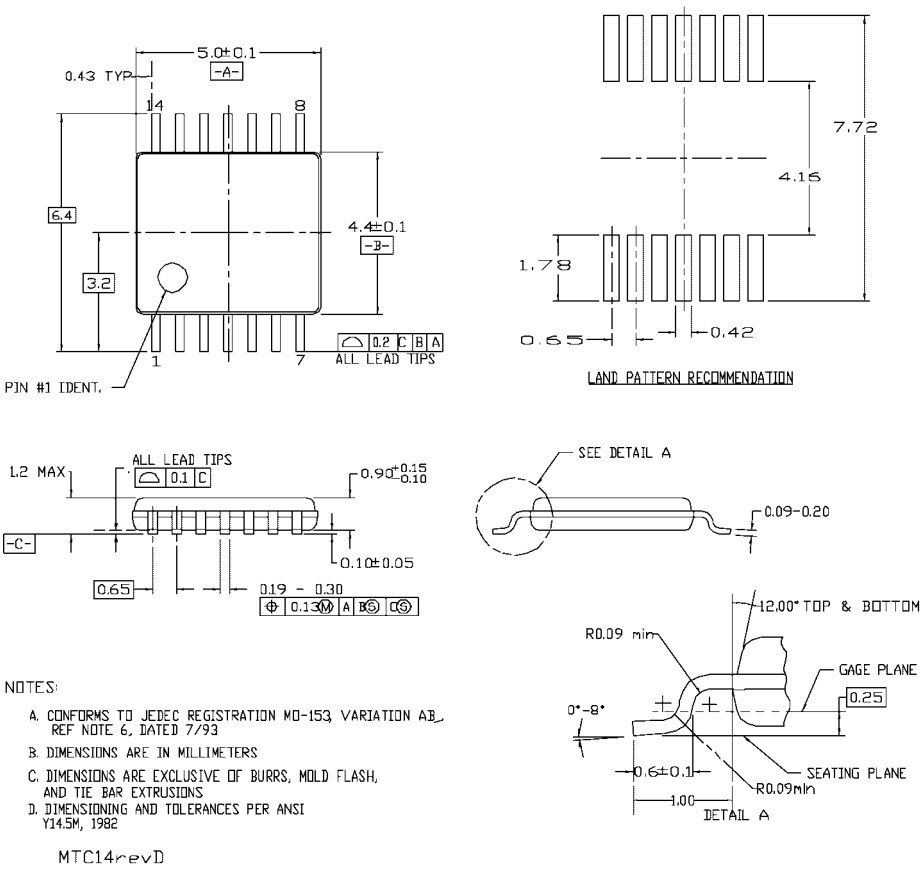
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

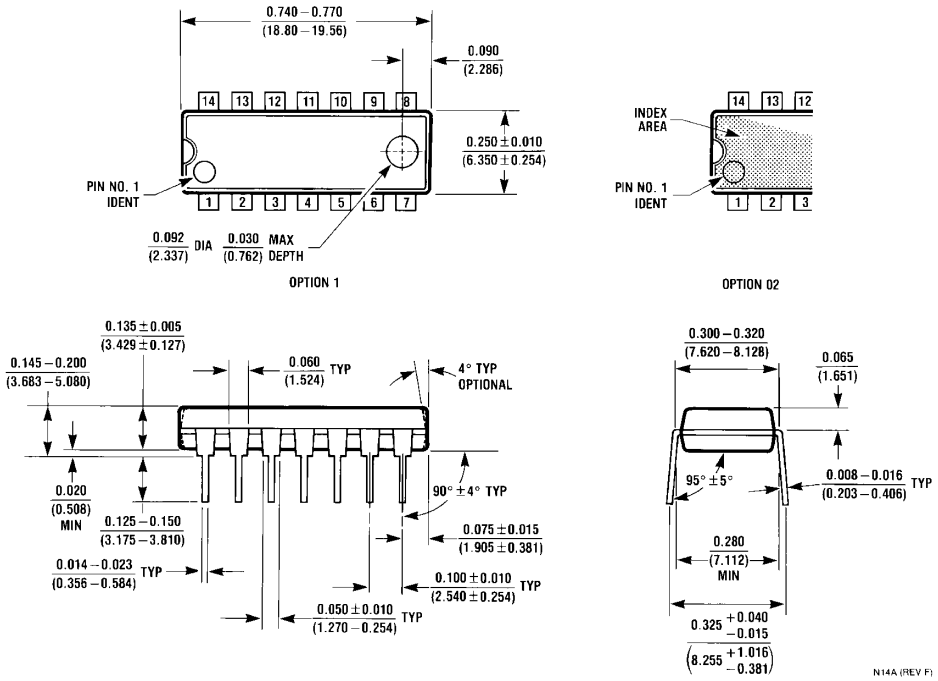
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A