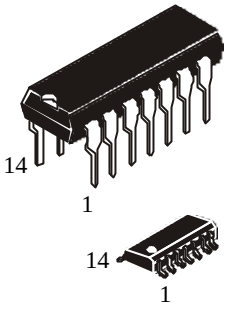
SL74LVU04

Hex Inverter



N SUFFIX
PLASTIC

D SUFFIX
SOIC

ORDERING INFORMATION

SL74LVU04N	Plastic
SL74LVU04D	SOIC
SL74LVU04	Chip

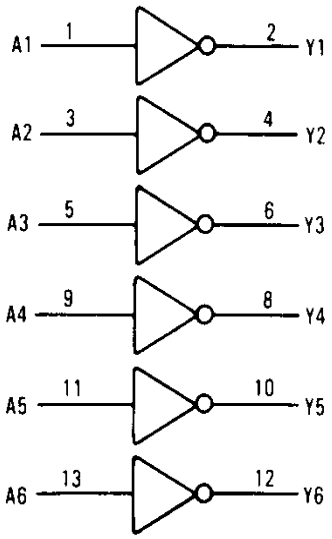
T_A = -40° ÷ 125° C for all packages

The 74LVU04 is a low-voltage, Si-gate CMOS device and is pin compatible with the 74HCU04.

The 74LVU04 is a general purpose hex inverter. Each of the six inverters is a single stage with unbuffered outputs.

- Wide Operating Voltage: 1.0÷5.5 V
- Optimized for Low Voltage applications: 1.0÷3.6 V
- Accepts TTL input levels between V_{CC} =2.7 V and V_{CC} =3.6 V
- Low Input Current

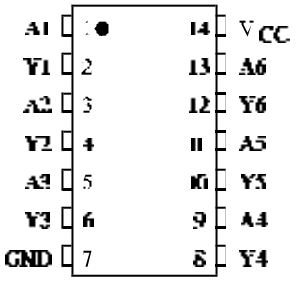
LOGIC DIAGRAM



$Y = \bar{A}$

PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Referenced to GND)	-0.5 ÷ +7.0	V
I_{IK} *[1]	DC input diode current	±20	mA
I_{OK} *[2]	DC output diode current	±50	mA
I_O *[3]	DC output source or sink current -bus driver outputs	±25	mA
I_{CC}	DC V_{CC} current for types with - bus driver outputs	±50	mA
I_{GND}	DC GND current for types with - bus driver outputs	±50	mA
P_D	Power dissipation per package, plastic DIP+ SOIC package+	750 500	mW
Tstg	Storage temperature	-65 ÷ +150	°C
T_L	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SOIC Package: : - 8 mW/°C from 70° to 125°C
*[1]: $V_I < -0.5V$ or $V_I > V_{CC}+0.5V$
*[2]: $Vo < -0.5V$ or $Vo > V_{CC}+0.5V$
*[3]: $-0.5V < Vo < V_{CC}+0.5V$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		1.0	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time	1.0 V≤V_{CC} <2.0 V	0	500	ns
		2.0 V≤V_{CC} <2.7 V	0	200	
		2.7 V≤V_{CC} <3.6 V	0	100	
		3.6 V≤V_{CC} ≤5.5 V	0	50	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}, V	Guaranteed Limit						Unit
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
				min	max	min	max	min	max	
V_{IH}	High-Level Input Voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	1.0 1.6 2.4 2.4 2.4 3.6 4.4		1.0 1.6 2.4 2.4 2.4 3.6 4.4		1.0 1.6 2.4 2.4 2.4 3.6 4.4		V
V_{IL}	Low -Level Input Voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.2 0.4 0.5 0.5 0.5 0.9 1.1	- - - - - - -	0.2 0.4 0.5 0.5 0.5 0.9 1.1	- - - - - - -	0.2 0.4 0.5 0.5 0.5 0.9 1.1	V
V_{OH}	High-Level Output Voltage	$V_I = V_{IH}$ or V_{IL} I_0=-100 ì A	1.2 2.0 2.7 3.0 3.6 4.5 5.5	1.05 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	V
		$V_I = V_{IH}$ or V_{IL} I_0=-6.0 mA	3.0	2.48	-	2.40	-	2.20	-	
		$V_I = V_{IH}$ or V_{IL} I_0=-12 mA	4.5	3.70	-	3.60	-	3.50	-	
V_{OL}	Low-Level Output Voltage	$V_I = V_{IH}$ or V_{IL} I_0=100 ì A	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.15 0.15 0.15 0.15 0.15 0.15 0.15	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	V
		$V_I = V_{IH}$ or V_{IL} I_0=6.0 mA	3.0	-	0.33	-	0.40	-	0.50	
		$V_I = V_{IH}$ or V_{IL} I_0=12 mA	4.5	-	0.40	-	0.55	-	0.65	
I_{IL}	Low-Level Input Leakage Current	V_I=0 V	5.5	-	-0.1	-	-1.0	-	-1.0	ì A

DC ELECTRICAL CHARACTERISTICS (continuation)

Symbol	Parameter	Test Conditions	V_{CC},	Guaranteed Limit			Unit
				25°C	-40°C ÷ 85°C	-40°C ÷ 125°C	

			V	min	max	min	max	min	max	
I_{IH}	High-Level Input Leakage Current	V_I= $V_{ÑÑ}$	5.5	-	0.1	-	1.0	-	1.0	
I_{CC}	Quiescent Supply Current (per Package)	V_I=0 Âor $V_{ÑÑ}$ I_O = 0 ì A	5.5	-	4.0	-	20	-	40	ì A
I_{CC1}	Additional Quiescent Supply Current on input	V_I = $V_{ÑÑ}$- 0.6V	2.7 3.6	- -	0.2 0.2	- -	0.5 0.5 -	- -	0.85 0.85	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_{LH} =t_{HL} = 2.5 ns, R_L=1 kÙ)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
				Min	max	min	max	min	max	
t_{PHL} (t_{PLH})	Propagation Delay, Input A to Output Y (Figure 1)	V_I=0 V or V_1 t_{LH} = t_{HL} =2.5 ns ÑL = 50 pF R_L = 1 kÙ	1.2 2.0 2.7 3.0 4.5	- - - - -	70 22 16 13 11	- - - - -	80 26 19 15 13	- - - - -	100 31 23 18 16	ns
C_I	Input Capacitance		5.5	-	7.0	-	-	-	-	pF
C_{PD}	Power Dissipation Capacitance (Per Inverter)			ÒÀ=25°Ñ, V_I=0V or V_{CC}						pF
				36						

Used to determine the no-load dynamic power consumption:

P_D = $C_{PD}V_{CC}^2f_I$+ ($C_LV_{CC}^2$fo), f_I - input frequency, fo - output frequency (MHz)

($C_LV_{CC}^2$fo) – sum of the outputs

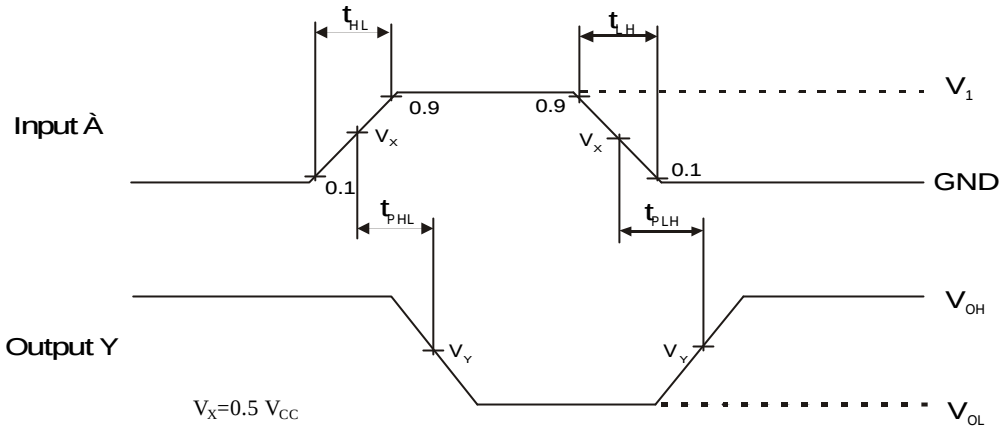
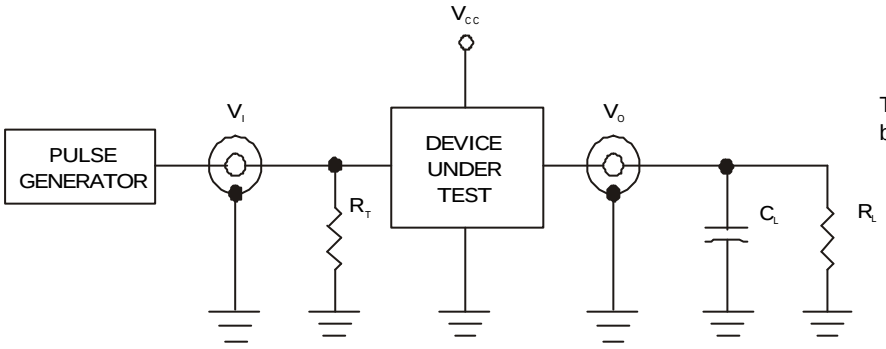


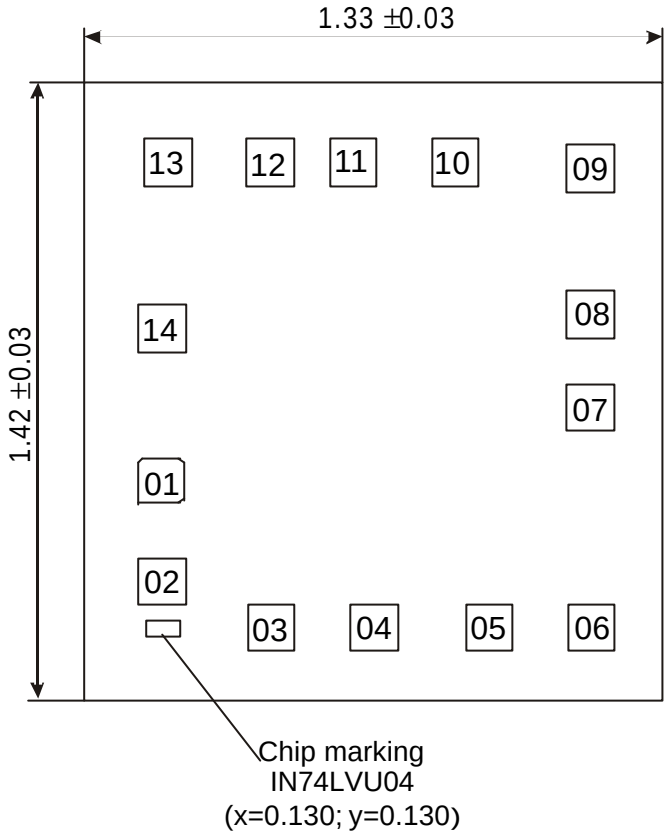
Figure 1. Switching Waveforms



Termination resistance R_T – should be equal to Z_{OUT} of pulse generators

Figure 2. Test circuit

CHIP PAD DIAGRAM SL74LVU04



Pad size 0.108 x 0.108 mm (Pad size is given as per metallization layer)
Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.130	0.463
02	Y1	0.130	0.230
03	A2	0.381	0.126
04	Y2	0.616	0.126
05	A3	0.881	0.126
06	Y3	1.116	0.126
07	GND	1.115	0.631
08	Y4	1.115	0.846
09	A4	1.115	1.181
10	Y5	0.804	1.194
11	A5	0.569	1.194
12	Y6	0.378	1.194
13	A6	0.143	1.194
14	V_{CC}	0.130	0.813