

# 74LVC544A

Octal D-type registered transceiver; inverting; 3-state

Rev. 4 — 18 December 2012

Product data sheet

## 1. General description

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The 74LVC544A is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable inputs ( $\overline{\text{LEAB}}$  and  $\overline{\text{LEBA}}$ ) and output enable inputs ( $\overline{\text{OEAB}}$  and  $\overline{\text{OEBA}}$ ) are provided for each register to permit independent control of input and output in either direction of the data flow.

The 74LVC544A contains eight D-type latches, with separate inputs and controls for each set. For data flow from pins A to B, for example, the A to B enable input (pin  $\overline{\text{EAB}}$ ) must be LOW in order to enter data from pins A0 to A7 or take data from pins B0 to B7. With pin  $\overline{\text{EAB}}$  LOW, a LOW signal on the A to B latch enable input (pin  $\overline{\text{LEAB}}$ ) makes the A to B latches transparent; a subsequent LOW-to-HIGH transition on pin  $\overline{\text{LEAB}}$  puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With pins  $\overline{\text{EAB}}$  and  $\overline{\text{OEAB}}$  both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

## 2. Features and benefits

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- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Supports partial power-down applications; inputs/outputs are high-impedance when  $V_{\text{CC}} = 0 \text{ V}$
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from  $-40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$  and  $-40 \text{ }^{\circ}\text{C}$  to  $+125 \text{ }^{\circ}\text{C}$

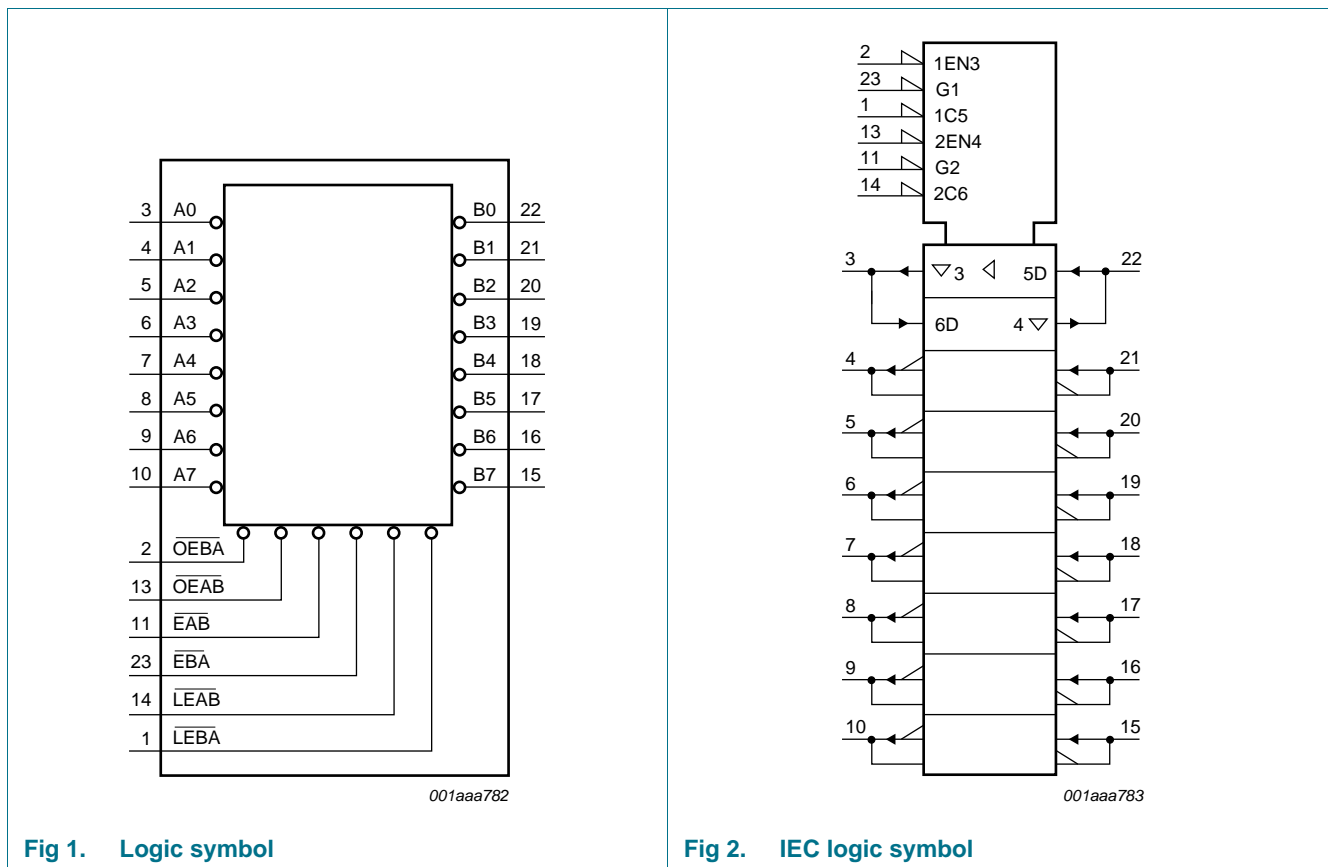


### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC544AD	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC544ADB	-40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC544APW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

### 4. Functional diagram



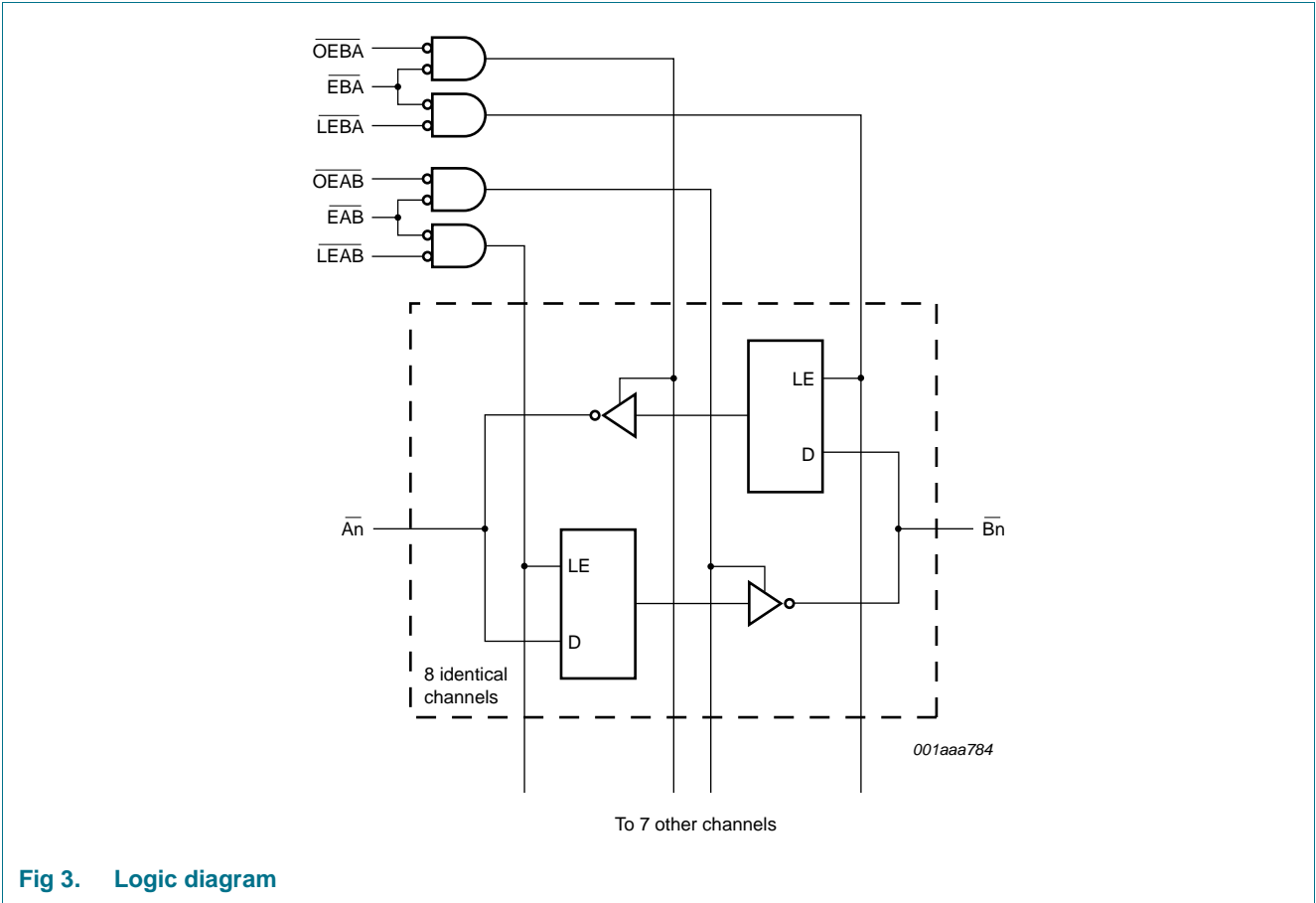


Fig 3. Logic diagram

## 5. Pinning information

### 5.1 Pinning

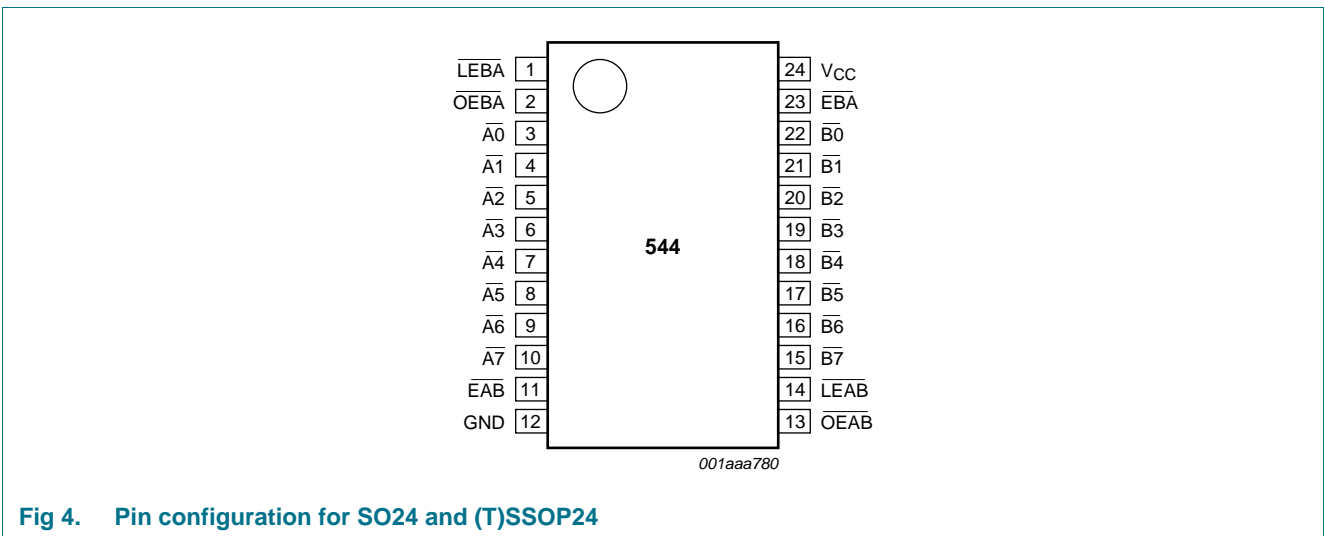


Fig 4. Pin configuration for SO24 and (T)SSOP24

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{LEBA}}$	1	B to A latch enable input (active LOW)
$\overline{\text{OEBA}}$	2	B to A output enable input (active LOW)
$\overline{\text{A0}}$	3	A data input or output
$\overline{\text{A1}}$	4	A data input or output
$\overline{\text{A2}}$	5	A data input or output
$\overline{\text{A3}}$	6	A data input or output
$\overline{\text{A4}}$	7	A data input or output
$\overline{\text{A5}}$	8	A data input or output
$\overline{\text{A6}}$	9	A data input or output
$\overline{\text{A7}}$	10	A data input or output
$\overline{\text{EAB}}$	11	A to B enable input (active LOW)
GND	12	ground (0 V)
$\overline{\text{OEAB}}$	13	A to B output enable input (active LOW)
$\overline{\text{LEAB}}$	14	A to B latch enable input (active LOW)
$\overline{\text{B7}}$	15	B data output or input
$\overline{\text{B6}}$	16	B data output or input
$\overline{\text{B5}}$	17	B data output or input
$\overline{\text{B4}}$	18	B data output or input
$\overline{\text{B3}}$	19	B data output or input
$\overline{\text{B2}}$	20	B data output or input
$\overline{\text{B1}}$	21	B data output or input
$\overline{\text{B0}}$	22	B data output or input
$\overline{\text{EBA}}$	23	B to A enable input (active LOW)
V <sub>CC</sub>	24	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Input				Output
	OEAB, OEBA	EAB, EBA	LEAB, LEBA	An, Bn	Bn, An
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled plus latch	L	↑	L	h	Z
	L	↑	L	l	Z
Latch plus display	L	L	↑	h	L
	L	L	↑	l	H
Transparent	L	L	L	H	L
	L	L	L	L	H
Hold (do nothing)	L	L	H	X	NC

[1] XX = AB for A to B direction and BA for B to A direction

H = HIGH voltage level

L = LOW voltage level

h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of  $\overline{LEAB}$ ,  $\overline{LEBA}$ ,  $\overline{EAB}$  and  $\overline{EBA}$

l = LOW state must be present one set-up time before the LOW-to-HIGH transition of  $\overline{LEAB}$ ,  $\overline{LEBA}$ ,  $\overline{EAB}$  and  $\overline{EBA}$

X = don't care

↑ = LOW to HIGH level transition

NC = no change

Z = high-impedance OFF-state

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO24 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

For (T)SSOP24 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
I <sub>I</sub>	input leakage current	I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 5.5 V or GND; <sup>[2]</sup>	-	0.1	±10	-	±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	0.1	±10	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

[2] For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	$\overline{A_n}$ to $\overline{B_n}$ ; $\overline{B_n}$ to $\overline{A_n}$ ; see <a href="#">Figure 5</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	17	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	7.4	14.9	1.0	17.1	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.9	7.8	1.0	9.0	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.9	7.5	1.5	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.3	6.5	1.0	8.5	ns
		$\overline{LEBA}$ to $\overline{A_n}$ ; $\overline{LEAB}$ to $\overline{B_n}$ ; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.2 V	-	19	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	7.5	17.5	1.5	20.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.9	9.0	1.0	10.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.3	8.5	1.5	11.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.3	7.5	1.0	9.5	ns

**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>en</sub>	enable time	OEBA to $\overline{\text{An}}$ ; OEAB to $\overline{\text{Bn}}$ ; see <a href="#">Figure 8</a> 						
		V <sub>CC</sub> = 1.2 V	-	18	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.7	7.5	19.4	1.7	22.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.2	10.7	1.5	12.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.3	9.5	1.5	12.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.4	8.5	1.0	11.0	ns
		EBA to $\overline{\text{An}}$ ; EAB to $\overline{\text{Bn}}$ ; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.2 V	-	20	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	8.1	20.4	1.9	23.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.5	11.2	1.5	12.9	ns
t <sub>dis</sub>	disable time	OEBA to $\overline{\text{An}}$ ; OEAB to $\overline{\text{Bn}}$ ; see <a href="#">Figure 8</a> 						
		V <sub>CC</sub> = 1.2 V	-	8.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.8	5.0	11.2	2.8	13.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	6.4	1.0	7.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.6	7.5	1.5	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.3	6.5	1.0	8.5	ns
		EBA to $\overline{\text{An}}$ ; EAB to $\overline{\text{Bn}}$ ; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.2 V	-	9.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.0	5.1	12.0	3.0	13.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.9	6.8	1.0	7.9	ns
t <sub>w</sub>	pulse width	LEX $\overline{\text{X}}$ LOW; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	2.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	0.9	-	2.0	-	ns
t <sub>su</sub>	set-up time	$\overline{\text{An}}$ , $\overline{\text{Bn}}$ to $\overline{\text{LEXX}}$ , $\overline{\text{EXX}}$ ; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	2.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-0.5	-	2.0	-	ns
t <sub>h</sub>	hold time	$\overline{\text{An}}$ , $\overline{\text{Bn}}$ to $\overline{\text{LEXX}}$ , $\overline{\text{EXX}}$ ; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	-	-	1.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	1.5	-	3.0	-	ns



**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	1.0	-	1.5	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$	-	8.1	-	-	-	pF
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	11.8	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	15.1	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V}$  and  $3.3\text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

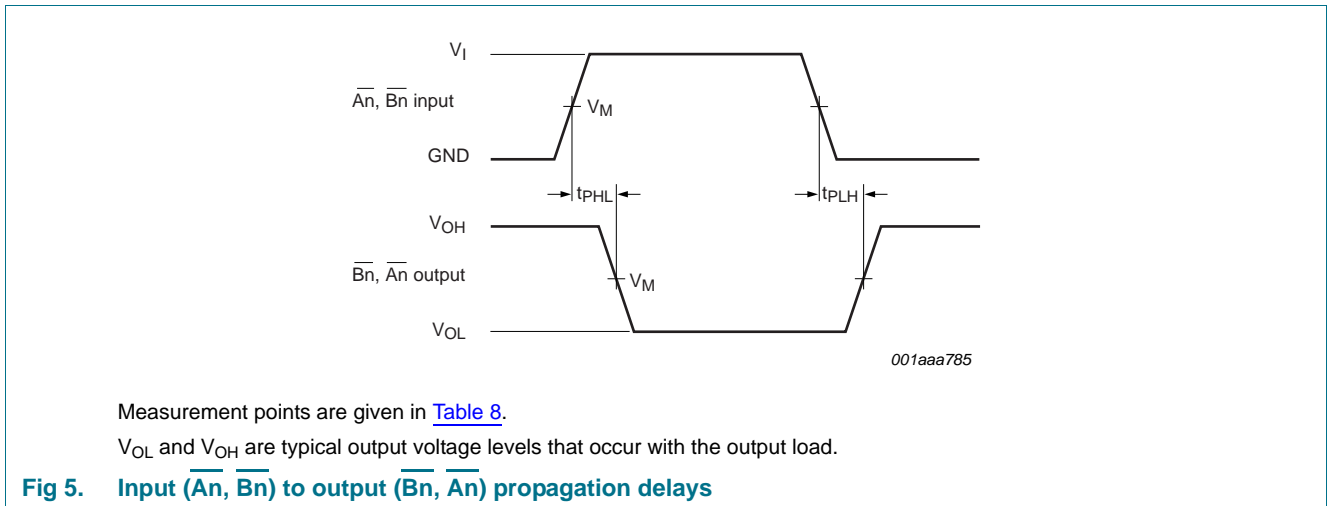
$C_L$  = output load capacitance in pF

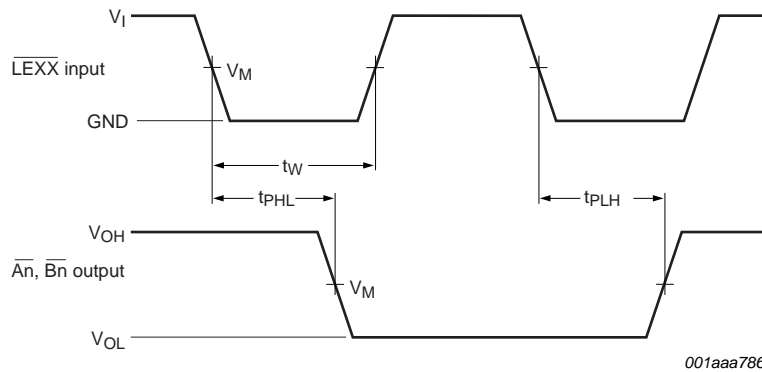
$V_{CC}$  = supply voltage in Volts

$N$  = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

## 11. Waveforms

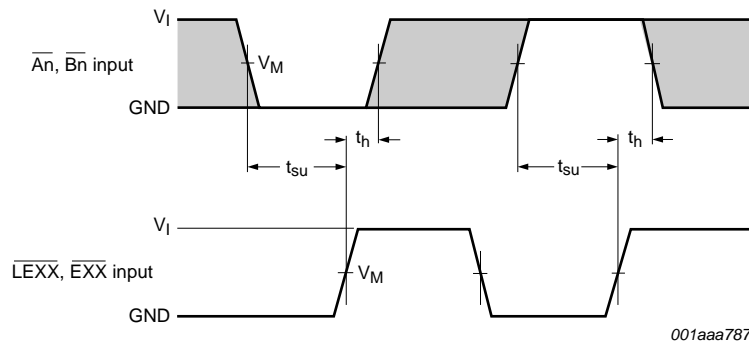




Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

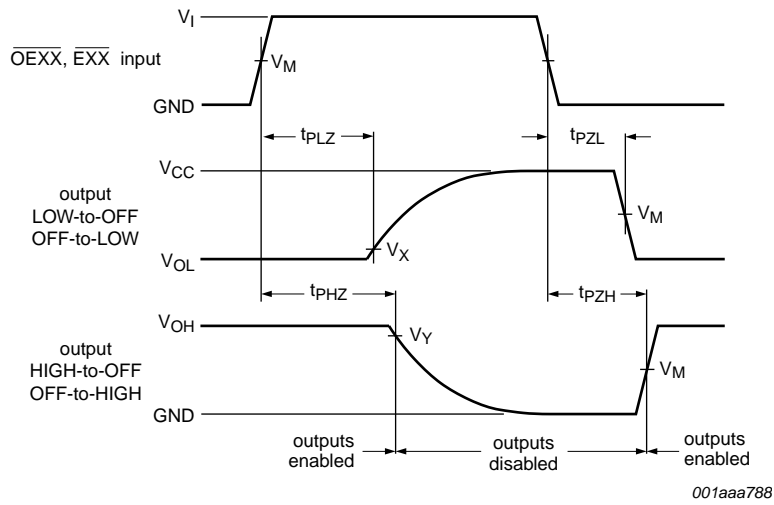
**Fig 6. Latch enable input (LEXX) pulse width and latch enable input to output ( $\overline{A_n}$ ,  $\overline{B_n}$ ) propagation delays**



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance

**Fig 7. Data set-up and hold times for the inputs ( $\overline{A_n}$ ,  $\overline{B_n}$ ) to  $\overline{LEXX}$  and  $\overline{EXX}$  inputs**



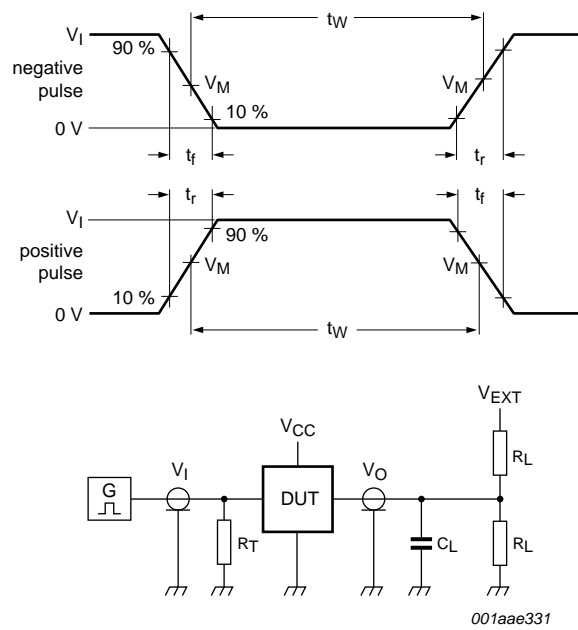
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. 3-state enable and disable times**

**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 9. Load circuitry for switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

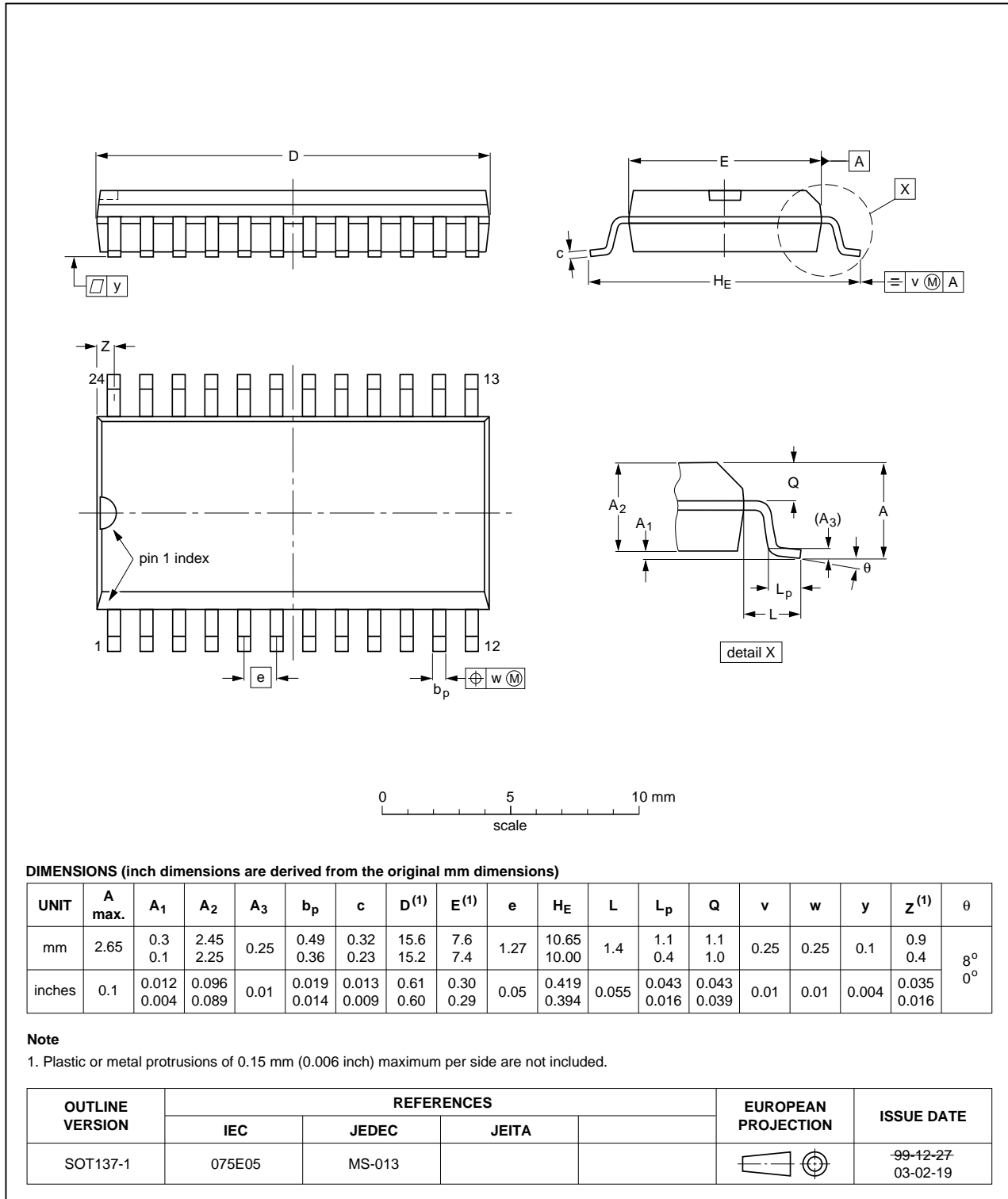


Fig 10. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

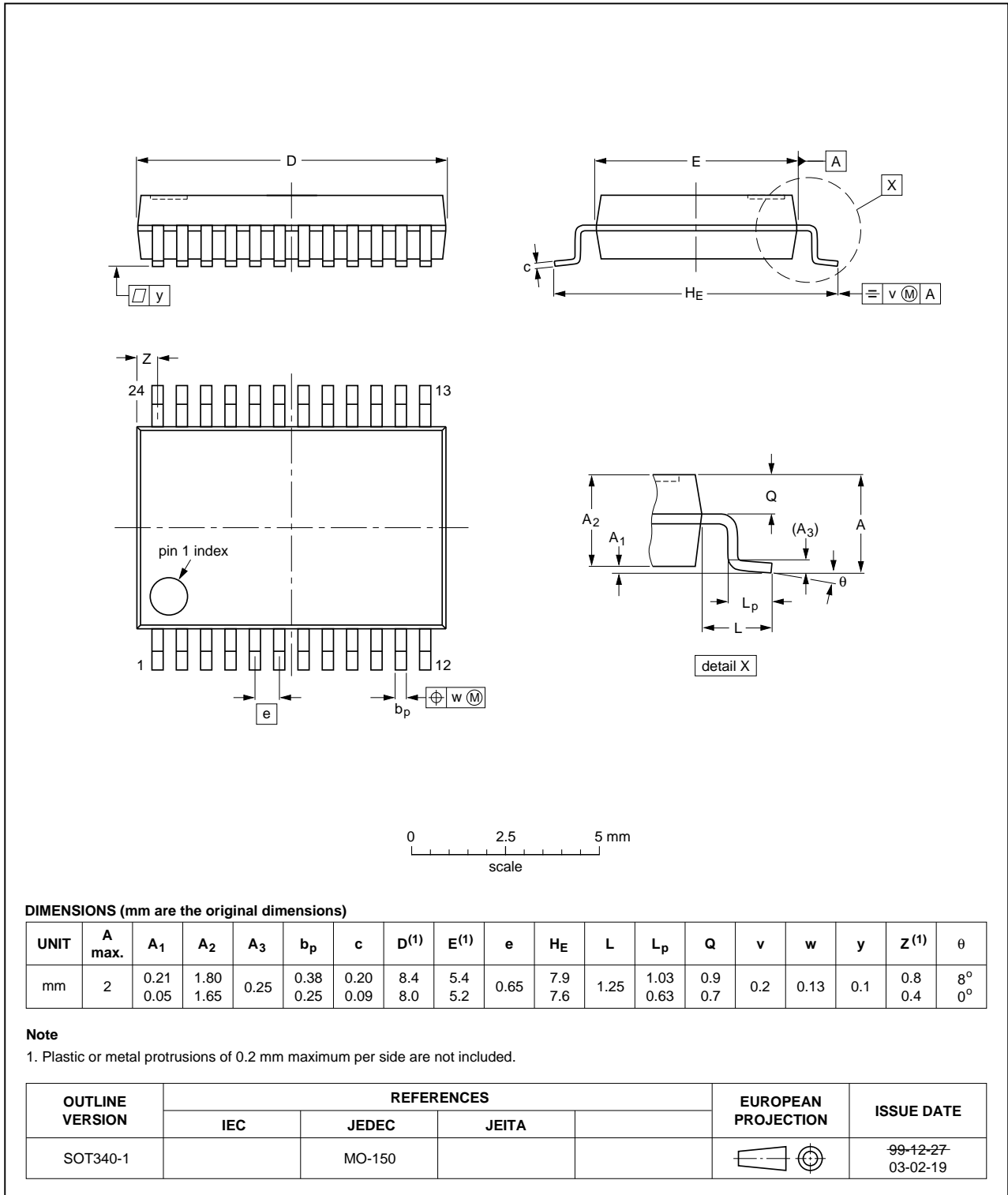


Fig 11. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

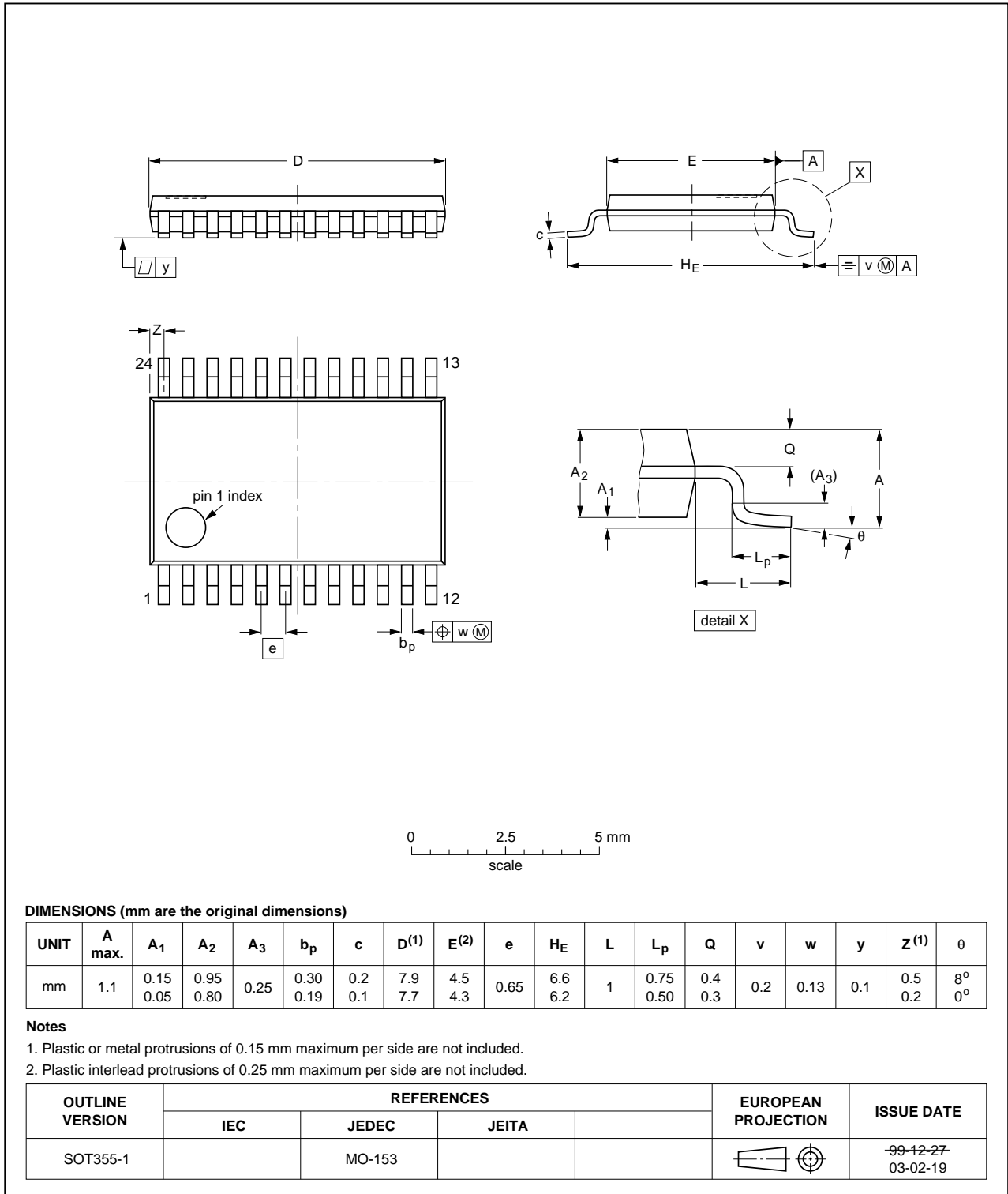


Fig 12. Package outline SOT355-1 (TSSOP24)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC544A v.4	20121218	Product data sheet	-	74LVC544A v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC544A v.3	20040511	Product specification	-	74LVC544A v.2
74LVC544A v.2	19980729	Product specification	-	74LVC544A v.1
74LVC544A v.1	19981110	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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