DATA SHEET

74LVC544A

Octal D-type registered transceiver, inverting (3-State)

Product specification

1998 Jul 29

Philips
Semiconductors

PHILIPS

Octal D-type registered transceiver, inverting (3-State)

74LVC544A

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Combines 74LVC640 and 74LVC533 type functions in one chip
- Octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State inverting outputs for bus oriented applications
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC544A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC544A is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}$AB, $\overline{LE}$BA) and output enable ($\overline{OE}$AB, $\overline{OE}$BA) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The '544A' contains eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{E}$AB) input must be LOW in order to enter data from $\overline{A0}$–$\overline{A7}$ or take data from $\overline{B0}$–$\overline{B7}$, as indicated in the function table.

With $\overline{E}$AB LOW, a LOW signal on the A-to-B latch enable ($\overline{LE}$AB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LE}$AB signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}$AB and $\overline{OE}$AB both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{An}$ to $\overline{Bn}$	C_L = 50pF V_{CC} = 3.3V	4	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

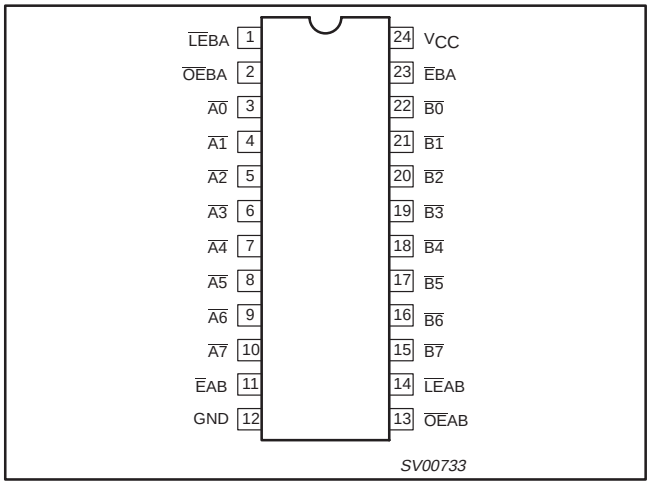
ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC544A D	74LVC544A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC544A DB	74LVC544A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC544A PW	7LVC544APW DH	SOT355-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LE}$BA	'B' to 'A' latch enable input (active LOW)
2	$\overline{OE}$BA	'B' to 'A' output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A0}$–$\overline{A7}$	'A' data inputs/outputs
11	$\overline{E}$BA	'B' to 'A' enable input (active LOW)
12	GND	Ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B0}$–$\overline{B7}$	'B' data inputs/outputs
13	$\overline{OE}$AB	'A' to 'B' output enable input (active LOW)
14	$\overline{LE}$AB	'A' to 'B' latch enable input (active LOW)
23	$\overline{E}$AB	'A' to 'B' enable input (active LOW)
24	VCC	Positive supply voltage

PIN CONFIGURATION

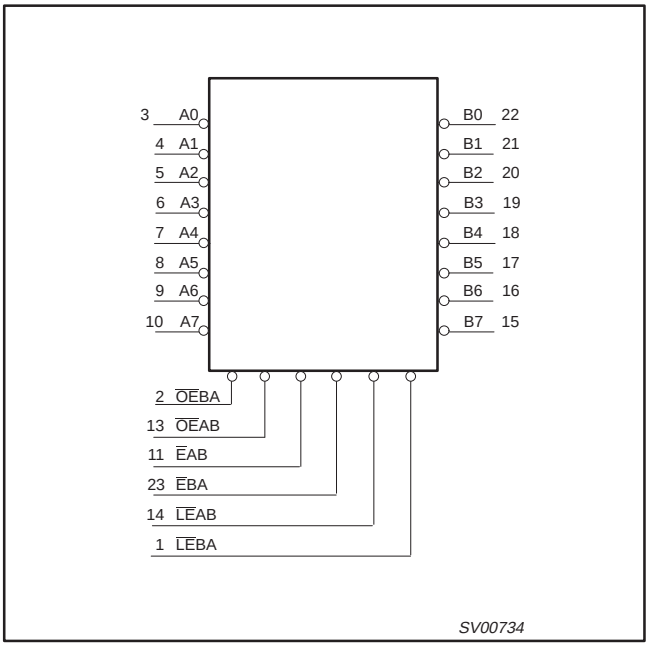


FUNCTION TABLE

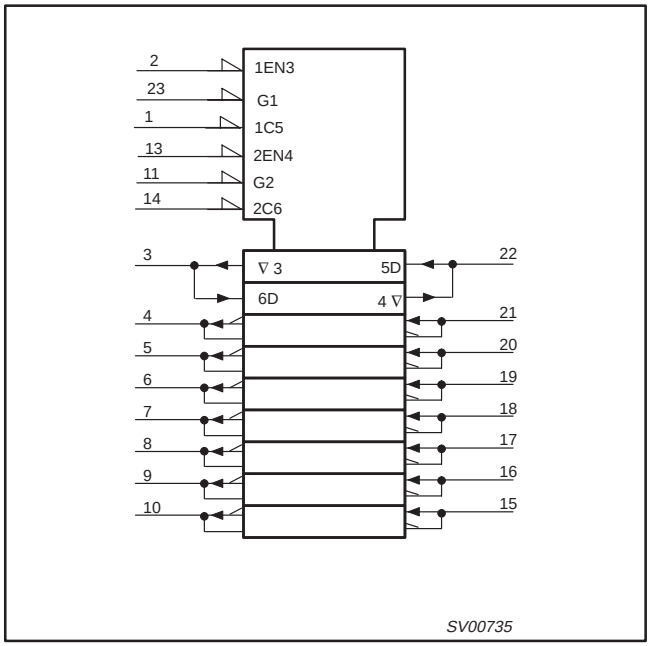
INPUTS				OUTPUTS	STATUS
$\overline{OE}$XX	$\overline{E}$XX	$\overline{LE}$XX	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}$AB, $\overline{LE}$BA, $\overline{E}$AB, $\overline{E}$BA
l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}$AB, $\overline{LE}$BA, $\overline{E}$AB, $\overline{E}$BA
X = Don't care
↑ = LOW–to–HIGH level transition
NC = No change
Z = High impedance OFF-state

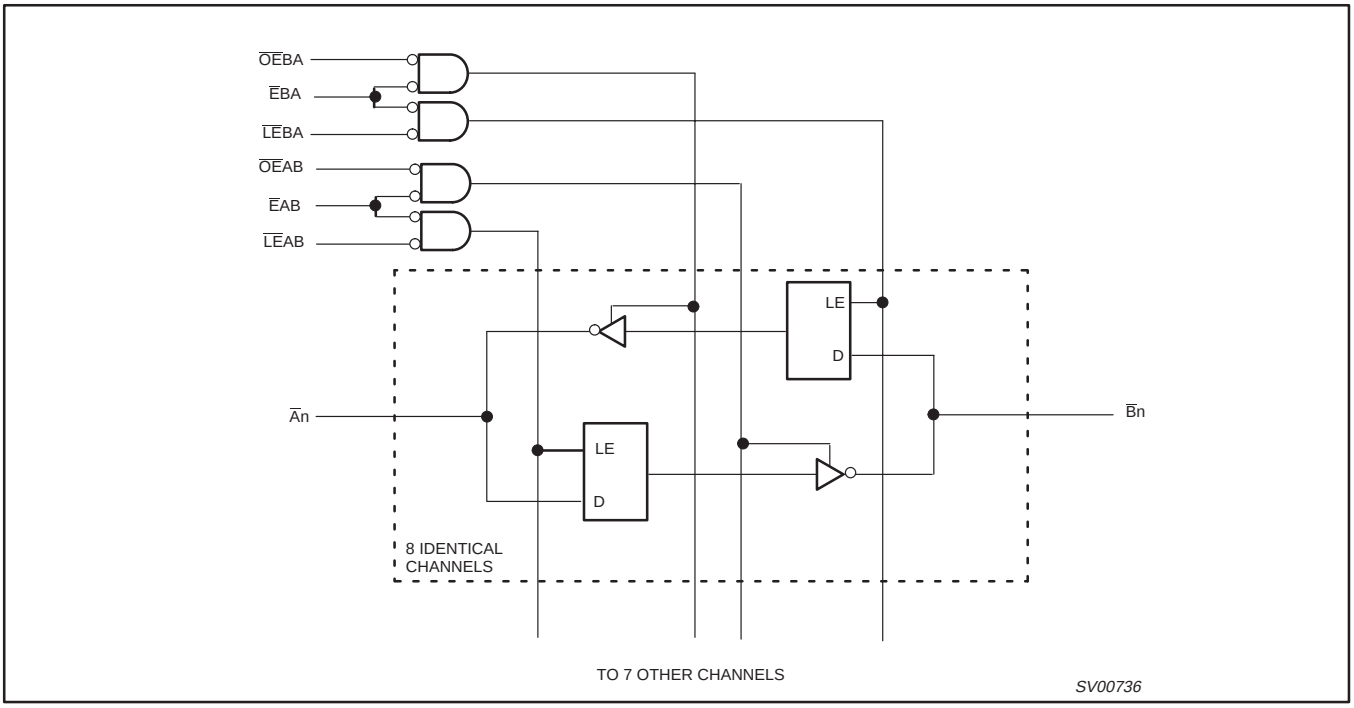
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or $V_{IL;}$ I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or $V_{IL;}$ I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or $V_{IL;}$ I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I = 5.5V; V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $\overline{A}n$ to $\overline{B}n$, $\overline{B}n$ to $\overline{A}n$	Figures 1, 5	1.5	4	6.5	1.5	7.5	ns
t_{PHL}/t_{PLH}	Propagation delay $\overline{LE}BA$ to $\overline{A}n$, $\overline{LE}AB$ to $\overline{B}n$	Figures 2, 5	1.5	4.3	7.5	1.5	8.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}BA$ to $\overline{A}n$, $\overline{OE}AB$ to $\overline{B}n$	Figures 3, 5	1.5	4.5	8.5	1.5	9.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}BA$ to $\overline{A}n$, $\overline{OE}AB$ to $\overline{B}n$	Figures 3, 5	1.5	3.9	6.5	1.5	7.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{E}BA$ to $\overline{A}n$, $\overline{E}AB$ to $\overline{B}n$	Figures 3, 5	1.5	4.7	8.9	1.5	9.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{E}BA$ to $\overline{A}n$, $\overline{E}AB$ to $\overline{B}n$	Figures 3, 5	1.5	3.9	6.9	1.5	7.9	ns
t_W	$\overline{LE}XX$ pulse width HIGH	Figure 2	2.0	–	–	2.0	–	ns
t_{su}	Set-up time $\overline{A}n/\overline{B}n$ to $\overline{LE}XX$, $\overline{A}n/\overline{B}n$ to $\overline{E}XX$	Figure 4	2.0	–	–	2.0	–	ns
t_h	Hold time $\overline{A}n/\overline{B}n$ to $\overline{LE}XX$, $\overline{A}n/\overline{B}n$ to $\overline{E}XX$	Figure 4	4.0	–	–	1.0	–	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

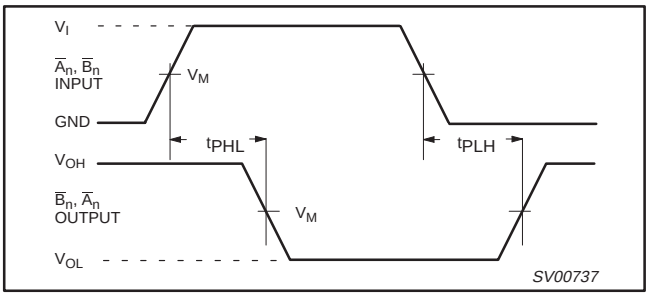


Figure 1. Input (An, Bn) to output (Bn, An) propagation delays.

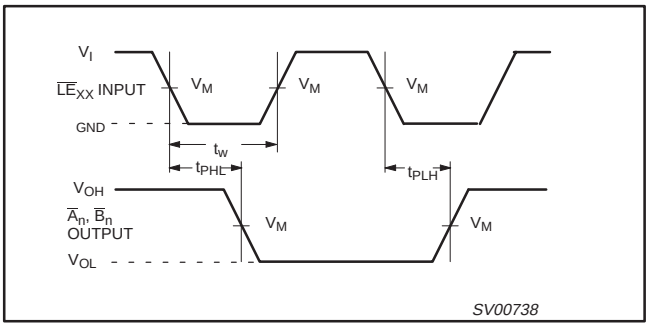


Figure 2. Latch enable input (LEXX) pulse width, the latch enable input to output (An, Bn) propagation delays.

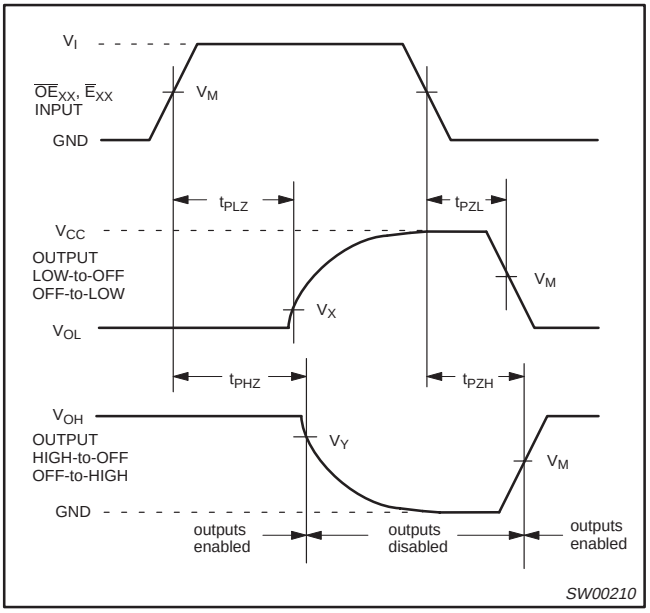


Figure 3. 3-State enable and disable times

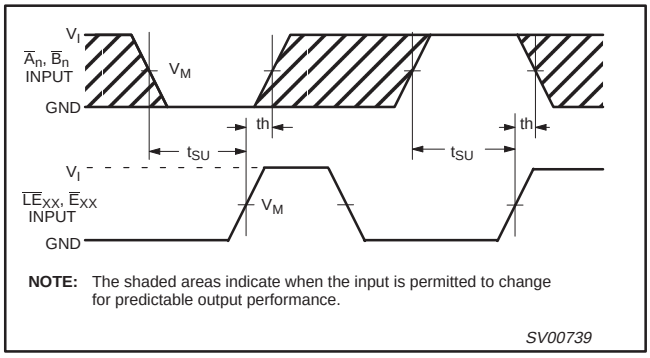
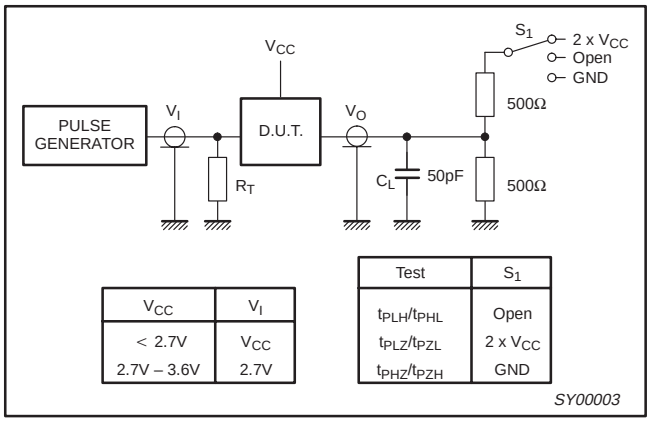


Figure 4. Data set-up and hold times for the (An, Bn) input to the LEXX and EXX inputs

TEST CIRCUIT

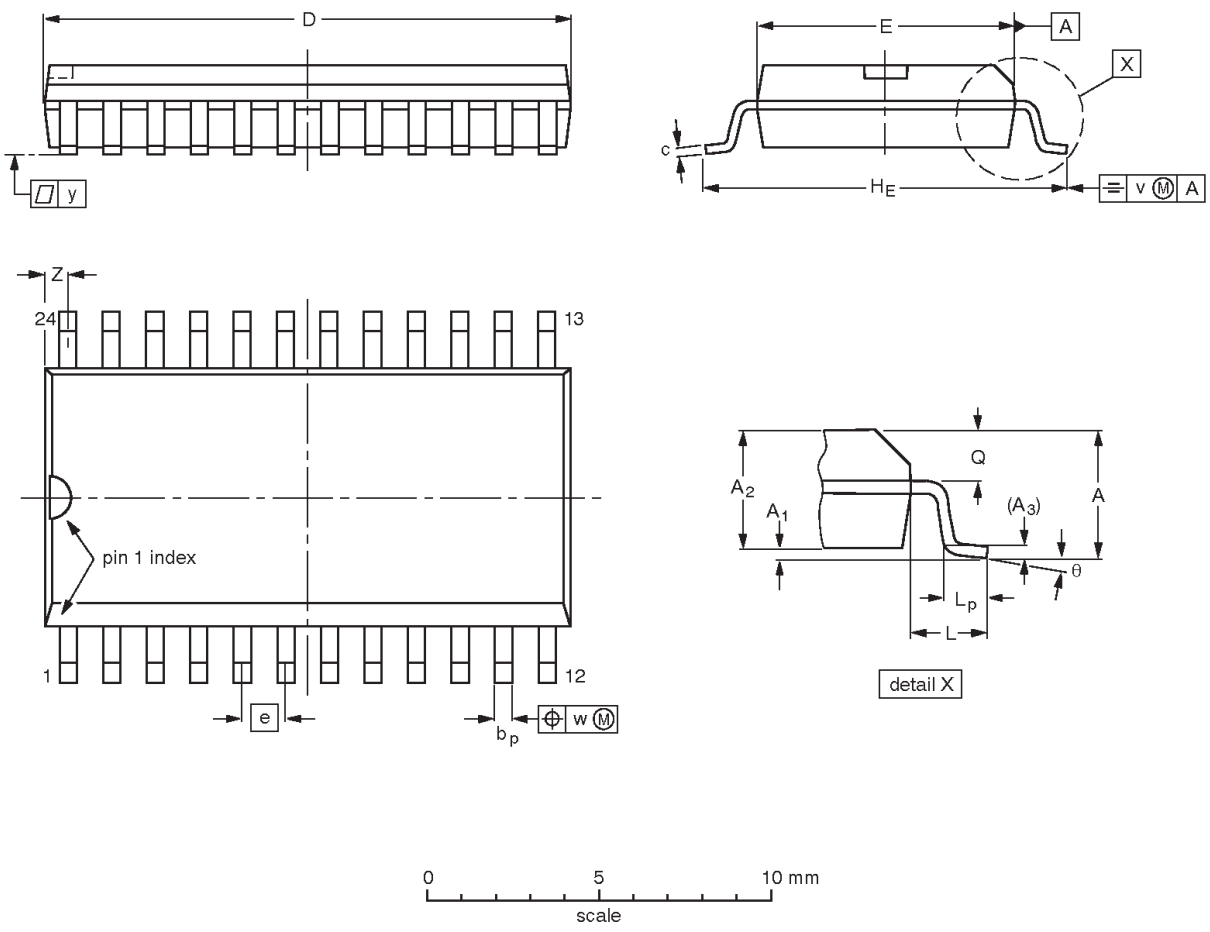


V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 5. Load circuitry for switching times

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

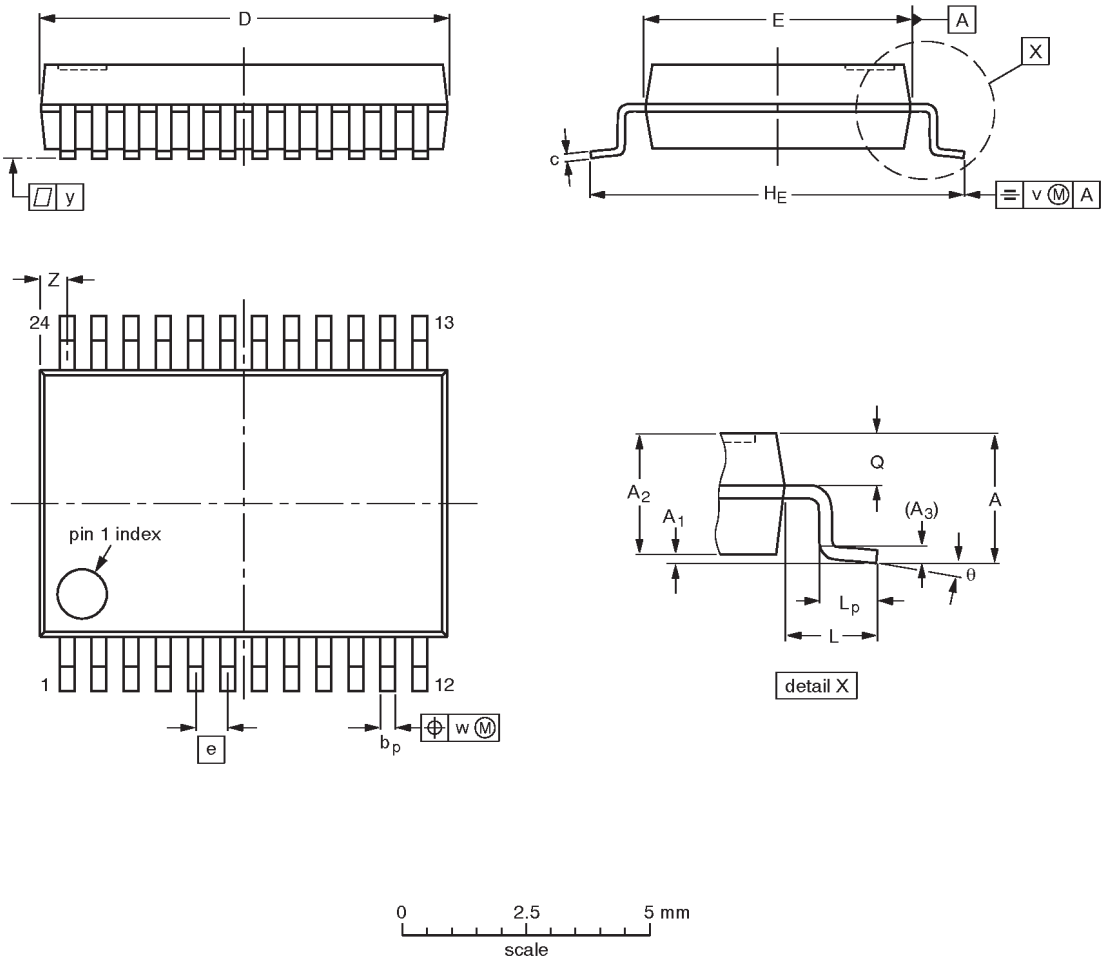
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

print code Date of release: 08-98

Document order number: 9397-750-04512

Let's make things better.

Philips Semiconductors

PHILIPS