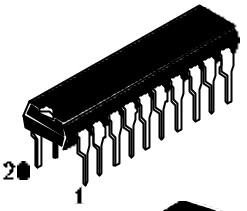
OCTAL D-TYPE TRANSPARENT LATCH (3-State)

SL74LV373 are compatible by pinning with SL74HC373 and SL74HCT373 series. Input voltage levels are compatible with standard CMOS levels.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Voltage supply range: 2.0 to 3.2 V
- LOW input current: 1.0 µÀ; 0.1 µÀ at Ò= 25 °Ñ
- Input current LOW/HIGH: 8 mÀ
- Latch current: not less than 150 mÀ at Ò= 125 °Ñ
- ESD acceptable value: not less than 2000 V as per HBM and not less than 200 V as per MM
-

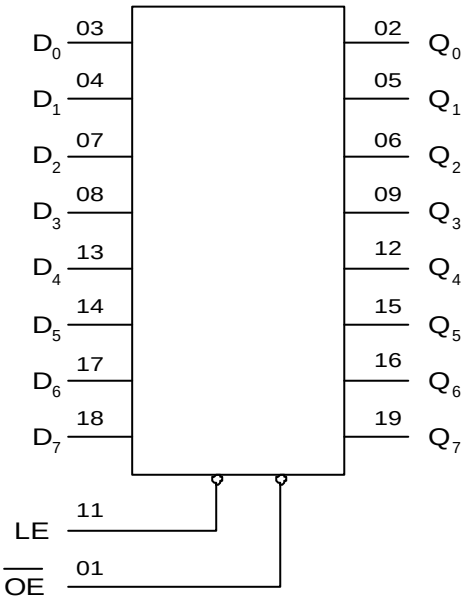


N SUFFIX
PLASTIC

D SUFFIX
SOIC

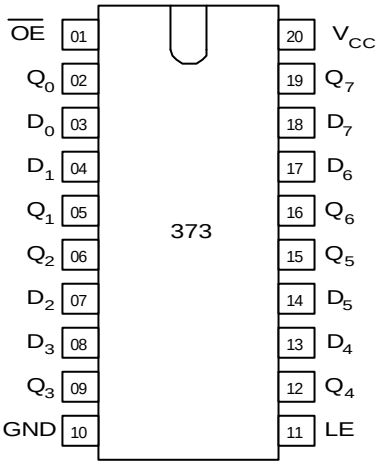
ORDERING INFORMATION
SL74LV373N Plastic DIP
SL74LV373D SOIC
T_A = -40° to 125° C
for all packages

BLOCK DIAGRAM



Pin 20=V_{CC}
Pin 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
$\overline{OE}$	LE	Dn	Qn
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 to +5.0	V
I_{IK} *1	Input diode current	±20	mÀ
I_{OK} *2	Output diode current	±50	mÀ
I_O *3	Output source or sink current	±35	mÀ
I_{CC}	V_{CC} current	±70	mÀ
I_{GND}	GND current	±70	mÀ
P_D	Power dissipation per package: Plastic DIP *4 SOIC *4	 750 500	mW
Tstg	Storage temperature range	-65 to +150	°C

* In absolute maximum ratings modes functioning is not guaranteed. Upon lifting the absolute maximum ratings functioning is guarateed at the recommended operatng conditions.
*1 Provided $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 Provided $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 Provided -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 When operating in the temperature range of 70°Ñto 125°C power dissipation value decreses:
- for Plastic DIP by 12 mW/°C
- for SOIC by 8 mW/°C

RECOMMENDED OPERAING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		1.2	3.6	V
V_{IN}	Input voltage		0	V_{CC}	V
V_{OUT}	Output voltage		0	V_{CC}	V
T_A	Operating ambient temperature range. For all types of packages		-40	125	°C
t_{LH}, t_{HL}	Input rise and fall times	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0	1000 700 500 400	ns

DC CHARACTERISTICS

Symbol	Parameter	Test conditions	V_{CC}, V	Limits						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level voltage	V_O = V_{CC}-0.1 V	1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	LOW level voltage	V_O =0.1 V	1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	HIGH level output voltage	V_I = V_{IH} or V_{IL} I_O = -50 µA	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		V_I = V_{IH} or V_{IL} I_O = -8 mA	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	LOW level output voltage	V_I = V_{IH} or V_{IL} I_O = 50 µA	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.1	- - - -	0.1 0.1 0.1 0.1	V
		V_I = V_{IH} or V_{IL} I_O = 8 mA	3.0	-	0.33	-	0.4	-	0.5	V
I_I	Input current	V_I = V_{CC} or 0 V	3.6	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	3-state outputs V_I = V_{IL} or V_{IH} V_O =V_{CC} or 0 V	3.6	-	±0.5	-	±5	-	±10	µA
I_{CC}	Supply current	V_I =V_{CC} or 0 V I_O = 0 µA	3.6	-	8.0	-	80	-	160	µA

AC CHARACTERISTICS (C_L=50 pF, t_{LH} = t_{HL} = 6.0 ns)

Symbol	Parameter	Test conditions	V_{CC}, V	Limits						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH} from Dn to Qn	Propagation delay	Figure 1	1.2 2.0 3.0	- - -	150 38 23	- - -	190 48 29	- - -	220 58 35	ns
t_{PHL}, t_{PLH} from LE to Qn	Propagation delay	Figure 2	1.2 2.0 3.0	- - -	180 45 27	- - -	230 56 34	- - -	270 68 41	
t_{PHZ} t_{PLZ} from OE to Qn	3-state output enable time	Figure 4	1.2 2.0 3.0	- - -	160 35 23	- - -	200 43 28	- - -	240 45 32	
t_{PZH} t_{PZL} from OE to Qn	3-state disable time	Figure 4	1.2 2.0 3.0	- - -	160 40 24	- - -	200 50 30	- - -	240 60 36	
t_{THL}, t_{TLH}	HIGH-to-LOW and LOW-to-HIGH transition time	Figures 1,2	1.2 2.0 3.0	- - -	75 16 10	- - -	100 20 13	- - -	120 24 15	
t_W	Clock pulse width HIGH or LOW	Figure 2	1.2 2.0 3.0	250 30 18	- - -	350 34 20	- - -	450 41 24	- - -	
t_{SU}	Set-up time Dn to LE	Figure 3	1.2 2.0 3.0	45 15 9	- - -	50 17 10	- - -	100 15 12	- - -	
t_H	Hold time Dn to LE	Figure 3	1.2 2.0 3.0	25 5 5	- - -	25 5 5	- - -	25 5 5	- - -	
C_I	Input capacitance		3.0	-	7	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per flip-flop)	V_I = 0 V or V_{CC}	3.0	-	80	-	-	-	-	

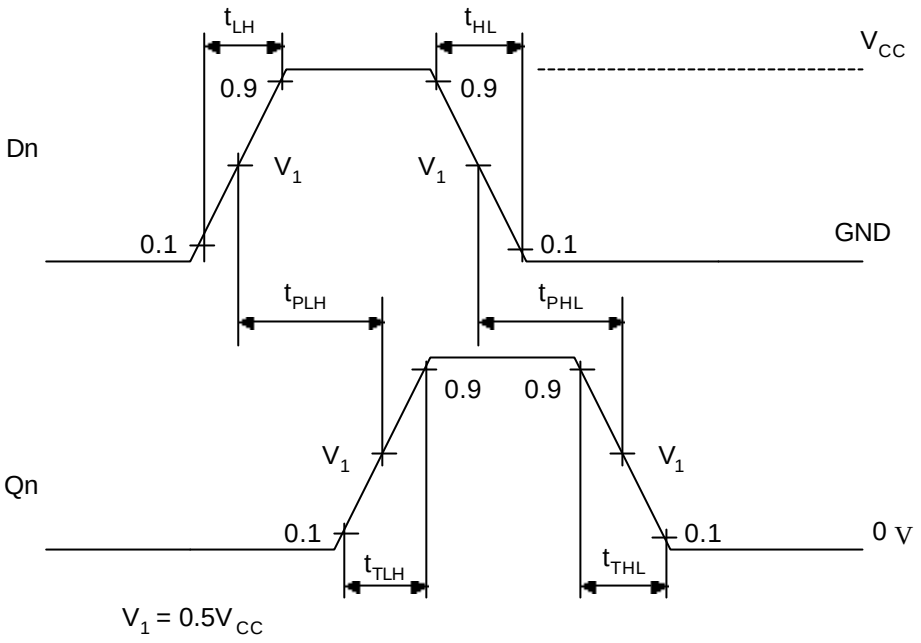


Figure 1 - Time diagram

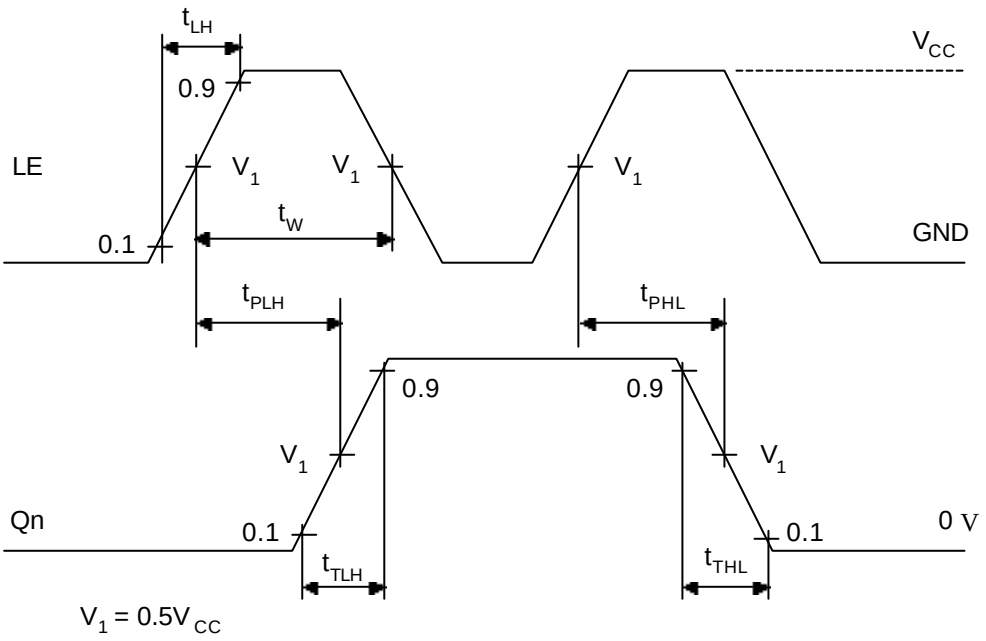


Figure 2 - Time diagram

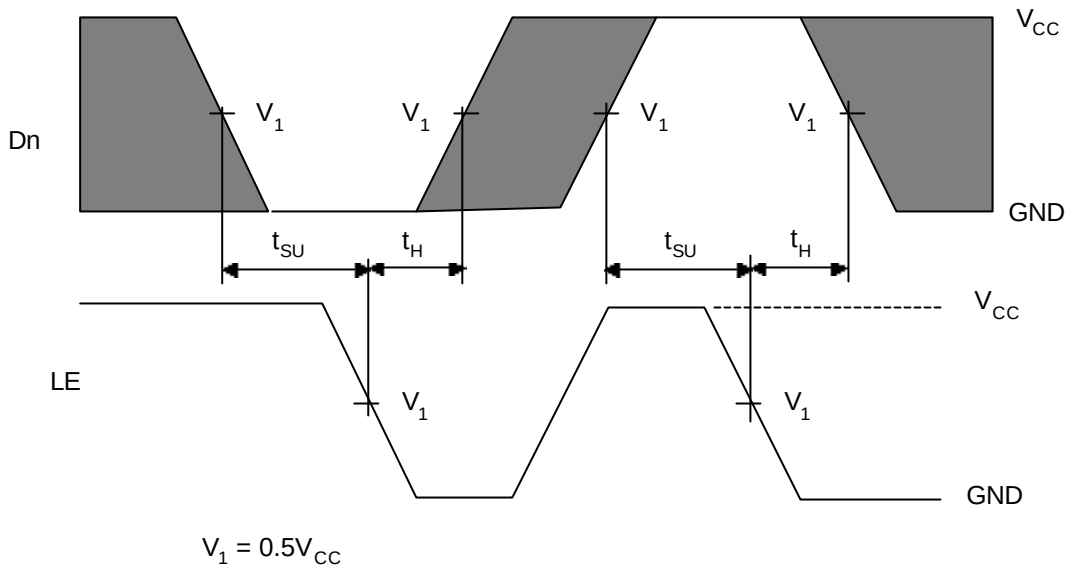


Figure 3 - Time diagram

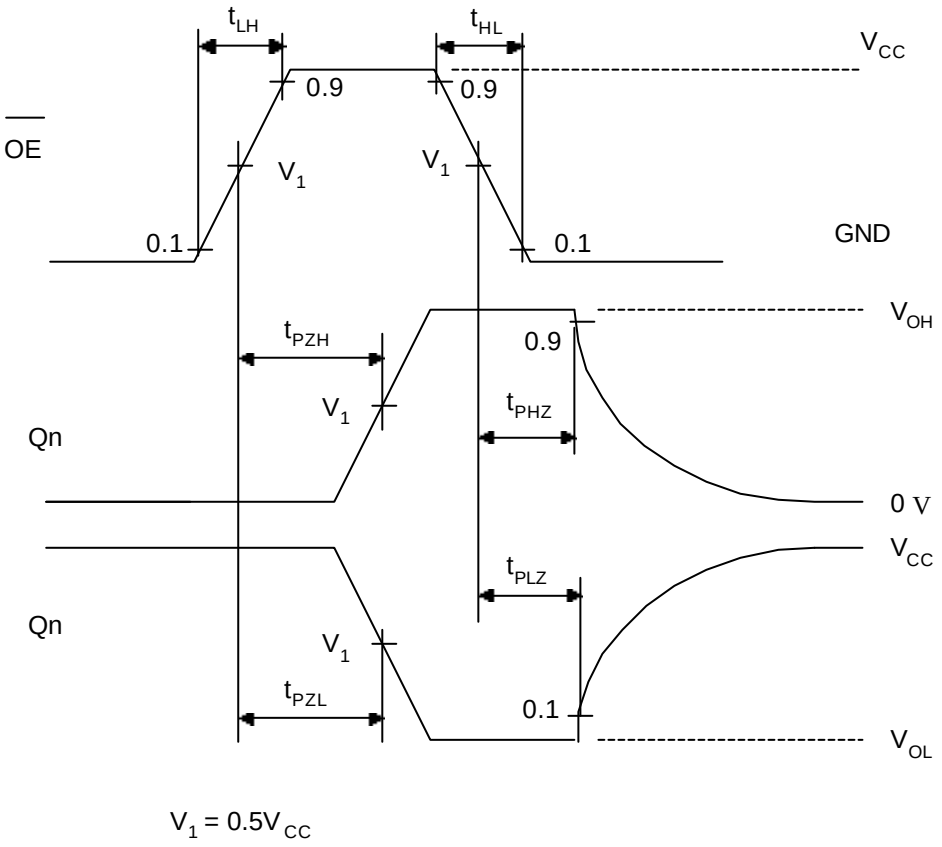
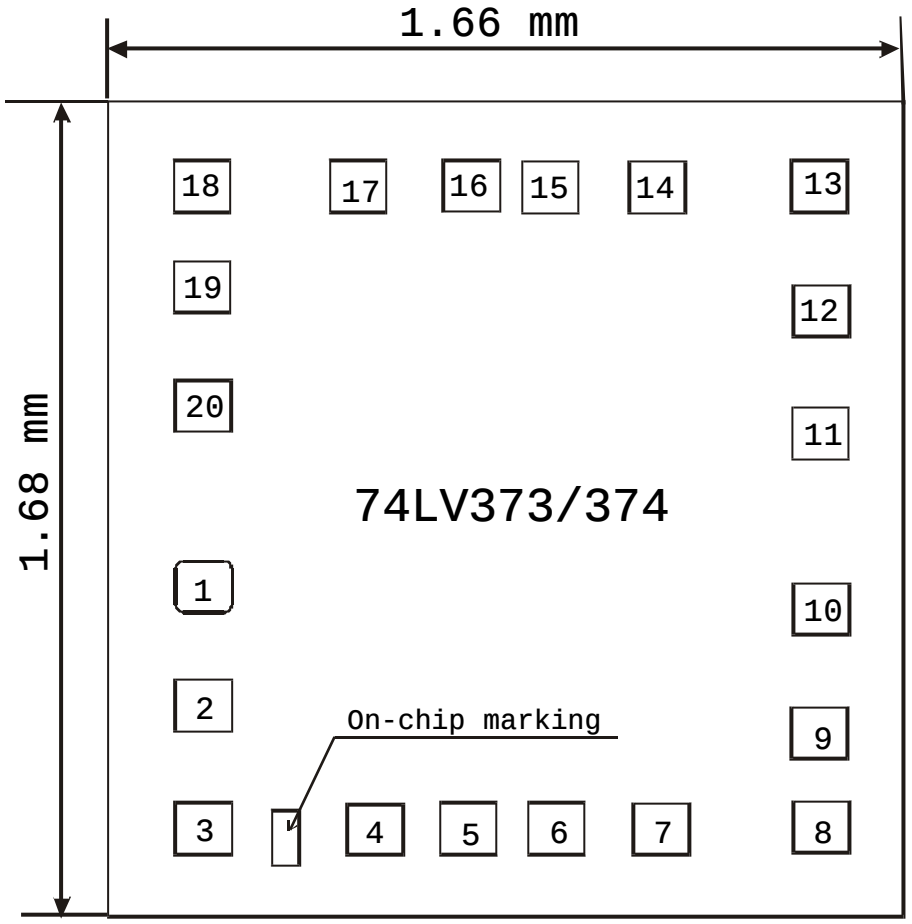


Figure 4 -Time diagram



Drawing of the chip

Pads allocation Table

Pad number	coordinates (counted from lower left corner), mm		Pad size, mm
	X	Y	
01	0.142	0.628	0.108 x 0.108
02	0.142	0.377	0.108 x 0.108
03	0.142	0.125	0.108 x 0.108
04	0.498	0.125	0.108 x 0.108
05	0.693	0.125	0.108 x 0.108
06	0.871	0.125	0.108 x 0.108
07	1.095	0.125	0.108 x 0.108
08	1.423	0.130	0.108 x 0.108
09	1.423	0.329	0.108 x 0.108
10	1.423	0.587	0.108 x 0.108
11	1.423	0.949	0.108 x 0.108
12	1.423	1.198	0.108 x 0.108
13	1.423	1.447	0.108 x 0.108
14	1.085	1.447	0.108 x 0.108
15	0.868	1.447	0.108 x 0.108
16	0.696	1.447	0.108 x 0.108
17	0.461	1.447	0.108 x 0.108
18	0.142	1.447	0.108 x 0.108

19	0.142	1.245	0.108 x 0.108
20	0.142	0.997	0.108 x 0.108