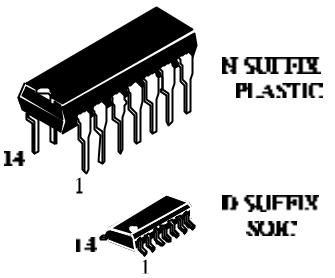
Dual D Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS



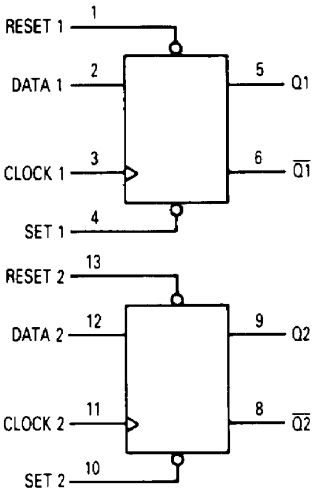
ORDERING INFORMATION
SL74HCT74N Plastic
SL74HCT74D SOIC
T_A = -55° to 125° C for all packages

The SL74HCT74 is identical in pinout to the LS/ALS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

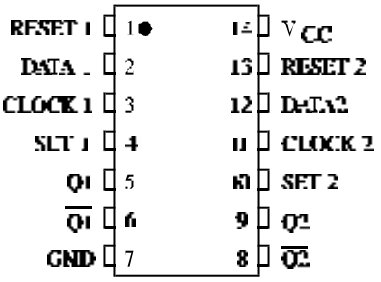
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA

LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	¬	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond whitch damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5	0.26	0.33	0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	5.5	1.0	10	40	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{IN}=2.4 V, Any One Input V_{IN}=V_{CC} or GND, Other Inputs		≥-55°C		25°C to 125°C	mA
		I_{OUT}=0μA	5.5	2.9		2.4	

AC ELECTRICAL CHARACTERISTICS (V_{CC} =5.0 V±10%,C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	24	30	36	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 130	pF

TIMING REQUIREMENTS (V_{CC} =5.0 V±10%,C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to-55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	15	19	22	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	3	3	3	ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	6	8	9	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	15	19	22	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	15	19	22	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

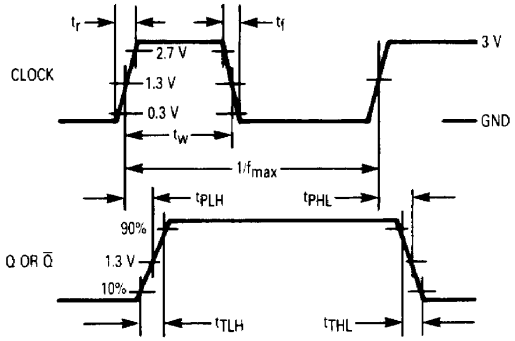


Figure 1. Switching Waveforms

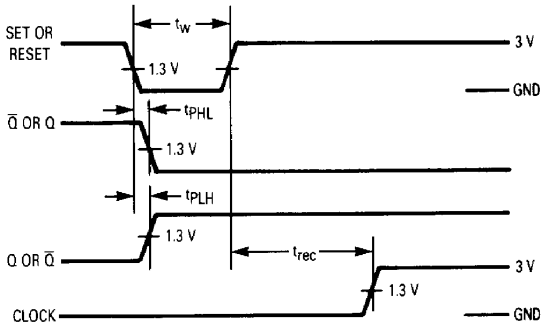


Figure 2. Switching Waveforms

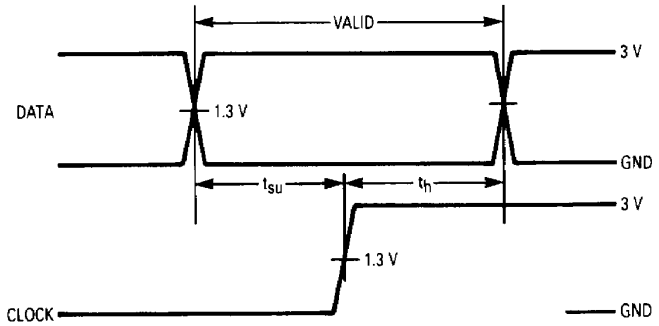


Figure 3. Switching Waveforms

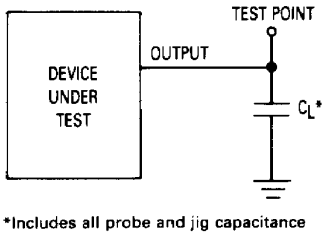


Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM