

OCTAL D-TYPE FLIP-FLOP WITH DATA ENABLE; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See "273" for master reset version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable (\bar{E}) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop. The \bar{E} input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	13	14	ns
f_{max}	maximum clock frequency		77	53	MHz
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; $T_{amb} = 25 \text{ }^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

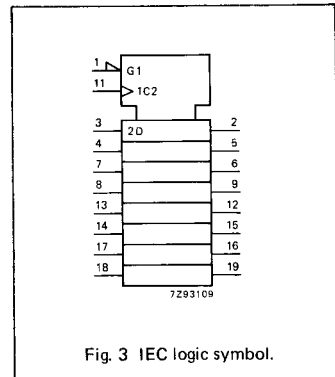
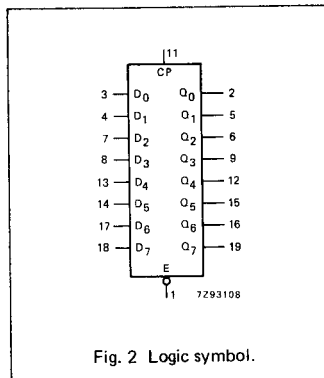
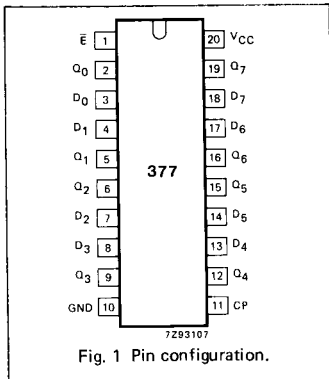
$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz
 f_o = output frequency in MHz
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in V
2. For HC the condition is $V_I = \text{GND to } V_{CC}$
 For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

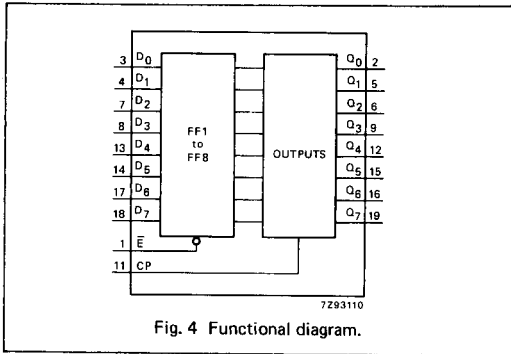
PACKAGE OUTLINES

- 20-lead DIL; plastic (SOT146).
- 20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\bar{E}	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

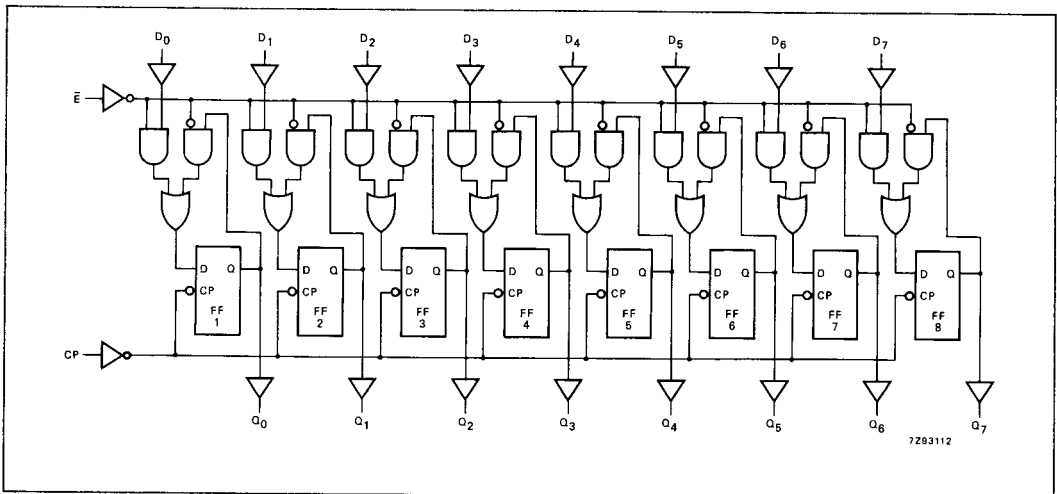




FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	CP	\bar{E}	D_n	Q_n
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑ X	h H	X X	no change no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V_{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ t_{PLH}	propagation delay CP to Q_n		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
$t_{THL}/$ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_{su}	set-up time D_n to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time \bar{E} to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time D_n to CP	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time \bar{E} to CP	4 4 4	-3 -1 -1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6 30 35	23 70 83		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E	1.50
CP	0.50
D _n	0.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		17	32		40		48	ns	4.5	Fig. 6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t _W	clock pulse width HIGH or LOW	20	8		25		30		ns	4.5	Fig. 6
t _{su}	set-up time D _n to CP	12	4		15		18		ns	4.5	Fig. 7
t _{su}	set-up time E to CP	22	12		28		33		ns	4.5	Fig. 7
t _h	hold time D _n to CP	2	-4		2		2		ns	4.5	Fig. 7
t _h	hold time E to CP	3	-2		3		3		ns	4.5	Fig. 7
f _{max}	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

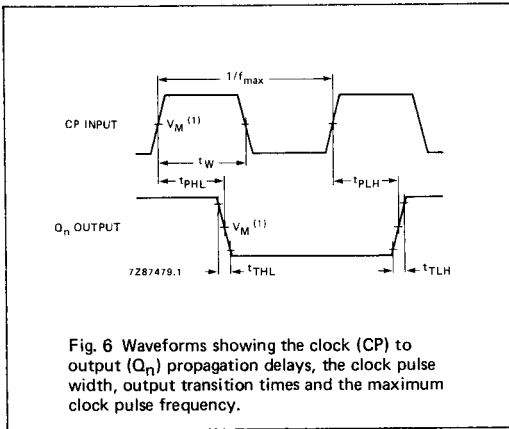


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

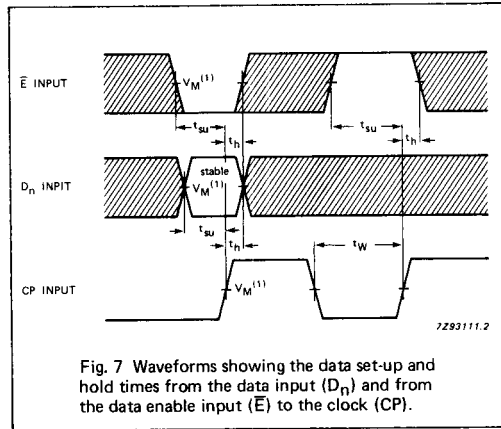


Fig. 7 Waveforms showing the data set-up and hold times from the data input (D_n) and from the data enable input (\bar{E}) to the clock (CP).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.