

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT40104

4-bit bidirectional universal shift register; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

4-bit bidirectional universal shift register; 3-state

74HC/HCT40104

FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the "40104" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized systems.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP to Q _n	C _L = 15 pF; V _{CC} = 5 V	13	15	ns
f _{max}	maximum clock frequency		62	57	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	75	75	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

In the parallel-load mode (S₀ and S₁ are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (D_{SR}) and shift-left (D_{SL}) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (S₀ and S₁) LOW and clocking the register. When the output enable input (OE) is LOW, all outputs assume the high-impedance OFF-state (Z).

APPLICATIONS

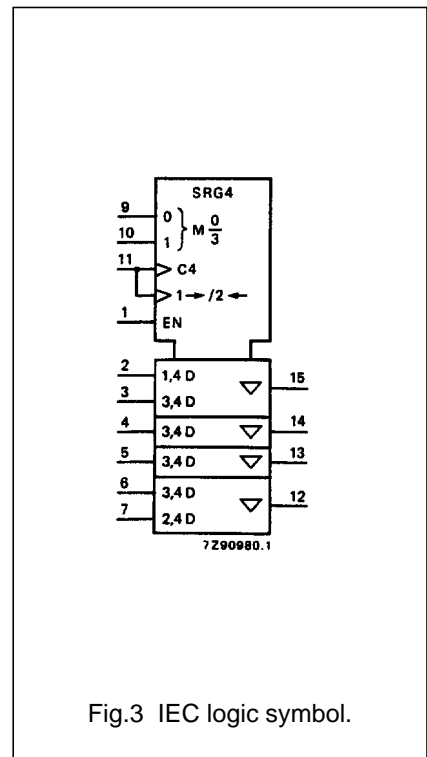
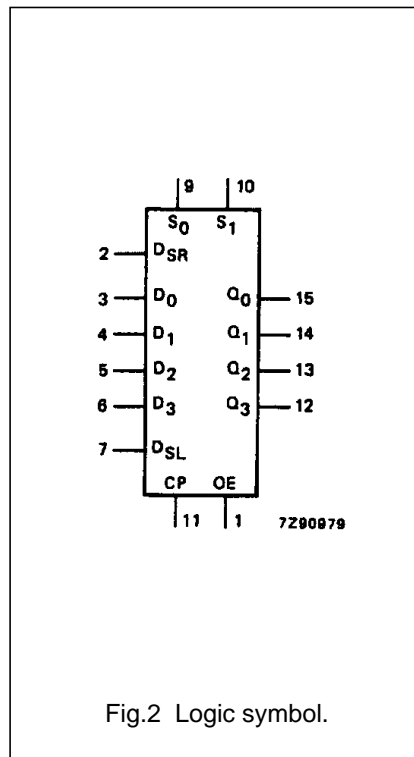
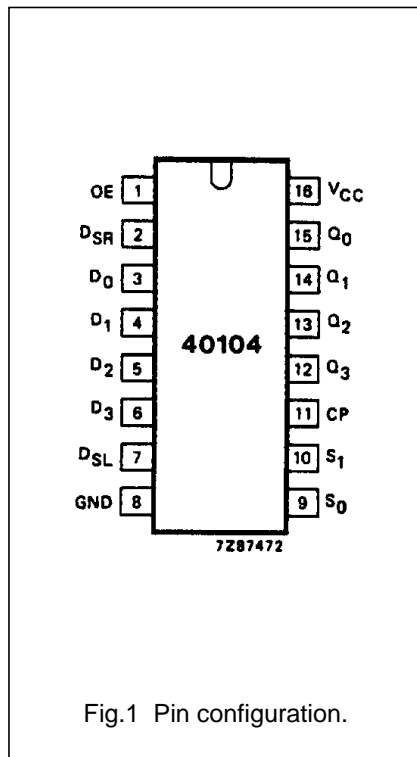
- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

4-bit bidirectional universal shift register;
3-state

74HC/HCT40104

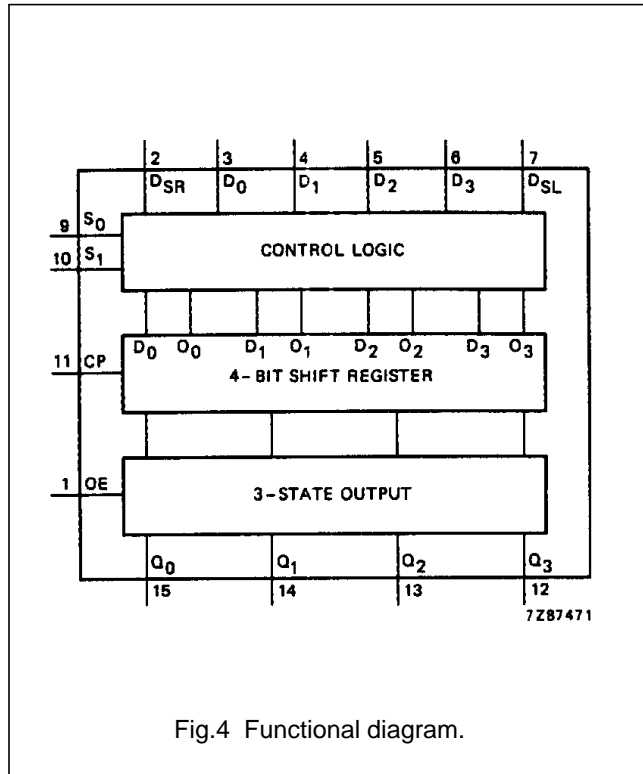
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active HIGH)
2	D _{SR}	serial data shift-right input
3, 4, 5, 6	D ₀ to D ₃	parallel data inputs
7	D _{SL}	serial data shift-left input
8	GND	ground (0 V)
9, 10	S ₀ , S ₁	mode control inputs
11	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 14, 13, 12	Q ₀ to Q ₃	3-state parallel outputs
16	V _{CC}	positive supply voltage



4-bit bidirectional universal shift register;
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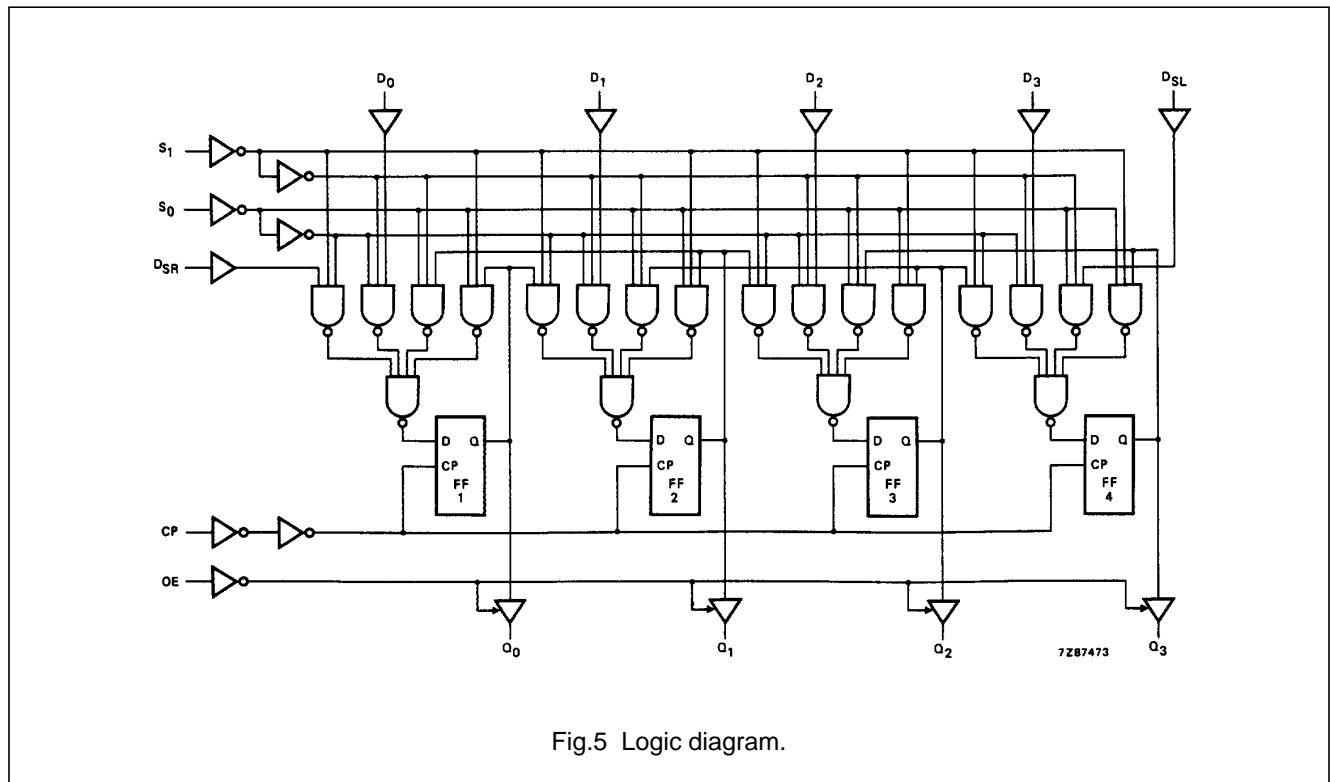


FUNCTION TABLE

OPERATING MODES	INPUTS (OE = HIGH)					OUTPUTS at t_{n+1}			
	S ₁	S ₀	D _{SR}	D _{SL}	D ₀ to D ₃	Q ₀	Q ₁	Q ₂	Q ₃
reset	L	L	X	X	X	L	L	L	L
shift left	H	L	X	L	X	Q ₁	Q ₂	Q ₃	L
	H	L	X	H	X	Q ₁	Q ₂	Q ₃	H
shift right	L	H	L	X	X	L	Q ₀	Q ₁	Q ₂
	L	H	H	X	X	H	Q ₀	Q ₁	Q ₂
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care
 t_{n+1} = state after next LOW-to-HIGH transition of CP



4-bit bidirectional universal shift register; 3-state

74HC/HCT40104

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		44 16 13	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _n		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Q _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t _W	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t _{SU}	set-up time D _n , D _{SR} , D _{SL} to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _{SU}	set-up time S ₀ , S ₁ to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _H	hold time D _n , D _{SR} , D _{SL} to CP	2 2 2	-8 -3 -2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
t _H	hold time S ₀ , S ₁ to CP	2 2 2	-14 -5 -4		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
f _{max}	maximum clock pulse frequency	6.0 30 35	19 56 67		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

4-bit bidirectional universal shift register; 3-state

74HC/HCT40104

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D ₀ to D ₃	0.35
D _{SR} , D _{SL}	0.35
CP	0.35
S ₀ , S ₁	0.70
OE	1.40

AC CHARACTERISTICS FOR 74HCT

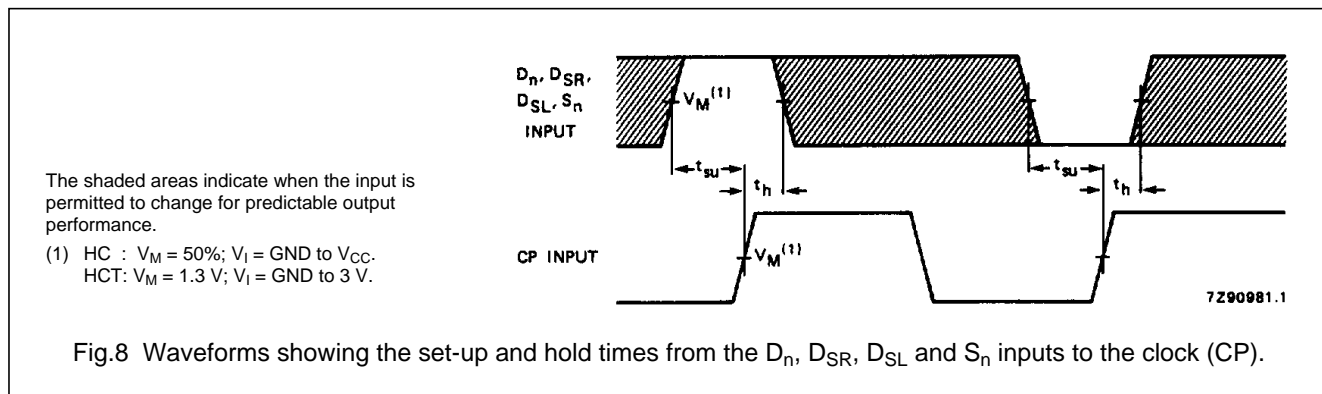
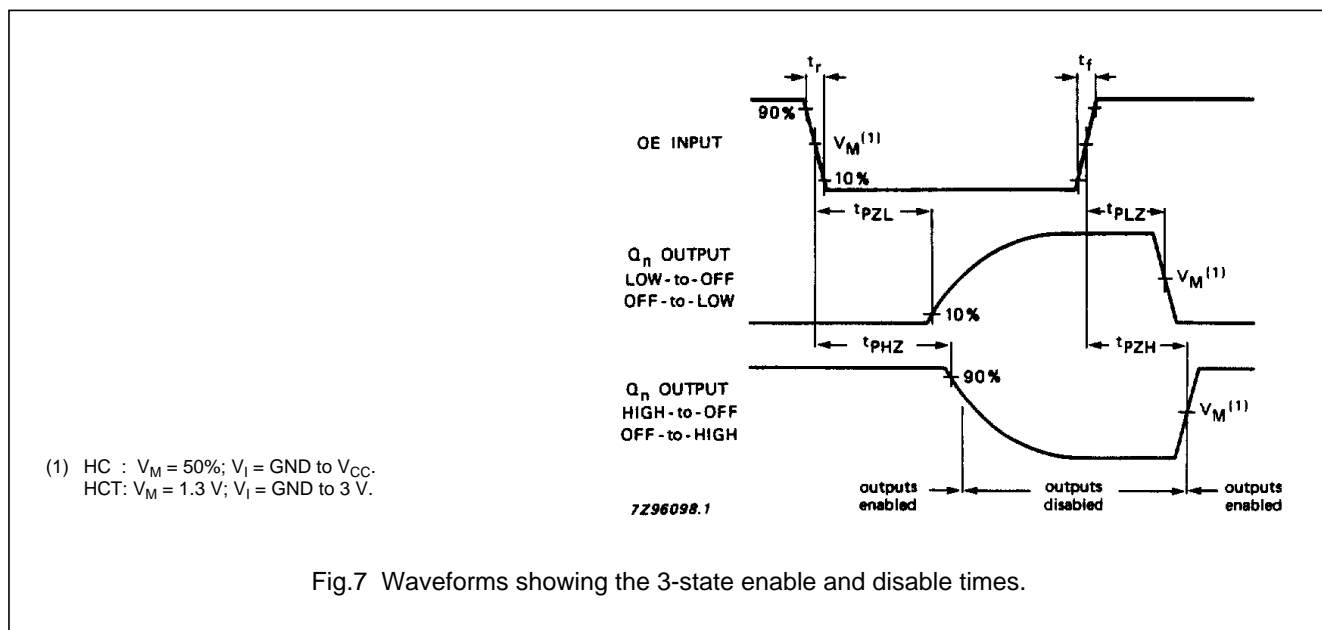
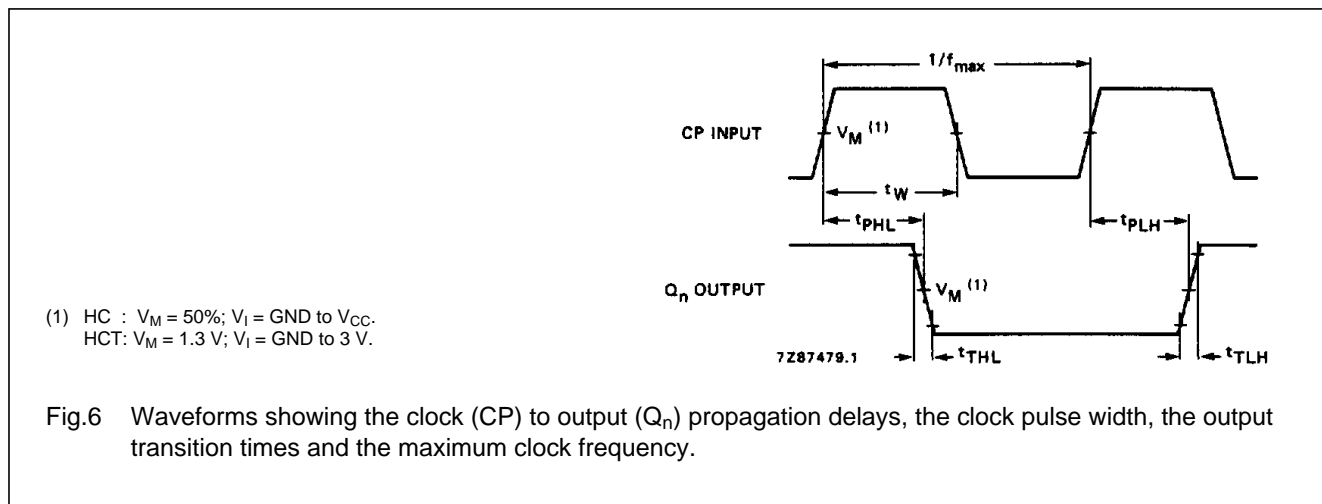
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		18	34		43		51	ns	4.5	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _n		12	30		38		45	ns	4.5	Fig.8
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Q _n		21	35		44		53	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t _W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.6
t _{SU}	set-up time D _n , D _{SR} , D _{SL} to CP	16	8		20		24		ns	4.5	Fig.8
t _{SU}	set-up time S ₀ , S ₁ to CP	20	9		25		30		ns	4.5	Fig.8
t _H	hold time D _n , D _{SR} , D _{SL} to CP	2	-2		2		2		ns	4.5	Fig.8
t _H	hold time S ₀ , S ₁ to CP	2	-5		2		2		ns	4.5	Fig.8
f _{max}	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig.6

4-bit bidirectional universal shift register;
3-state

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AC WAVEFORMS



4-bit bidirectional universal shift register;
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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.