INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT283 4-bit binary full adder with fast carry

Product specification
File under Integrated Circuits, IC06

December 1990





74HC/HCT283

FEATURES

· High-speed 4-bit binary addition

· Cascadable in 4-bit increments

· Fast internal look-ahead carry

· Output capability: standard

• I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 to Σ_4) and the out-going carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + +4(A_3 + B_3) + 8(A_4 + B_4) =$$

= $\sum_1 + 2\sum_2 + 4\sum_3 + 8\sum_4 + 16C_{OUT}$

Where (+) = plus.

Due to the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ_1 to Σ_4 and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus $C_{\text{IN}},\,A_1,\,B_1$ can be assigned arbitrarily to pins 5, 6, 7, etc.

See the "583" for the BCD version.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

CVMDOL	DADAMETED	CONDITIONS	TYP		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} / t _{PLH}	propagation delay	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$			
	C_{IN} to Σ_1		16	15	ns
	C_IN to Σ_2		18	21	ns
	C_{IN} to Σ_3		20	23	ns
	C_{IN} to Σ_4		23	27	ns
	A_n or B_n to Σ_n		21	25	ns
	C _{IN} to C _{OUT}		20	23	ns
	A _n or B _n to C _{OUT}		20	24	ns
Cı	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	88	92	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz

f_o = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

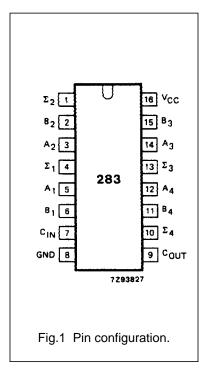
74HC/HCT283

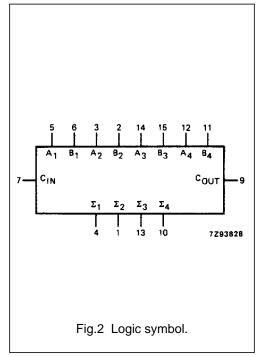
ORDERING INFORMATION

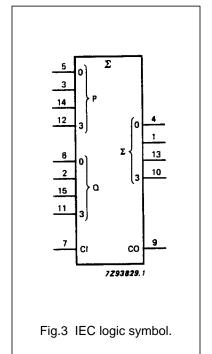
See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ_1 to Σ_4	sum outputs
5, 3, 14, 12	A ₁ to A ₄	A operand inputs
6, 2, 15, 11	B ₁ to B ₄	B operand inputs
7	C _{IN}	carry input
8	GND	ground (0 V)
9	C _{OUT}	carry output
16	V _{CC}	positive supply voltage



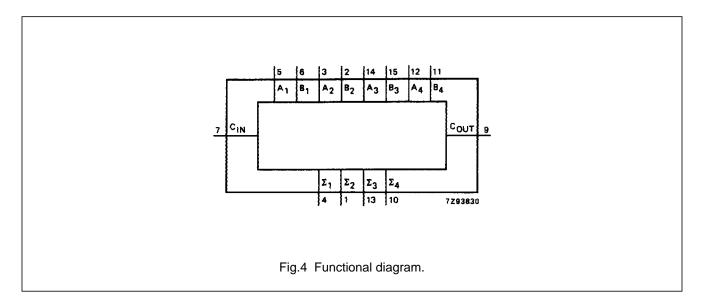




Philips Semiconductors Product specification

4-bit binary full adder with fast carry

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FUNCTION TABLE

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ_1	Σ_2	Σ_3	Σ_4	C _{OUT}	EXAMPLE ⁽²⁾
logic levels	L	L	Н	L	Н	Н	L	L	Н	Н	Н	L	L	Н	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(3)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(4)

Note

H = HIGH voltage level
 L = LOW voltage level

2. example

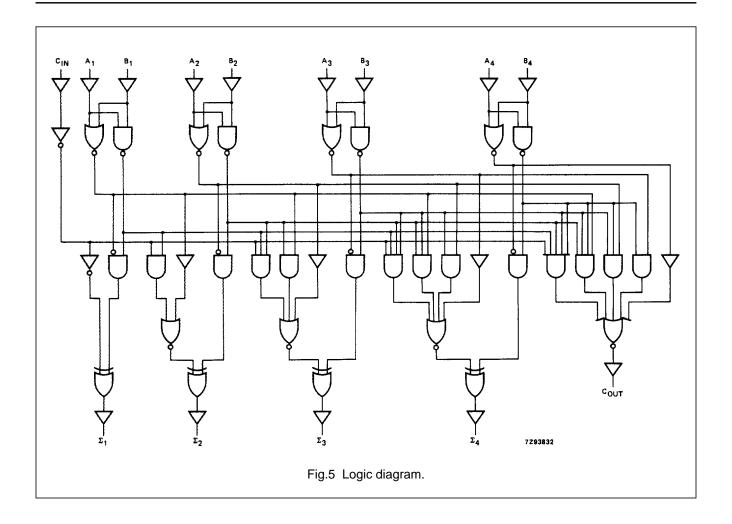
1001

1010

10011

- 3. for active HIGH, example = (9 + 10 = 19)
- 4. for active LOW, example = (carry + 6 + 5 = 12)

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

					T _{amb} (TEST CONDITIONS				
SYMBOL					74H0						
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(*)	
t _{PHL} / t _{PLH}	propagation delay		52	160		200		240	ns	2.0	Fig.6
	C_{IN} to Σ_1		19 15	32 27		40 34		48 41		4.5 6.0	
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_2		58 21	180 36		225 45		270 54	ns	2.0 4.5	Fig.6
			17	31		38		46		6.0	
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_3		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_4		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay A_n or B_n to Σ_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to C _{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay A _n or B _n to C _{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

Philips Semiconductors Product specification

4-bit binary full adder with fast carry

74HC/HCT283

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
C _{IN}	1.50
B ₂ , A ₂ , A ₁	1.00
B ₁	0.40
B ₄ , A ₄ , A ₃ , B ₃	0.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL		T _{amb} (°C)								TES	TEST CONDITIONS	
		74HCT									WAVEEGRAG	
	PARAMETER	+25			-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(•)		
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_1		18	31		39		47	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_2		25	43		54		65	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_3		27	46		58		69	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay C_{IN} to Σ_4		31	53		66		80	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	$\begin{array}{c} \text{propagation delay} \\ A_n \text{ or } B_n \text{ to } \Sigma_n \end{array}$		29	49		61		74	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay C _{IN} to C _{OUT}		27	46		58		69	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay A _n or B _n to C _{OUT}		28	48		60		72	ns	4.5	Fig.6	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6	

74HC/HCT283

AC WAVEFORMS

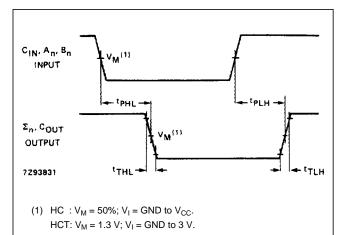
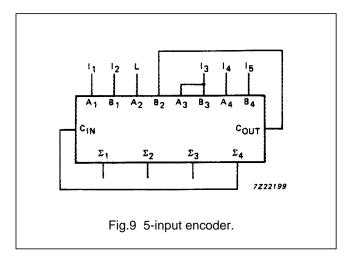


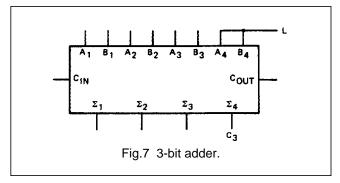
Fig.6 Waveforms showing the inputs (C_{IN} , A_n , B_n) to the outputs (Σ_n , C_{OUT}) propagation delays and the output transition times.

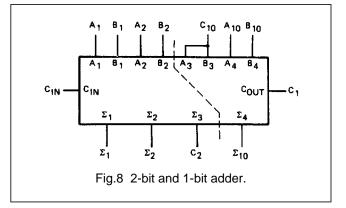


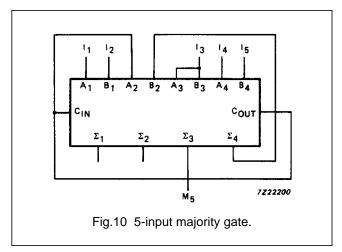
Notes to Figs 7 to 10

Figure 7 shows a 3-bit adder using the "283". Tying the operand inputs of the fourth adder (A3, B3) LOW makes Σ_3 dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the "283" into a 2-bit and 1-bit adder. The third stage adder (A2, B2, Σ_2) is used simply as means of transferring the carry into the fourth stage (via A2 and B2) and transferring the carry from the second stage on Σ_2 . Note that as long as long as A2 and B2 are the same, HIGH or LOW, they do not influence Σ_2 . Similarly, when A2 and B2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the

APPLICATION INFORMATION







inputs are equally weighted. The outputs Σ 0, Σ 1 and Σ 2 produce a binary number equal to the number inputs (I₁ to I₅) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I₁ to I₅) are HIGH, the output M₅ is HIGH.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".