74HC158

Quad 2-input multiplexer; inverting

Rev. 4 — 23 December 2015 Product data sheet

1. General description

The 74HC158 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC158 is specified in compliance with JEDEC standard no. 7A.

The 74HC158 is a quad 2-input multiplexer which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input ($\overline{E}$) is active LOW.

When $\overline{E}$ is HIGH, all the outputs ($1\overline{Y}$ to $4\overline{Y}$) are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the 74HC158. The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The 74HC158 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

$1\overline{Y} = \overline{E}.(1I1.S + 1I0.\overline{S})$

$2\overline{Y} = \overline{E}.(2I1.S + 2I0.\overline{S})$

$3\overline{Y} = \overline{E}.(3I1.S + 3I0.\overline{S})$

$4\overline{Y} = \overline{E}.(4I1.S + 4I0.\overline{S})$

The 74HC158 is identical to the 74HC157 but has inverting outputs.

2. Features and benefits

- Low-power dissipation
- Inverting data path
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40° C to +85 °C and –40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC158D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

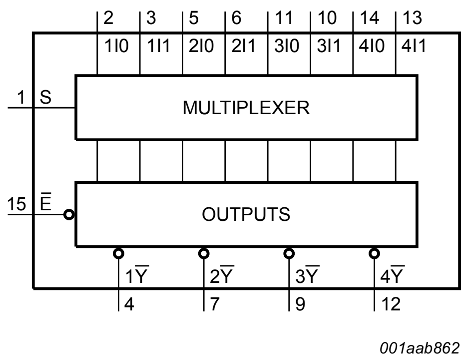


Fig 1. Functional diagram

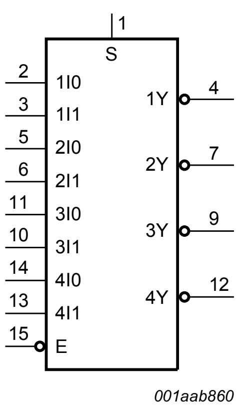


Fig 2. Logic symbol

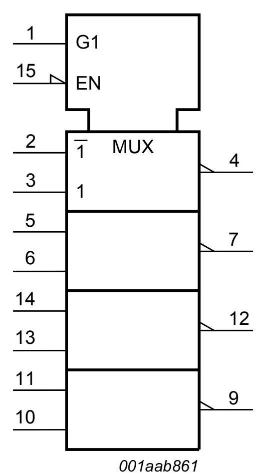


Fig 3. IEC logic symbol

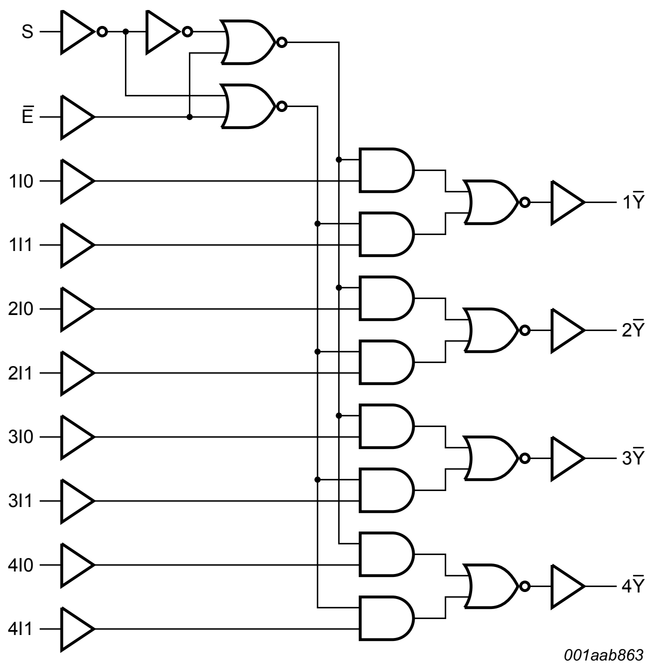


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

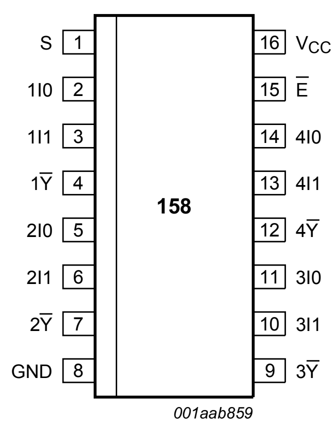


Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0	2	data input 1 from source 0
1I1	3	data input 1 from source 1
1$\overline{Y}$	4	multiplexer output 1
2I0	5	data input 2 from source 0
2I1	6	data input 2 from source 1
2$\overline{Y}$	7	multiplexer output 2
GND	8	ground (0 V)
3$\overline{Y}$	9	multiplexer output 3
3I1	10	data input 3 from source 1
3I0	11	data input 3 from source 0
4$\overline{Y}$	12	multiplexer output 4
4I1	13	data input 4 from source 1
4I0	14	data input 4 from source 0
$\overline{E}$	15	enable input (active LOW)
V_{CC}	16	positive supply voltage

6. Functional description

6.1 Function table

Table 3. Function[1]

Control		Input		Output
$\overline{E}$	**S**	**nI0**	**nI1**	**n$\overline{Y}$**
H	X	X	X	H
L	L	L	X	H
		H	X	L
	H	X	L	H
		X	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C			
		SO16 package [1]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 6. Static characteristics *…continued*
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0\ V$	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5\ V$	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0\ V$	-	-	0.1	V
		$I_O = 4\ mA$; $V_{CC} = 4.5\ V$	-	-	0.33	V
		$I_O = 5.2\ mA$; $V_{CC} = 6.0\ V$	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\ V$	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 6.0\ V$	-	-	80	μA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\ V$	1.5	-	-	V
		$V_{CC} = 4.5\ V$	3.15	-	-	V
		$V_{CC} = 6.0\ V$	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\ V$	-	-	0.5	V
		$V_{CC} = 4.5\ V$	-	-	1.35	V
		$V_{CC} = 6.0\ V$	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\ \mu A$; $V_{CC} = 2.0\ V$	1.9	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 4.5\ V$	4.4	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 6.0\ V$	5.9	-	-	V
		$I_O = -4\ mA$; $V_{CC} = 4.5\ V$	3.7	-	-	V
		$I_O = -5.2\ mA$; $V_{CC} = 6.0\ V$	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0\ V$	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5\ V$	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0\ V$	-	-	0.1	V
		$I_O = 4\ mA$; $V_{CC} = 4.5\ V$	-	-	0.4	V
		$I_O = 5.2\ mA$; $V_{CC} = 6.0\ V$	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\ V$	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 6.0\ V$	-	-	160	μA

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; for test circuit see Figure 8.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{pd}	propagation delay	nI0, nI1 to $n\overline{Y}$; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	41	125	ns
		V_{CC} = 4.5 V		-	15	25	ns
		V_{CC} = 6.0 V		-	12	21	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	12	-	ns
		$\overline{E}$ to $n\overline{Y}$; see Figure 7	[1]				
		V_{CC} = 2.0 V		-	47	145	ns
		V_{CC} = 4.5 V		-	17	29	ns
		V_{CC} = 6.0 V		-	14	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	14	-	ns
		S to $n\overline{Y}$; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	47	145	ns
		V_{CC} = 4.5 V		-	17	29	ns
		V_{CC} = 6.0 V		-	14	25	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	14	-	ns
t_t	transition time	see Figure 6 and 7	[2]				
		V_{CC} = 2.0 V		-	19	75	ns
		V_{CC} = 4.5 V		-	7	15	ns
		V_{CC} = 6.0 V		-	6	13	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC}	[3]	-	40	-	pF
T_{amb} = −40 °C to +85 °C							
t_{pd}	propagation delay	nI0, nI1 to $n\overline{Y}$; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	-	155	ns
		V_{CC} = 4.5 V		-	-	31	ns
		V_{CC} = 6.0 V		-	-	26	ns
		$\overline{E}$ to $n\overline{Y}$; see Figure 7	[1]				
		V_{CC} = 2.0 V		-	-	180	ns
		V_{CC} = 4.5 V		-	-	36	ns
		V_{CC} = 6.0 V		-	-	31	ns
		S to $n\overline{Y}$; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	-	180	ns
		V_{CC} = 4.5 V		-	-	36	ns
		V_{CC} = 6.0 V		-	-	31	ns
t_t	transition time	see Figure 6 and 7	[2]				
		V_{CC} = 2.0 V		-	-	95	ns
		V_{CC} = 4.5 V		-	-	19	ns
		V_{CC} = 6.0 V		-	-	16	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
t_{pd}	propagation delay	nI0, nI1 to $n\overline{Y}$; see Figure 6 [1]				
		V_{CC} = 2.0 V	-	-	190	ns
		V_{CC} = 4.5 V	-	-	38	ns
		V_{CC} = 6.0 V	-	-	32	ns
		$\overline{E}$ to $n\overline{Y}$; see Figure 7 [1]				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	38	ns
		S to $n\overline{Y}$; see Figure 6 [1]				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	38	ns
t_t	transition time	see Figure 6 and 7 [2]				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

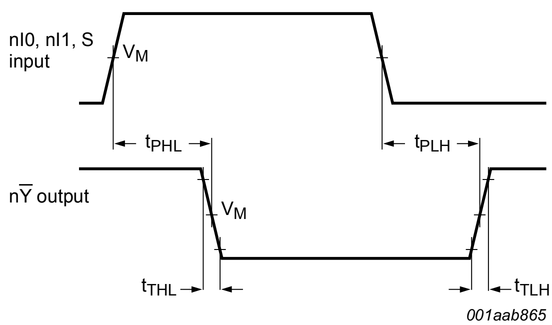
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

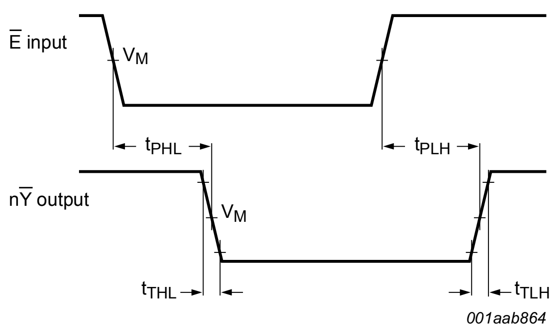
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



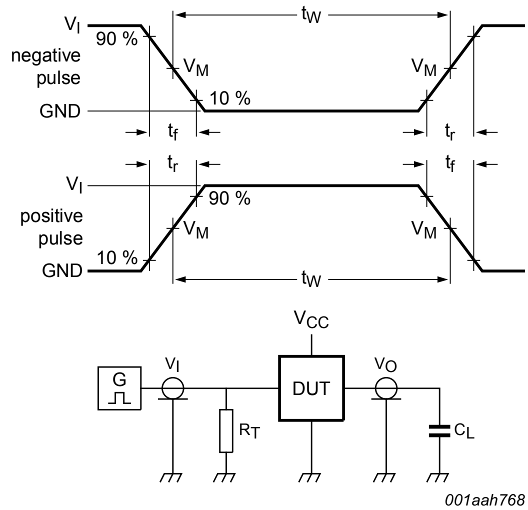
$V_M = 0.5V_{CC}$.

Fig 6. Waveforms showing the data input (nI0, nI1) to output ($n\overline{Y}$) propagation delays and the output transition times



$V_M = 0.5V_{CC}$.

Fig 7. Waveforms showing the enable input ($\overline{E}$) to output ($n\overline{Y}$) propagation delays and the output transition times



Test data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

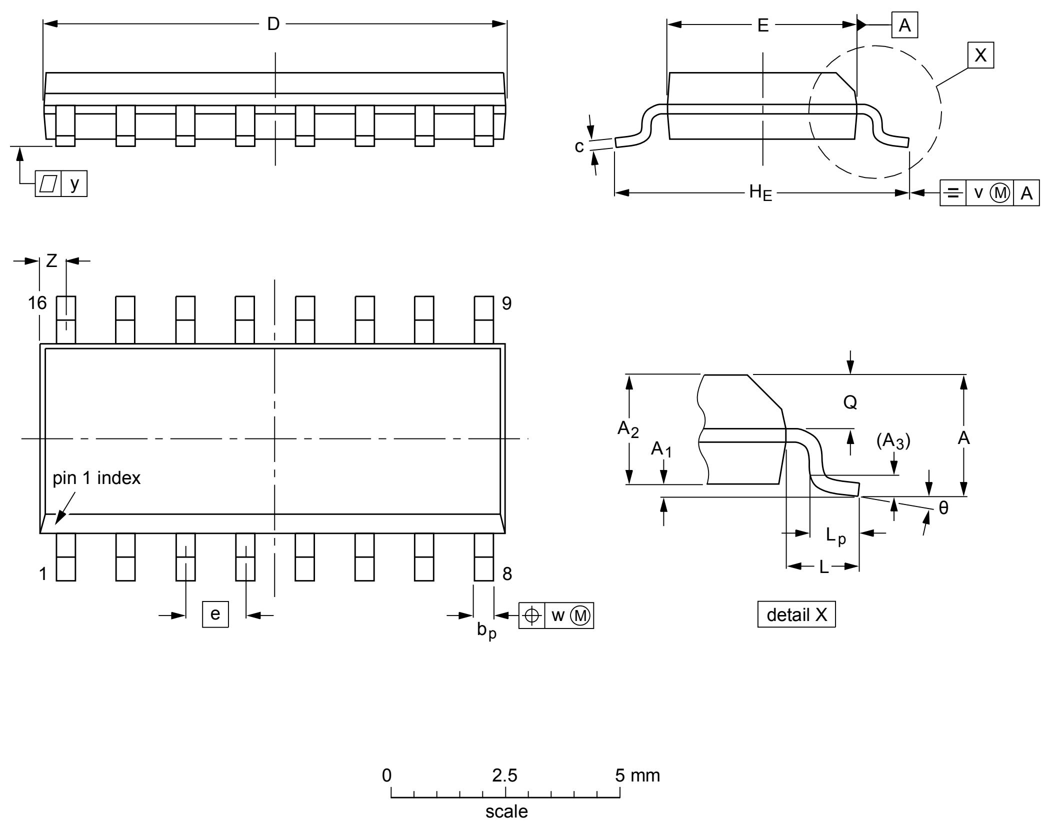
Fig 8. Test circuit for measuring switching times

Table 8. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC158	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC158 v.4	20151223	Product data sheet	-	74HC158 v.3
Modifications:	• Type number 74HC158N (SOT38-4) removed.			
74HC158 v.3	20041112	Product data sheet	-	74HC_HCT158_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT158. • Inserted family specification.			
74HC_HCT158_CNV v.2	19970827	Product specification	-	74HC_HCT158 v.1
74HC_HCT158 v.1	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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