

# DATA SHEET

**74F640**

Octal bus transceiver, inverting (3-State)

Product specification

1989 Nov 27

IC15 Data Handbook

## Octal bus transceiver, inverting (3-State)

74F640

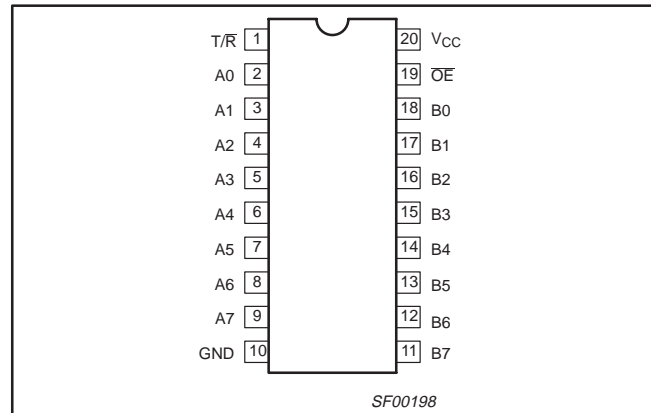
## FEATURES

- High-impedance NPN base inputs for reduced loading (70 $\mu$ A in High and Low states)
- Ideal for applications which require high-output drive and minimal bus loading
- Inverting version of 74F245
- Octal bidirectional bus interface
- 3-State outputs sink 64mA and source 15mA

## DESCRIPTION

The 74F640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics. The device features an Output Enable ( $\overline{OE}$ ) input for easy cascading and Transmit/Receiver ( $T/\overline{R}$ ) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
20-pin plastic DIP	N74F640N	SOT146-1
20-pin plastic SOL	N74F640D	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

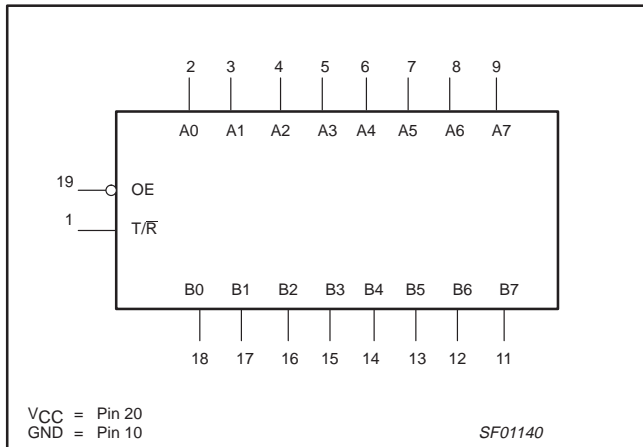
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	3.5/0.115	70 $\mu$ A/70 $\mu$ A
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40 $\mu$ A/40 $\mu$ A
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40 $\mu$ A/40 $\mu$ A
A0 - A7	A port outputs	150/40	3.0mA/24mA
B0 - B7	B port outputs	750/106.7	15mA/64mA

**NOTE:** One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

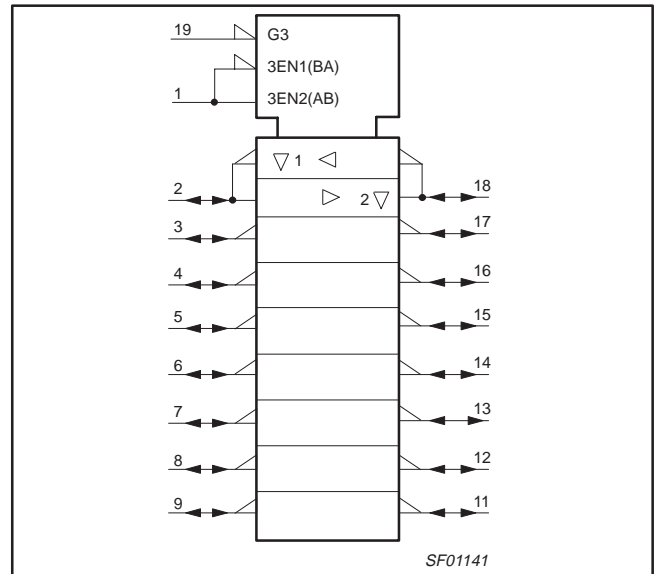
# Octal bus transceiver, inverting (3-State)

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## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

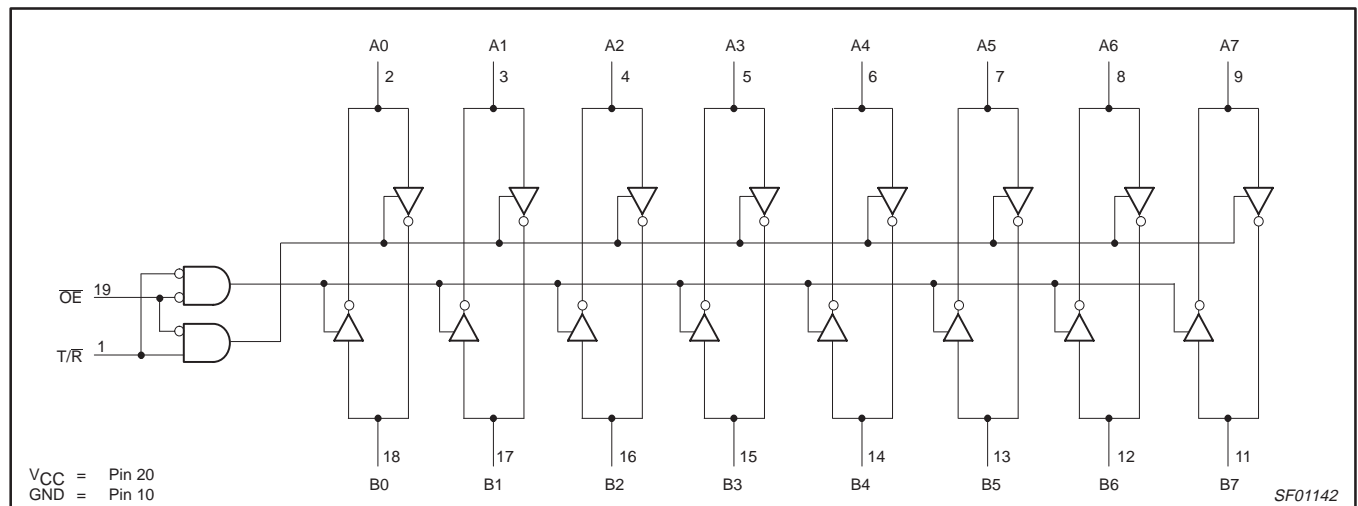


## FUNCTION TABLE

INPUTS		OUTPUTS
OE	T/R	
L	L	Bus B data to Bus $\bar{A}$
L	H	Bus A data to Bus $\bar{B}$
H	X	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High impedance "off" state

## LOGIC DIAGRAM



## Octal bus transceiver, inverting (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage		-0.5 to +7.0	V
I <sub>IN</sub>	Input current		-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state		-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	A0-A7	48	mA
		B0-B7	128	mA
T <sub>amb</sub>	Operating free-air temperature range		0 to +70	°C
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current	A0-A7		-3	mA
		B0-B7		-15	mA
I <sub>OL</sub>	Low-level output current	A0-A7		24	mA
		B0-B7		64	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

## Octal bus transceiver, inverting (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>NO TAG</sup>			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V <sub>OH</sub>	High-level output voltage	A0–A7	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = –3mA	±10%V <sub>CC</sub>	2.4			V
		B0–B7			±5%V <sub>CC</sub>	2.7	3.3		V
		B0–B7		I <sub>OH</sub> = –15mA	±10%V <sub>CC</sub>	2.0			V
					±5%V <sub>CC</sub>	2.0			V
V <sub>OL</sub>	Low-level output voltage	A0–A7	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN,	I <sub>OL</sub> = 24mA	±10%V <sub>CC</sub>		0.35	0.50	V
		B0–B7			±5%V <sub>CC</sub>		0.35	0.50	V
		B0–B7		I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>			0.55	V
					±5%V <sub>CC</sub>		0.42	0.55	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			–0.73	–1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	$\overline{OE}$ , T/R	V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V				100	μA	
		A0–A7, B0–B7	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 5.5V				1.0	mA	
I <sub>IH</sub>	High-level input current	$\overline{OE}$ , T/R	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				40	μA	
I <sub>IL</sub>	Low-level input current	only	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				–40	μA	
I <sub>OZH</sub> +I <sub>IH</sub>	Off-state output current, High level of voltage applied		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				70	μA	
I <sub>OZL</sub> +I <sub>IL</sub>	Off-state output current, Low level of voltage applied		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				–70	μA	
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>	A0–A7	V <sub>CC</sub> = MAX		–60		–150	mA	
		B0–B7			–100		–225	μA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX	T/R = A <sub>n</sub> = 4.5V, $\overline{OE}$ = GND		66	85	mA	
		I <sub>CCL</sub>		T/R = B <sub>n</sub> = $\overline{OE}$ = GND		91	120	mA	
		I <sub>CCZ</sub>		T/R = B <sub>n</sub> = GND, $\overline{OE}$ = 4.5V		78	102	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

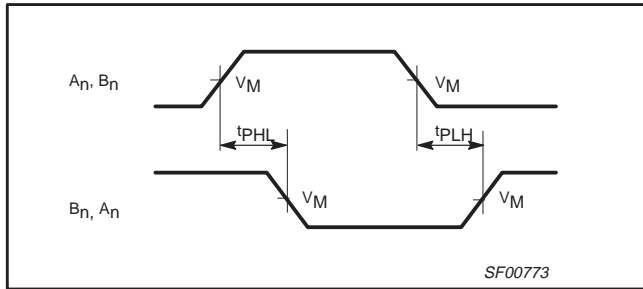
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to Bn, Bn to An	Waveform NO TAG	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 3 Waveform 2	5.5 5.5	6.5 7.0	10.5 10.5	5.0 5.0	12.0 11.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level	Waveform 3 Waveform 2	2.0 2.0	3.5 4.5	6.5 7.0	1.5 2.0	8.0 7.5	ns

# Octal bus transceiver, inverting (3-State)

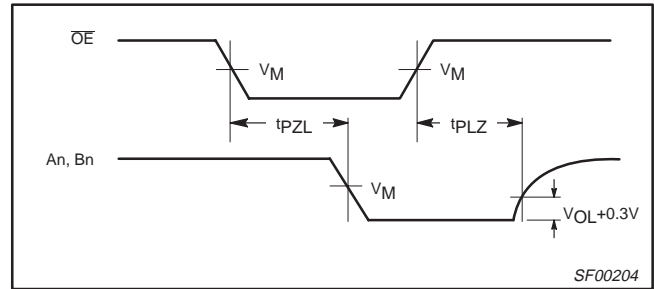
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## AC WAVEFORMS

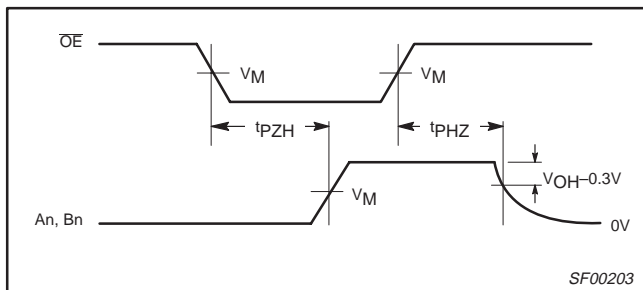
For all waveforms,  $V_M = 1.5V$ .



Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Open Collector Outputs**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

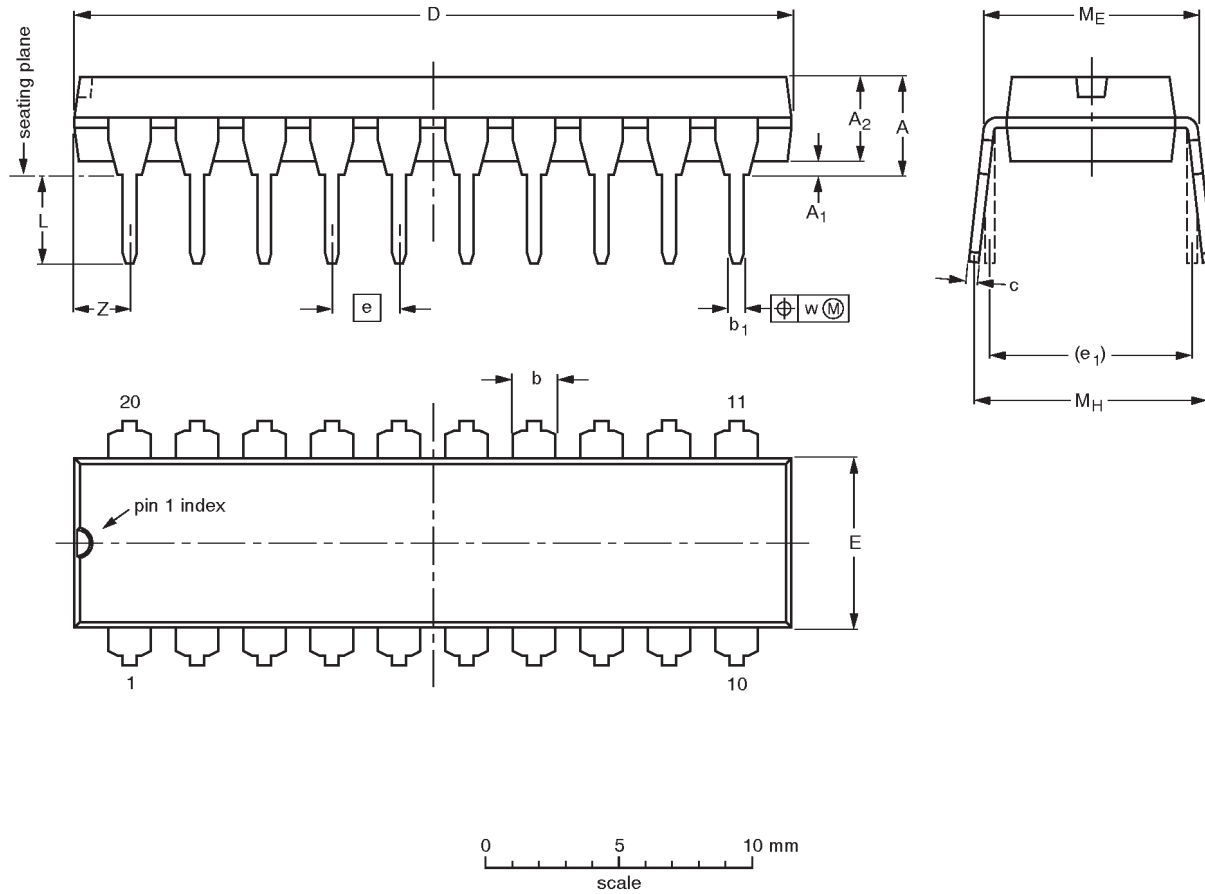
SF00128

# Octal bus transceiver, inverting (3-State)

## 74F640

**DIP20: plastic dual in-line package; 20 leads (300 mil)**

**SOT146-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

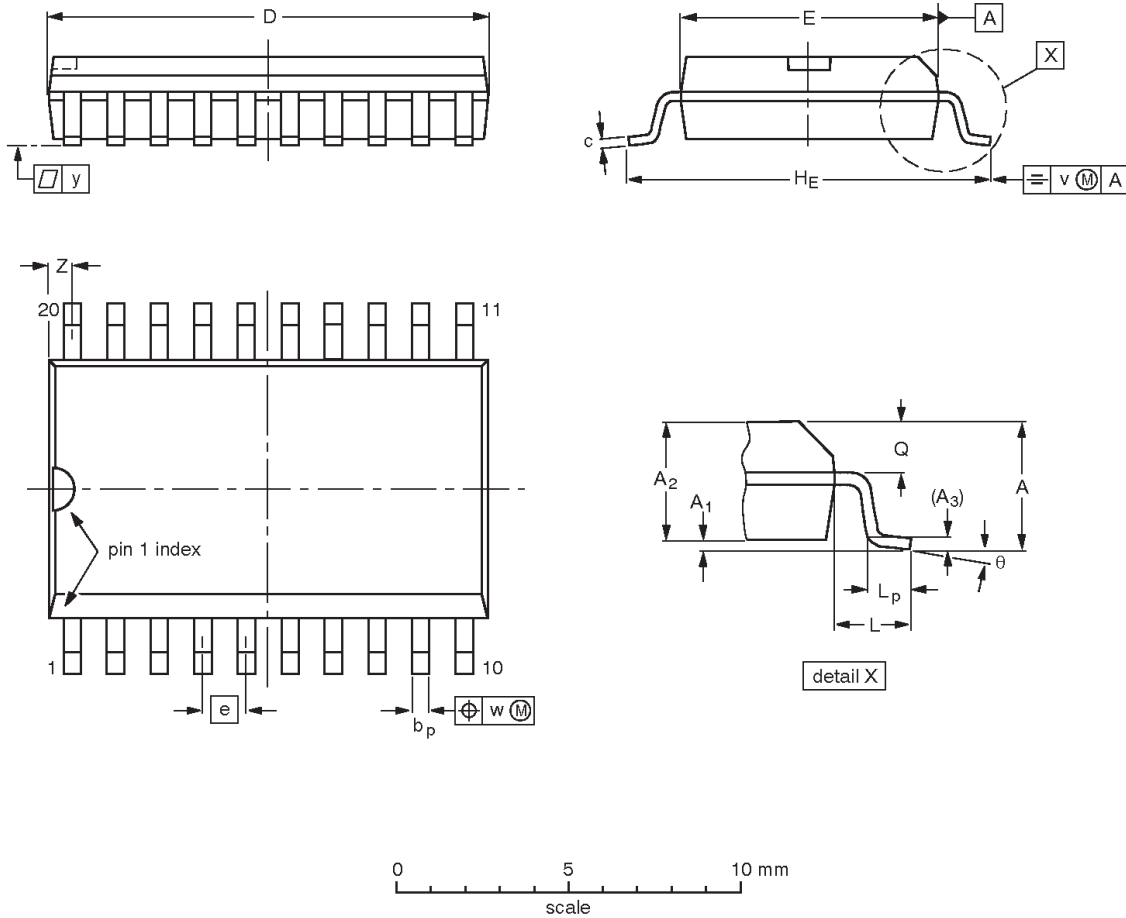


# Octal bus transceiver, inverting (3-State)

## 74F640

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

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**NOTES**

## Octal bus transceiver, inverting (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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