Shift Register

FAST 74F195, 74F195A

4-Bit Parallel-Access Shift Register

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in Low and High states) ('F195 only)
- Shift right and parallel load capability
- J - $\overline{K}$ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset
- Diode inputs ('F195A only)
- Improved AC, DC and functional properties ('F195A only)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA
74F195A	180MHz	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%, T_{amb} = 0°C to +70°C
16-pin plastic DIP	N74F195N
16-pin plastic SO	N74F195D
16-pin plastic DIP	N74F195AN
16-pin plastic SO	N74F195AD

DESCRIPTION

The 74F195 and 74F195A are 4-bit Parallel Access Shift Registers and their functional characteristics are indicated in the Logic diagram and Function Table. These devices are useful in a variety of shifting, counting and storage applications. They perform serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195 and 74F195A operate in two primary modes: shift right (Q0 → Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction Q0 → Q1 → Q2 →Q3 following each Low -to-High clock transition.

The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the

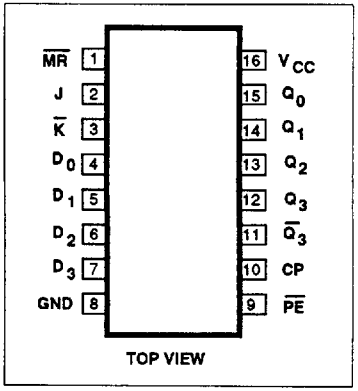
(continued)

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

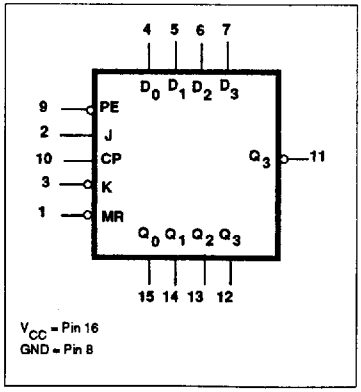
PINS	DESCRIPTION		74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	'F195	1.0/0.033	20μA/20μA
		'F195A	1.0/1.0	20μA/0.6mA
J, $\overline{K}$	J-K or D type serial inputs	'F195	1.0/0.033	20μA/20μA
		'F195A	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	'F195	1.0/0.033	20μA/20μA
		'F195A	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	'F195	2.0/0.066	40μA/40μA
		'F195A	1.0/1.0	20μA/0.6mA
Q0 - Q3, $\overline{Q3}$	Data outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

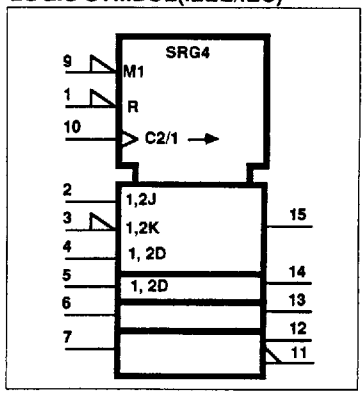
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Shift Register

FAST 74F195, 74F195A

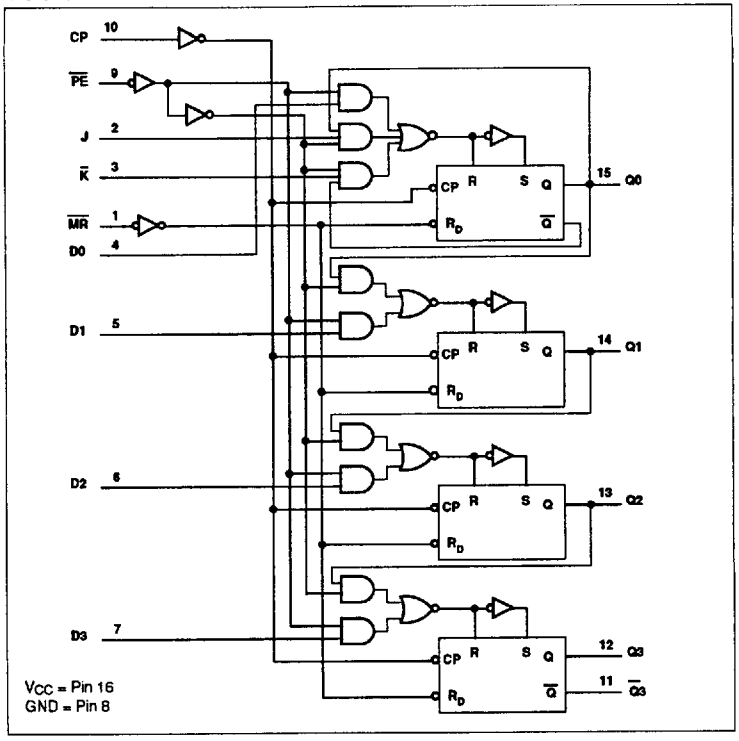
simple D-type input is made for general applications.

The device appears as four common clocked D flip-flops when the PE input is Low. After the Low-to-High clock transition, data on the parallel inputs (D0 - D3) is transferred to the respective Q0 - Q3 outputs. Shift left operation (Q3 - Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the PE input Low.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F195 and 74F195A utilize edge-triggering, therefore there is no restriction on the activity of the J, K, Dn, and PE inputs for logic operation, other than the set-up and hold time requirements.

A Low on the asynchronous Master Reset (MR) input sets all Q outputs Low, independent of any other input condition.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS					OPERATING MODES
MR	CP	PE	J	K	Dn	Q0	Q1	Q2	Q3	Q3	
L	X	X	X	X	X	L	L	L	L	H	Reset (clear)
H	↑	h	h	h	X	H	q0	q1	q2	q2	Shift, set First stage
H	↑	h	l	l	X	L	q0	q1	q2	q2	Shift, reset First stage
H	↑	h	h	l	X	q0	q0	q1	q2	q2	Shift, toggle First stage
H	↑	h	l	h	X	q0	q0	q1	q2	q2	Shift, retain First stage

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
dn(qn) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

Shift Register

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS [1]		LIMITS			UNIT
				Min	Typ [2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} =MIN, I_{OH} =MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} =MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
			±5%V_{CC}		0.35	0.5	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V	'F195			100	µA
		V_{CC} = MAX, V_I = 7.0V	'F195A			100	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	all others			20	µA
			MR ('F195)			40	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	others 'F195			-20	µA
			MR ('F195)			-40	
			'F195A			-600	
I_{OS}	Short-circuit output current [3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	'F195		45	58	mA
			'F195A		40	58	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F195

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Load mode	Waveform 1	120	130		110		MHz
		Shift mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q3}$		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q3}$		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74F195A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Load mode	Waveform 1	165	180		150		MHz
		Shift mode		180	190		170		
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.0 2.5	5.0 4.0	9.5 7.0	2.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q3}$		Waveform 1	2.0 2.0	5.5 4.0	9.5 6.5	2.5 2.0	9.5 7.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 2	2.0	4.0	7.0	2.0	7.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q3}$		Waveform 2	2.5	4.5	8.0	2.0	10.0	ns

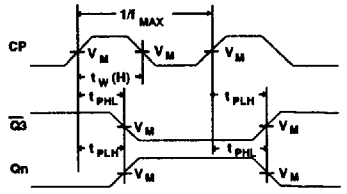
AC SETUP REQUIREMENTS FOR 74F195

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and Dn to CP	Waveform3	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	3.0 4.0			3.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width High	Waveform 1	6.0			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	6.0			6.0		ns

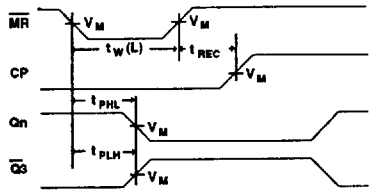
AC SETUP REQUIREMENTS FOR 74F195A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	2.5 2.5			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and Dn to CP	Waveform3	0.0 1.0			0.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	2.0 2.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width High	Waveform 1	4.5			4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	2.5			3.0		ns

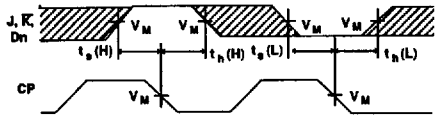
AC WAVEFORMS



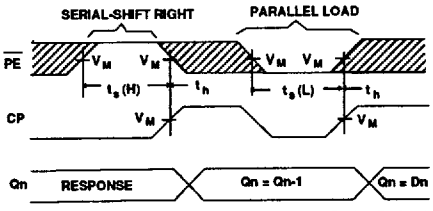
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



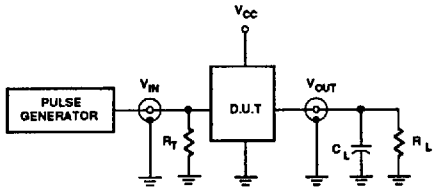
Waveform 3. Data Setup And Hold Times



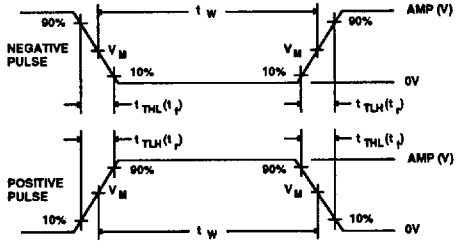
Waveform 4. Setup And Hold Times, Parallel Enable To Clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.