FAIRCHILD
SEMICONDUCTOR™

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74ACTQ652
Quiet Series™ Transceiver/Register

General Description

The ACTQ652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

The ACTQ652 utilizes Fairchild FACT Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Outputs source/sink 24 mA
- TTL-compatible inputs

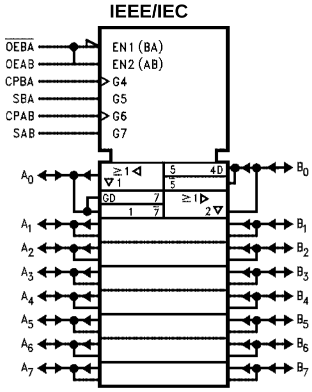
Ordering Code:

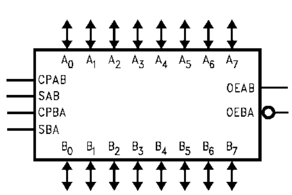
Order Number	Package Number	Package Description
74ACTQ652SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide Body
74ACTQ652MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACTQ652SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300” Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

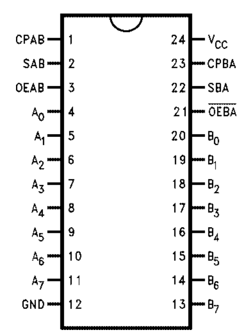
Logic Symbols

IEEE/IEC





Connection Diagram



Pin Descriptions

Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/3-STATE Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

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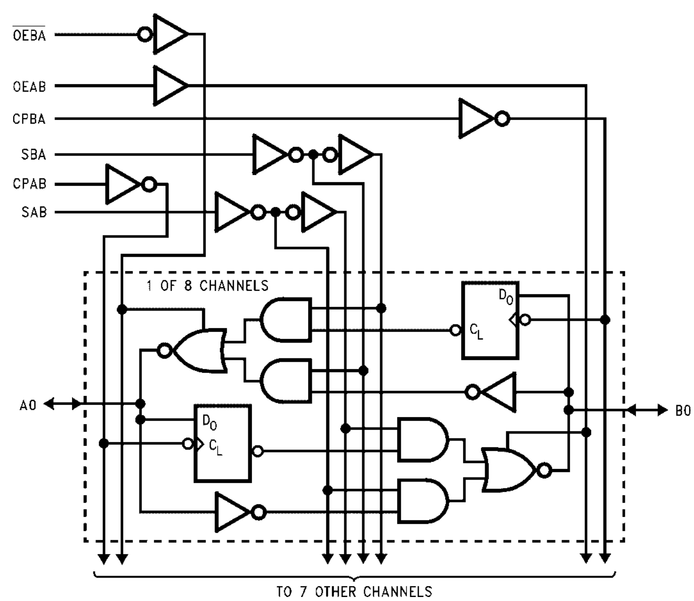
Function Table

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Not Specified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

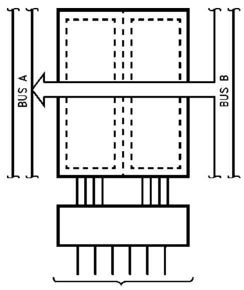
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

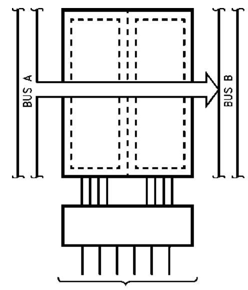
Data on the A or B data bus, or both can be stored in the internal D-type flip-flop by LOW-to-HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Note A: Real-Time Transfer Bus B to Bus A



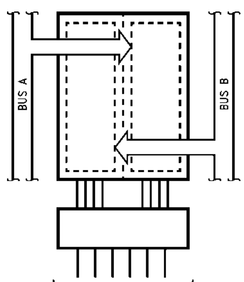
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



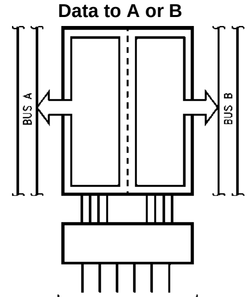
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Note C: Storage



OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Note D: Transfer Storage Data to A or B



OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1.

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	± 300 mA
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = +25°C Guaranteed Limits	T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum LOW Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum HIGH Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 µA
		4.5 5.5		3.86 4.86	3.76 4.76	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA I_{OH} = −24 mA (Note 3)
V_{OL}	Maximum LOW Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5		0.36 0.36	0.44 0.44	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA I_{OL} = 24 mA (Note 3)
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	V_I = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current	5.5		± 0.6	± 6.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 4)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	µA	V_{IN} = V_{CC} or GND
V_{OLP}	Maximum HIGH Level Output Noise	5.0	1.1	1.5		V	Figure 2Figure 3 (Note 5)(Note 6)
V_{OLV}	Maximum LOW Level Output Noise	5.0	−0.6	−1.2		V	Figure 2Figure 3 (Note 5)(Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 5)(Note 7)

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 5)(Note 7)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: PDIP package.

Note 6: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 7: Max number of data inputs (n) switching. (n – 1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{MAX}	Maximum Clock Frequency	5.0						MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	5.0	2.0	7.0	9.5	2.0	10.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	5.0	2.0	6.5	9.0	2.0	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	5.0	2.5	6.5	10.0	2.5	10.5	ns
t_{PZH} t_{PZL}	Enable Time OEBA to A (Note 8)	5.0	2.0	7.0	10.5	2.0	11.0	ns
t_{PHZ} t_{PLZ}	Disable Time OEBA to A (Note 8)	5.0	1.0	5.0	8.0	1.0	8.5	
t_{PZH} t_{PZL}	Enable Time OEAB to B	5.0	2.0	7.0	10.5	2.0	11.0	
t_{PHZ} t_{PLZ}	Disable Time OEAB to B	5.0	1.0	5.0	8.0	1.0	8.5	ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW, Bus to Clock	5.0	3.0			3.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, Bus to Clock	5.0	1.5			1.5		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0	4.0			4.0		ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 9) A to B, B to A or Clock to Output	5.0		0.5	1.0		1.0	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any separate outputs of the same device. The specification applies to any output switching in the same direction, either HIGH-to-LOW (T_{OSHL}) or LOW-to-HIGH (T_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	54	pF	$V_{CC} = 5.0V$

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

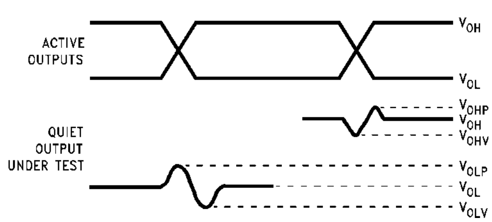
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 2. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH} until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

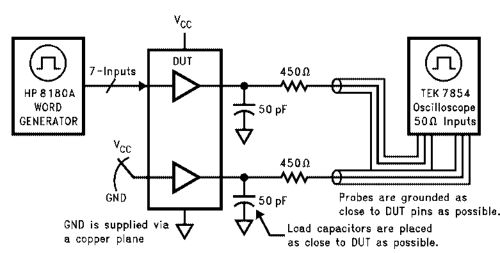
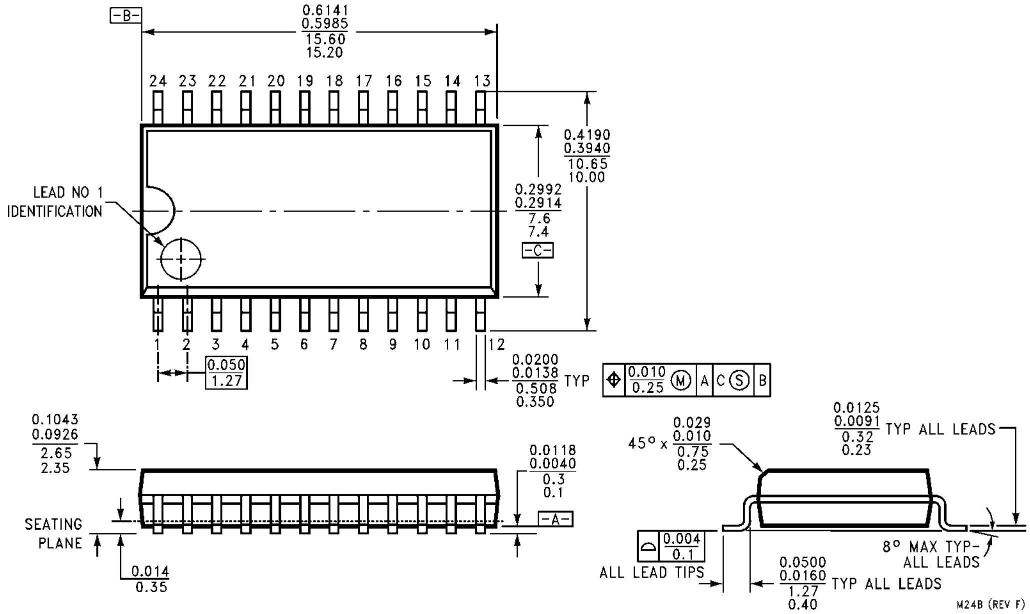


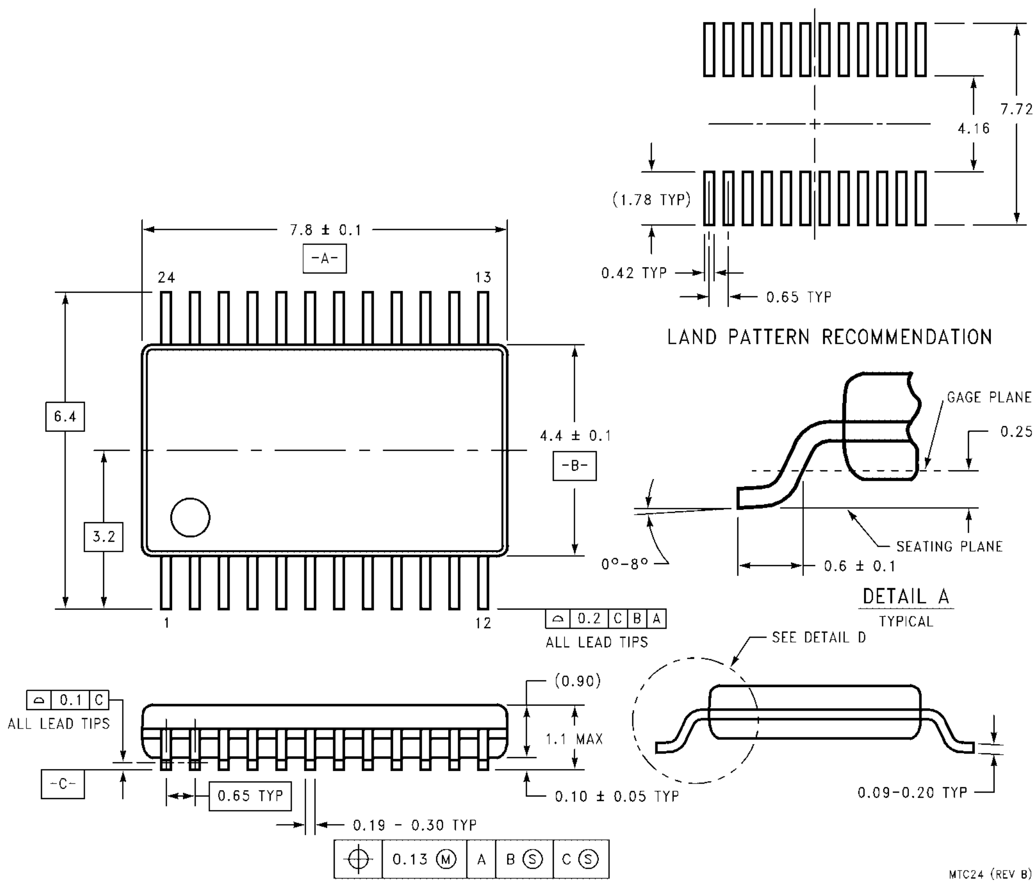
FIGURE 3. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



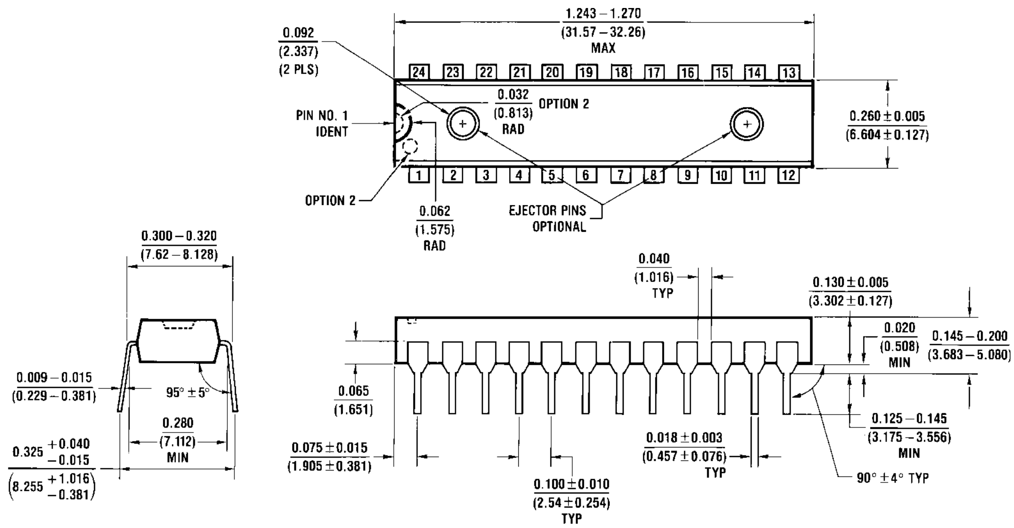
24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300" Wide
Package Number N24C

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