



74ACT257

QUAD 2 CHANNEL MULTIPLEXER (3-STATE)

- HIGH SPEED: $t_{PD} = 5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A=25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2V$ (MIN.), $V_{IL} = 0.8V$ (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 257
- IMPROVED LATCH-UP IMMUNITY



ORDER CODES

PACKAGE	TUBE	T & R
DIP	74ACT257B	
SOP	74ACT257M	74ACT257MTR
TSSOP		74ACT257TTR

DESCRIPTION

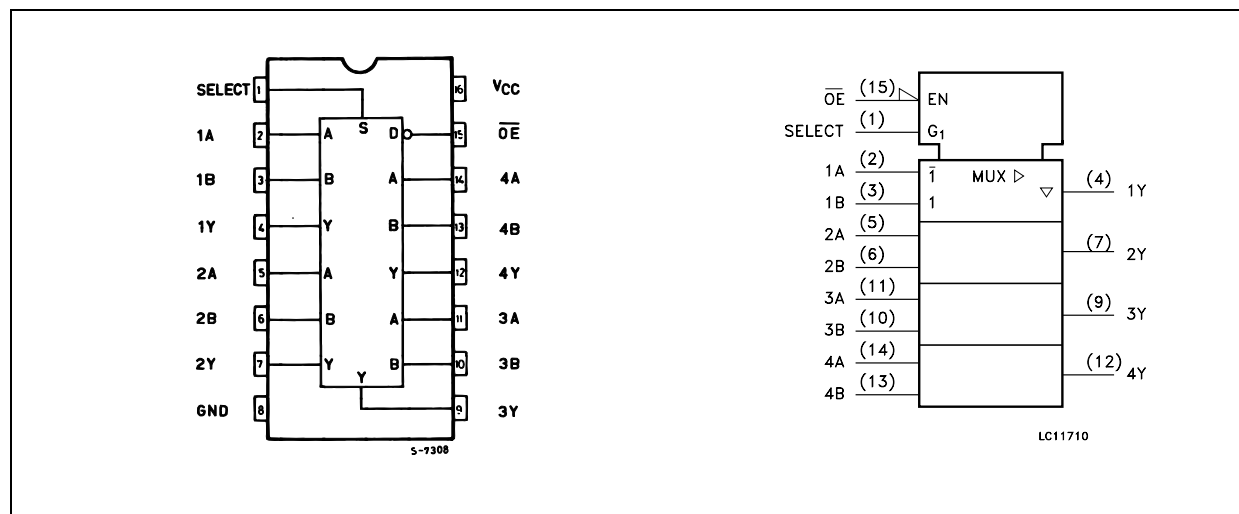
The 74ACT257 is an advanced high-speed CMOS QUAD 2-CHANNEL MULTIPLEXER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is composed of an independent 2-channel multiplexer with common SELECT and ENABLE (OE) inputs. It is a non-inverting multiplexer. When the ENABLE input is held HIGH, the outputs are forced to a high impedance state. When the

SELECT input is held LOW, "A" data is selected; when SELECT input is held HIGH, "B" data is selected.

The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.

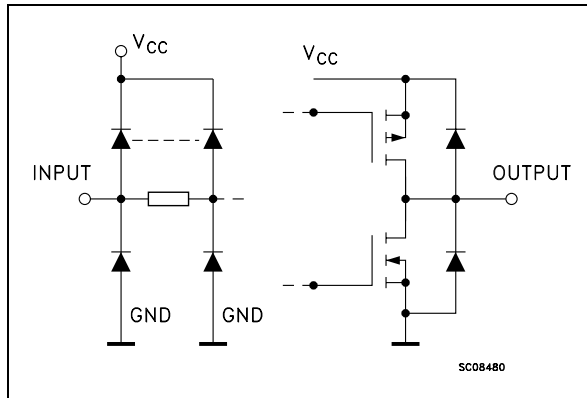
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



74ACT257

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

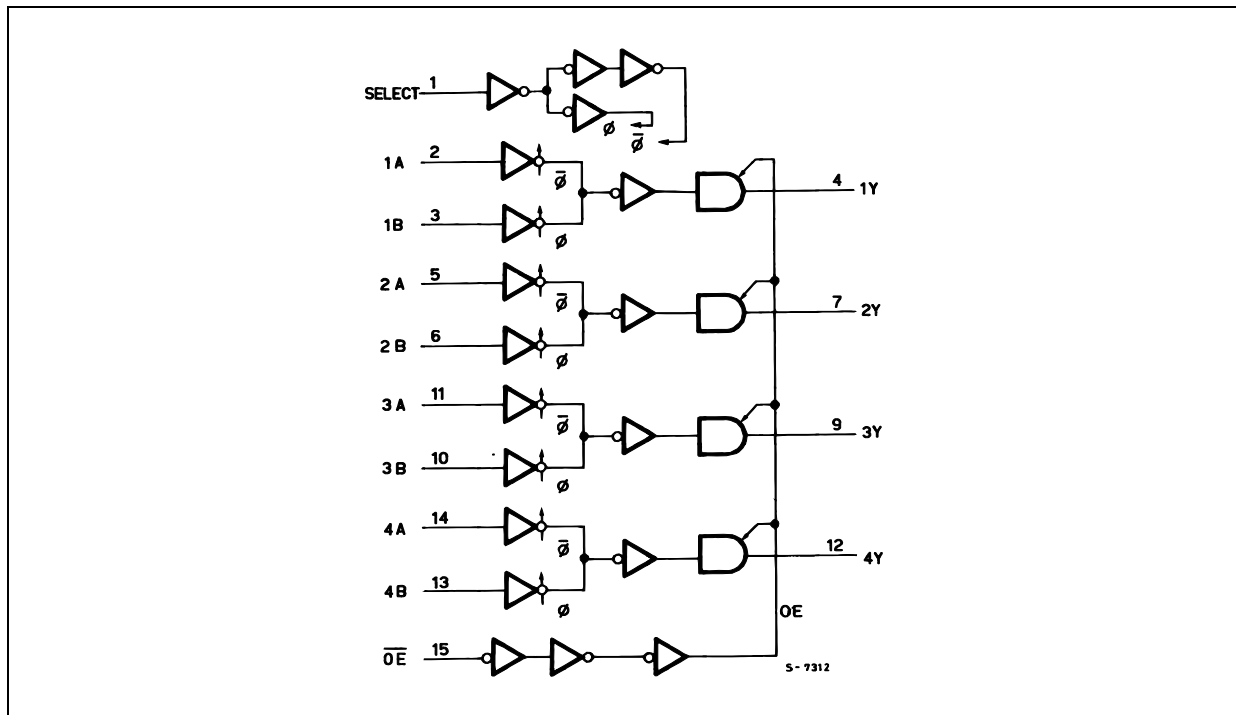
PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Inputs
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Outputs
15	OE	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUT
\overline{OE}	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care
Z : High Impedance

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 200	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to $5.5V$ (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
V _{IL}	Low Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.49		4.4		4.4		V
		5.5	I _O =-50 μA	5.4	5.49		5.4		5.4		
		4.5	I _O =-24 mA	3.86			3.76		3.7		V
		5.5	I _O =-24 mA	4.86			4.76		4.7		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.001	0.1		0.1		0.1	V
		5.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		4.5	I _O =24 mA			0.36		0.44		0.5	V
		5.5	I _O =24 mA			0.36		0.44		0.5	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5		± 5	mA
I _{CCT}	Max I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V		0.6			1.5		1.6	mA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		80	μA
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75		50	mA
I _{OHD}			V _{OHD} = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at a time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time A, B to Y	5.0(*)			5.0	8.0		9.0		9.0	ns
t _{PLH} t _{PHL}	Propagation Delay Time SELECT to Y	5.0(*)			6.0	9.0		10.0		10.0	ns
t _{PZL} t _{PZH}	Output Enable Time	5.0(*)			5.0	8.0		9.0		9.0	ns
t _{PLZ} t _{PHZ}	Output Disable Time	5.0(*)			6.0	9.0		10.0		10.0	ns

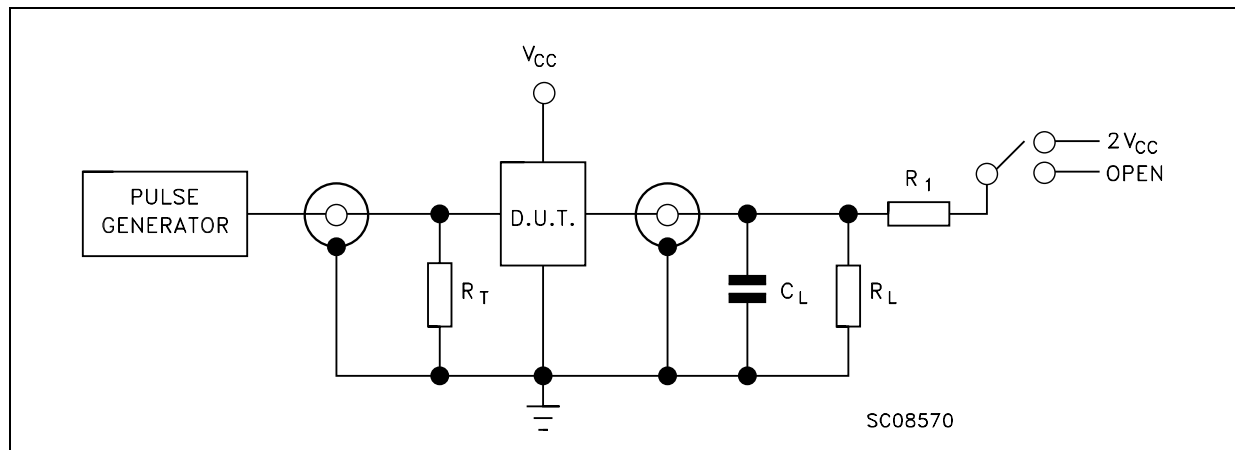
(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			5						pF
C _{OUT}	Output Capacitance	5.0			8						pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0	f _{IN} = 10MHz		25						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

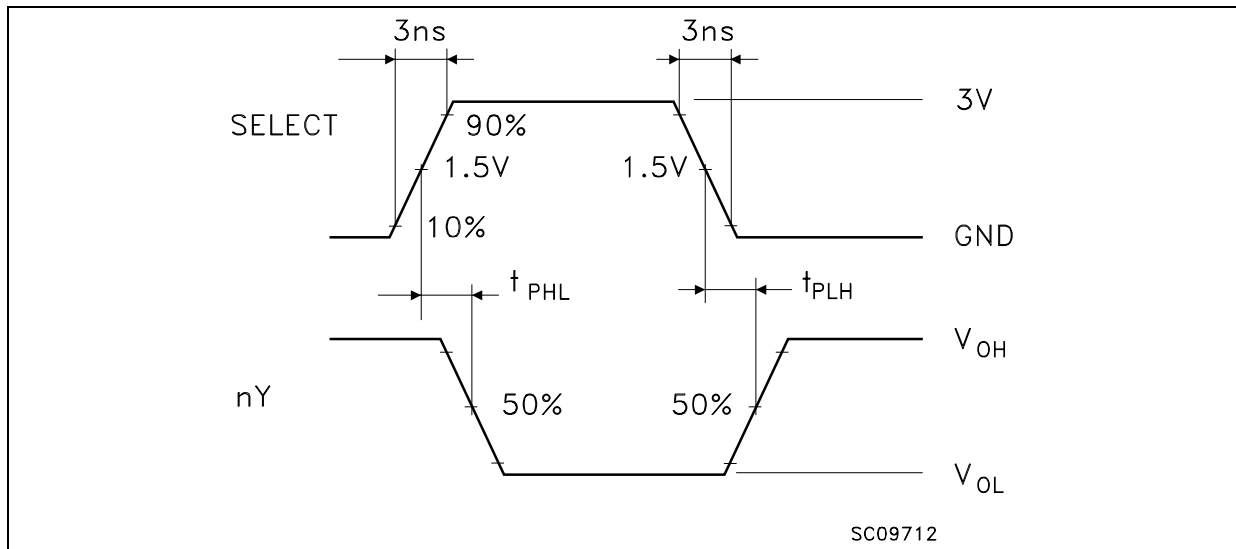
TEST CIRCUIT



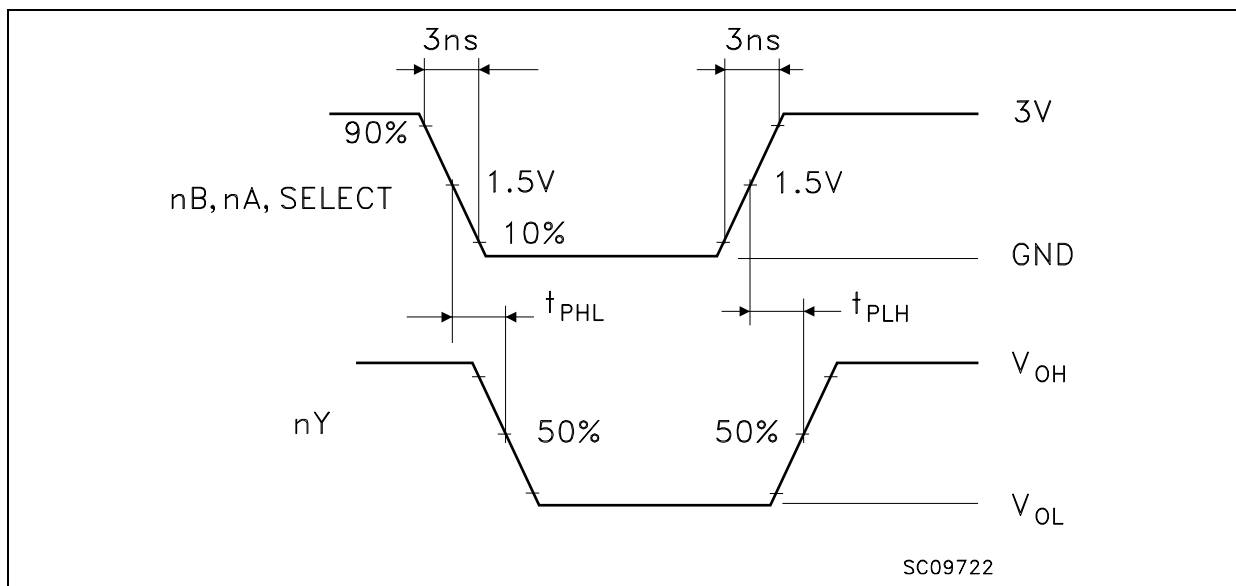
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	2V _{CC}
t _{PZH} , t _{PHZ}	Open

C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = R₁ = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING CONDITIONS (f=1MHz; 50% duty cycle)

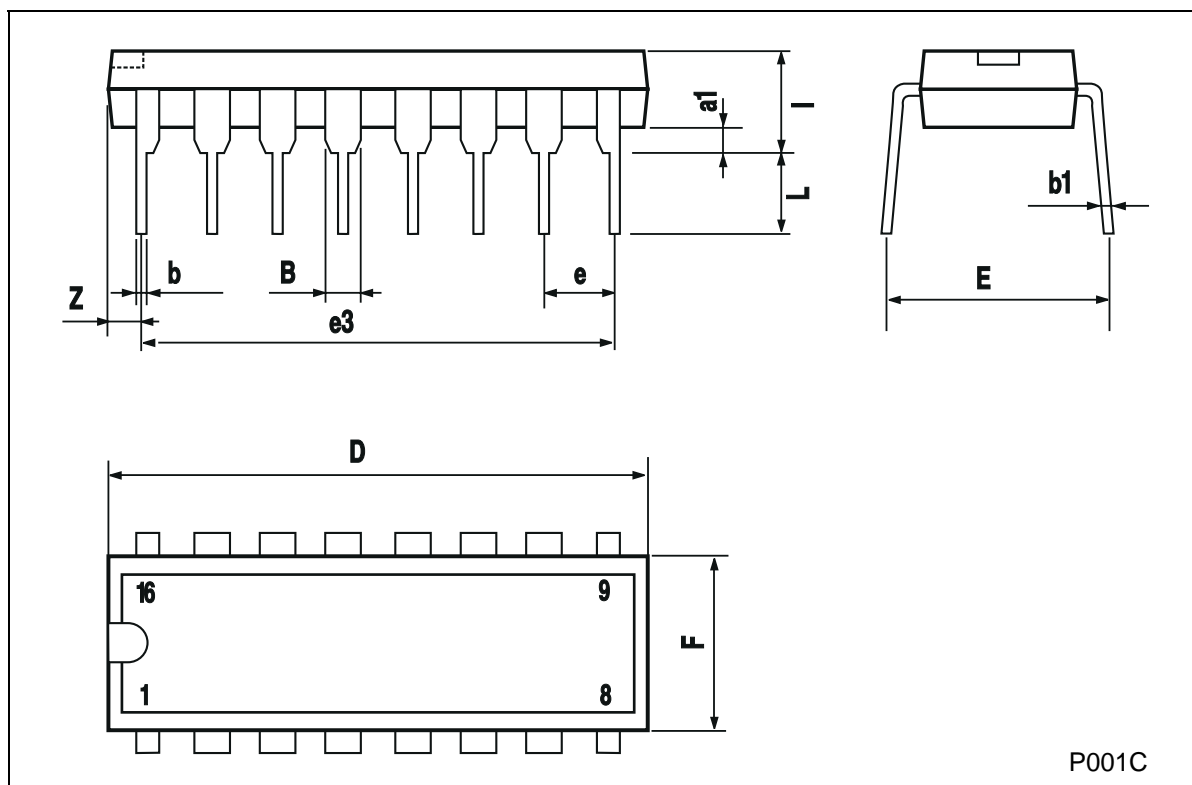


WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING CONDITIONS (f=1MHz; 50% duty cycle)



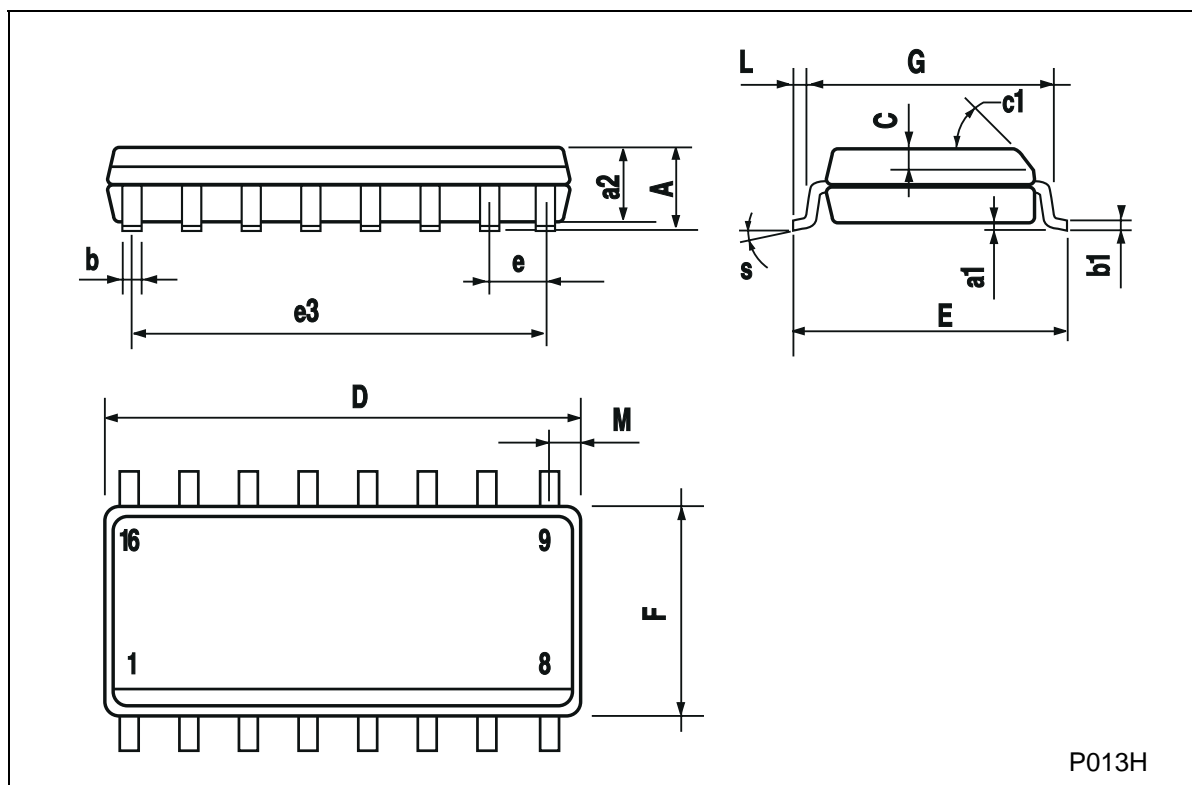
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



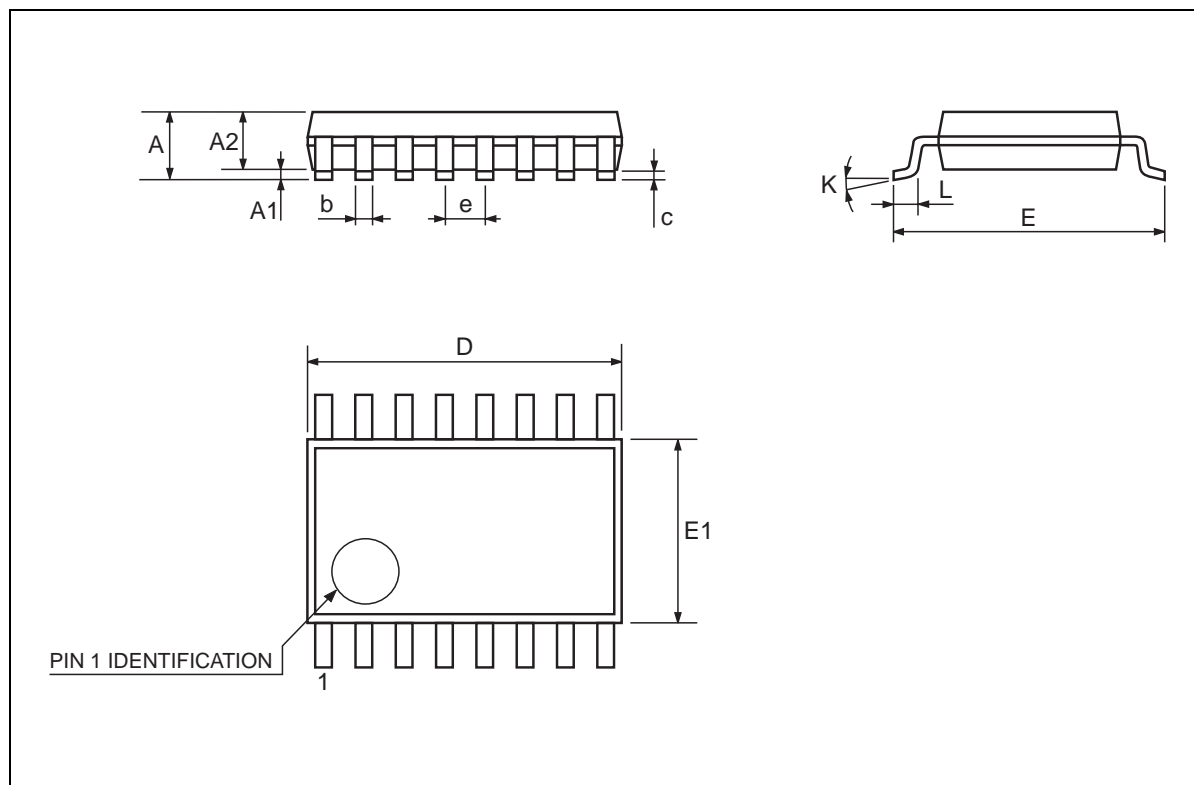
SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

