Document No.	853-1500
ECN No.	00731
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11544: Preliminary Specification
ACT11544: Product Specification
Octal latched transceiver with dual enable (3-State), INV

FEATURES

- Combines '245 and '373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11544 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11544 Octal Latched Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit inde-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	C_L = 50pF		5.4	6.5	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	43	47	pF
			Disabled	12	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

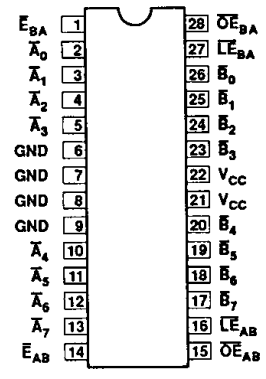
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

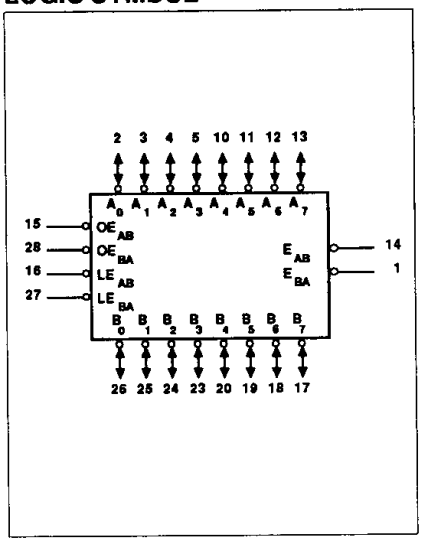
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11544N 74ACT11544N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11544D 74ACT11544D

PIN CONFIGURATION

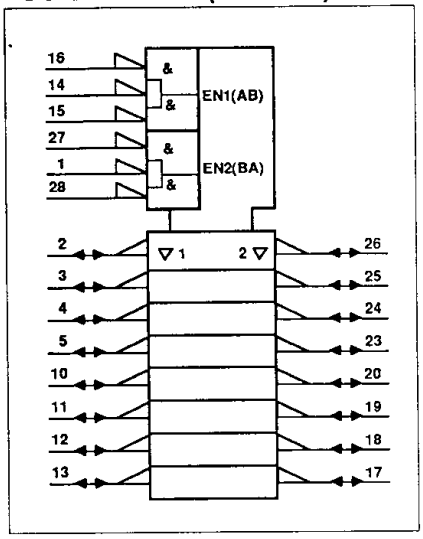
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

pendent control of inputting and outputting in either direction of data flow.

FUNCTIONAL DESCRIPTION

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{E}_{AB}$) input must be Low in order to enter data from A_0 - A_7 or take data from B_0 - B_7 as indicated in the Function Table. With $\overline{E}_{AB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition of the $\overline{LE}_{AB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{E}_{BA}$, $\overline{LE}_{BA}$, and $\overline{OE}_{BA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
16	$\overline{LE}_{AB}$	A-to-B latch enable input (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L L	↑ ↑	L L	h l	Z Z	Diasabled + latched
L L	L L	↑ ↑	h l	L H	Latch + display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H = High voltage level

h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)

L = Low voltage level

l = Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)

↑ = Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)

X = Don't care

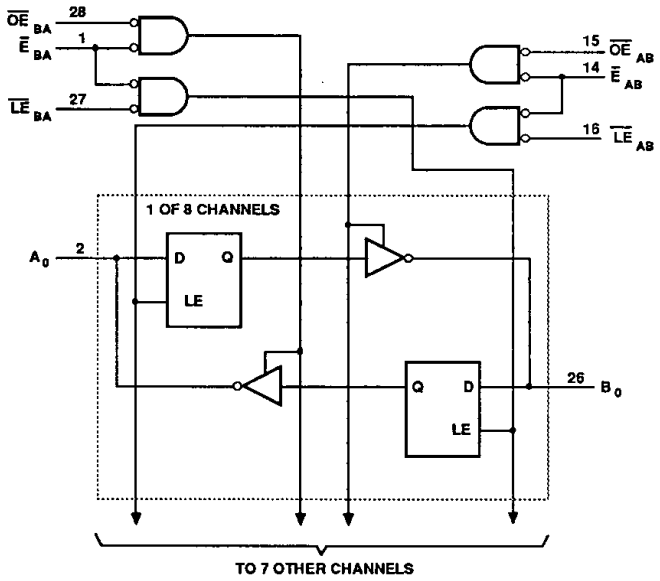
NC = No change

Z = High-impedance state

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

LOGIC DIAGRAM



Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11544			74ACT11544			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11544				74ACT11544				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11544					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	1	2.9 3.7	7.4 7.9	8.9 9.5	2.9 3.7	10.0 10.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ or $\overline{LE}_{AB}$ to $\overline{B}_n$	2	3.4 4.5	8.3 9.4	9.7 11.0	3.4 4.5	10.9 12.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.4 4.7	8.2 9.6	9.8 11.2	3.4 4.7	10.9 12.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.2 5.4	9.2 10.6	10.8 12.3	4.2 5.4	12.1 13.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	4.0 3.9	7.3 7.1	9.0 8.6	4.0 3.9	9.7 9.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.4 4.8	8.1 8.1	9.9 9.6	4.4 4.8	10.7 10.3	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to $\overline{A}_n$ or $\overline{LE}_{BA}$ to $\overline{B}_n$	4	0.5			0.5		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	4.0			4.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to $\overline{A}_n$ or $\overline{E}_{BA}$ to $\overline{B}_n$	4	0.0			0.0		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11544					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	1	2.6 3.0	4.9 5.8	6.7 7.8	2.6 3.0	7.4 8.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ or $\overline{LE}_{AB}$ to $\overline{B}_n$	2	3.0 3.9	5.4 6.8	7.2 8.6	3.0 3.9	8.0 9.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.1 4.0	5.6 7.1	7.4 9.2	3.1 4.0	8.2 10.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	3.7 4.7	6.3 7.8	8.2 9.8	3.7 4.7	9.1 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.6 3.6	5.8 5.7	7.5 7.6	3.6 3.6	8.0 8.1	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.1 4.4	6.4 6.4	8.2 8.0	4.1 4.4	8.8 8.5	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	2.5			2.5		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to $\overline{A}_n$ or $\overline{LE}_{BA}$ to $\overline{B}_n$	4	1.0			1.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to $\overline{A}_n$ or $\overline{E}_{BA}$ to $\overline{B}_n$	4	0.5			0.5		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

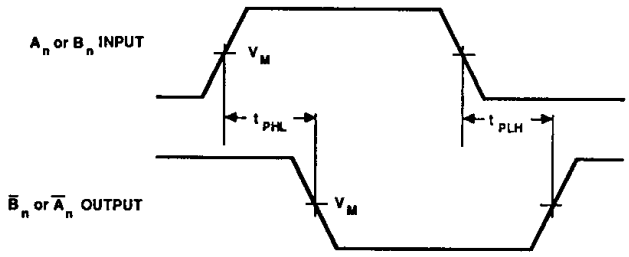
Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

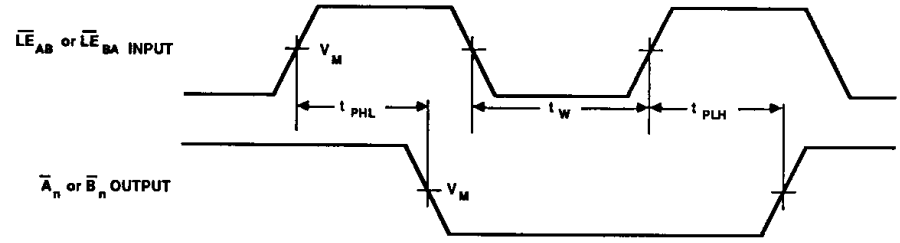
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11544					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	1	2.4 4.1	5.7 7.3	8.2 9.3	2.4 4.1	8.9 10.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ or $\overline{LE}_{AB}$ to $\overline{B}_n$	2	2.6 3.4	6.0 7.1	8.7 10.1	2.6 3.4	9.5 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.0 3.5	6.4 7.8	9.0 10.8	3.0 3.5	9.9 12.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	3.3 3.6	6.7 8.2	9.5 11.2	3.3 3.6	10.4 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	4.6 4.6	7.3 7.2	9.3 9.2	4.6 4.6	9.9 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.8 4.7	7.6 7.6	9.7 9.5	4.8 4.7	10.4 10.2	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	2.5			2.5		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to $\overline{A}_n$ or $\overline{LE}_{BA}$ to $\overline{B}_n$	4	2.0			2.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to $\overline{A}_n$ or $\overline{E}_{BA}$ to $\overline{B}_n$	4	1.5			1.5		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n or B_n) to Output ($\overline{B}_n$ or $\overline{A}_n$) Propagation Delays

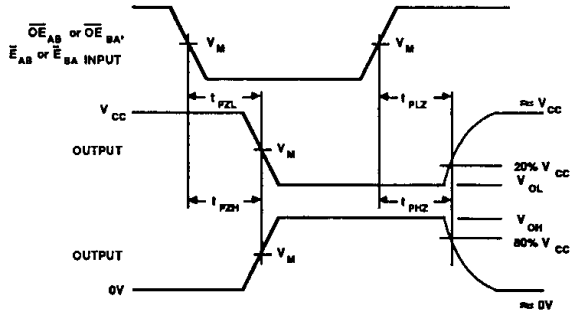


Waveform 2. Waveforms Showing the Latch Enable Input (LE_{XX}) Pulse Width and the Latch Enable Input to Output ($\overline{A}_n$ or $\overline{B}_n$) Propagation Delays

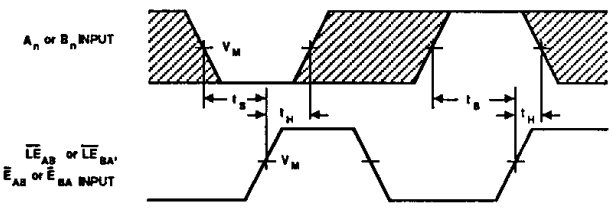
Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing the 3-State Output Enable and Disable Times

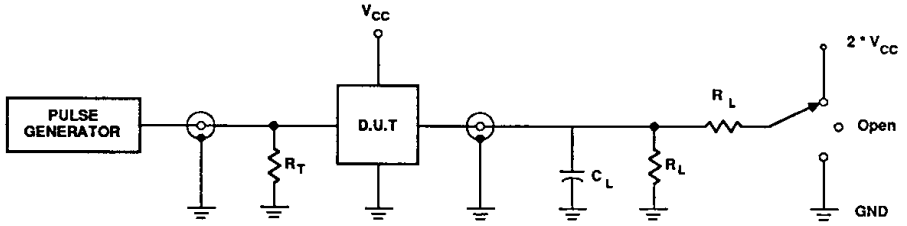


Waveform 4. Waveforms Showing the Data Setup and Hold Times for A_n or B_n Input to Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) Inputs

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2*V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns