

74ABT16543

16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ABT16543 16-bit transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Each byte has separate control inputs, which can be shorted together for full 16-bit operation.

Features

- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 32 mA and current sinking capability of 64 mA
- Separate control logic for each byte
- 16-bit version of the ABT543
- Separate controls for data flow in each direction
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

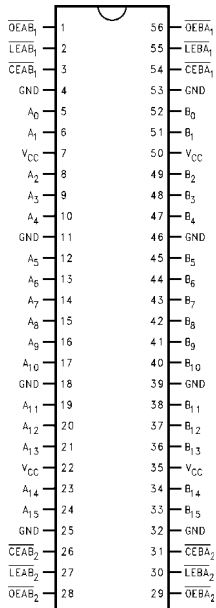
Ordering Code:

Order Number	Package Number	Package Description
74ABT16543CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16543CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for SSOP and TSSOP

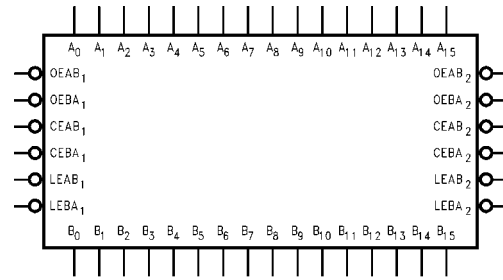


Pin Descriptions

Pin Names	Description
OEAB _n	A-to-B Output Enable Input (Active LOW)
OEBA _n	B-to-A Output Enable Input (Active LOW)
CEAB _n	A-to-B Enable Input (Active LOW)
CEBA _n	B-to-A Enable Input (Active LOW)
LEAB _n	A-to-B Latch Enable Input (Active LOW)
LEBA _n	B-to-A Latch Enable Input (Active LOW)
A ₀ -A ₁₅	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B ₀ -B ₁₅	B-to-A Data Inputs or A-to-B 3-STATE Outputs

74ABT16543 16-Bit Registered Transceiver with 3-STATE Outputs

Logic Symbol



Data I/O Control Table

Inputs			Latch Status	Output Buffers
CEAB _n	LEAB _n	OEAB _n	(Byte n)	(Byte n)
H	X	X	Latched	HIGH Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	HIGH Z
L	X	L	—	Driving

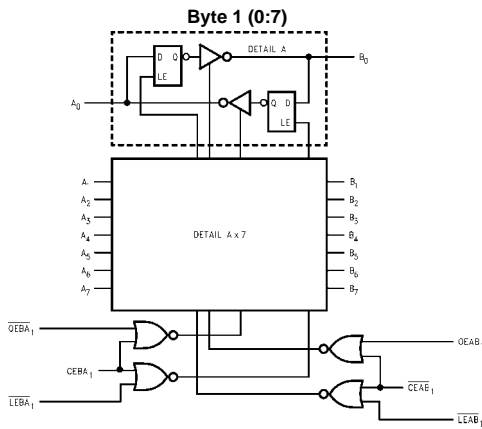
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 A-to-B data flow shown;
 B-to-A flow control is the same, except using $\overline{\text{CEBA}}_n$, $\overline{\text{LEBA}}_n$ and $\overline{\text{OEBA}}_n$

Functional Description

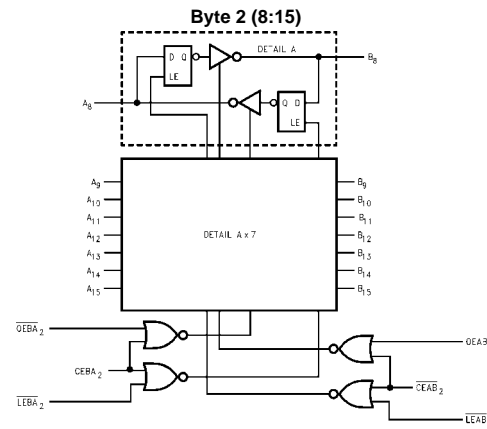
The ABT16543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable (CEAB) input must be low in order to enter data from the A port or take data from the B-Port as indicated in the Data I/O Control Table. With CEAB low, a low signal on (LEAB) input makes the A to B latches transparent; a subsequent low to high transition of the LEAB line puts the A latches in the storage

mode and their outputs no longer change with the A inputs. With CEAB and OEAB both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the CEBA, LEBA and OEBA. Each byte has separate control inputs, allowing the device to be used as two 8-bit transceivers or as one 16-bit transceiver.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		DC Latchup Source Current	-500 mA
Storage Temperature	-65°C to +150°C	Over Voltage Latchup (I/O)	10V
Ambient Temperature under Bias	-55°C to +125°C	Recommended Operating Conditions	
Junction Temperature under Bias	-55°C to +150°C	Free Air Ambient Temperature	-40°C to +85°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V	Supply Voltage	+4.5V to +5.5V
Input Voltage (Note 2)	-0.5V to +7.0V	Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Input Current (Note 2)	-30 mA to +5.0 mA	Data Input	50 mV/ns
Voltage Applied to Any Output in the Disable or Power-Off State	-0.5V to +5.5V	Enable Input	20 mV/ns
in the HIGH State	-0.5V to V _{CC}	Clock Input	100 mV/ns
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)	<p>Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.</p> <p>Note 2: Either voltage limit or current limit is sufficient to protect inputs.</p>	

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA (Non-I/O Pins)
V _{OH}	Output HIGH Voltage	2.5					I _{OH} = -3 mA, (A _n , B _n) I _{OH} = -32 mA, (A _n , B _n)
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA, (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μ A, (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current			1	μ A	Max	V _{IN} = 2.7V (Non-I/O Pins) ((Note 3) V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7	μ A	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μ A	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			-1	μ A	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 3) V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			10	μ A	0V-5.5V	V _{OUT} = 2.7V (A _n , B _n); OEAB or CEAB = 2V
I _{IL} + I _{OZL}	Output Leakage Current			-10	μ A	0V-5.5V	V _{OUT} = 0.5V (A _n , B _n); OEAB or CEAB = 2V
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μ A	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			100	μ A	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input			2.5	mA	Max	V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 3)	No Load		0.25	mA/MHz	Max	Outputs Open, CEAB, OEAB, LEAB = GND, CEBA = V _{CC} , One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed but not tested.

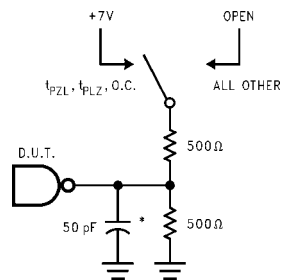
AC Electrical Characteristics							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	3.0	5.7	1.5	5.7	ns
t_{PHL}	A_n to B_n or B_n to A_n						
t_{PLH}	Propagation Delay	1.5	3.0	5.5	1.5	5.5	ns
t_{PHL}	\overline{LEAB}_n to B_n , \overline{LEBA}_n to A_n						
t_{PZH}	Enable Time	1.5	2.8	5.2	1.5	5.2	ns
t_{PZL}	\overline{OEBA}_n or \overline{OEAB}_n to A_n or B_n						
t_{PHZ}	Disable Time	1.6	3.1	6.0	1.6	6.0	ns
t_{PLZ}	\overline{OEAB}_n or \overline{OEBA}_n to A_n or B_n						
t_{PZH}	Enable Time	1.5	3.1	6.2	1.5	6.2	ns
t_{PZL}	\overline{CEBA}_n or \overline{CEAB}_n to A_n or B_n						
t_{PHZ}	Disable Time	1.7	3.2	6.3	1.7	6.3	ns
t_{PLZ}	\overline{CEBA}_n or \overline{CEAB}_n to A_n or B_n						

AC Operating Requirements							
(SSOP Package)							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		Units	
		Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	2.0		2.0		ns	
$t_S(L)$	A_n or B_n to \overline{LEBA}_n or \overline{LEAB}_n	2.0		2.0			
$t_H(H)$	Hold Time, HIGH or LOW	1.0		1.0		ns	
$t_H(L)$	A_n or B_n to \overline{LEBA}_n or \overline{LEAB}_n	1.0		1.0			
$t_W(L)$	Pulse Width, LOW	3.0		3.0		ns	

Capacitance					
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$	
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$ (non I/O pins)	
$C_{I/O}$ (Note 4)	Output Capacitance	11.0	pF	$V_{CC} = 5.0\text{V}$ (A_n , B_n)	

Note 4: $C_{I/O}$ is measured at frequency, $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

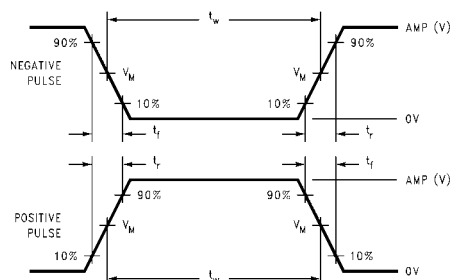


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

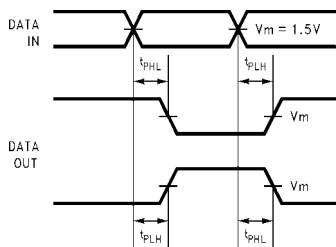


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

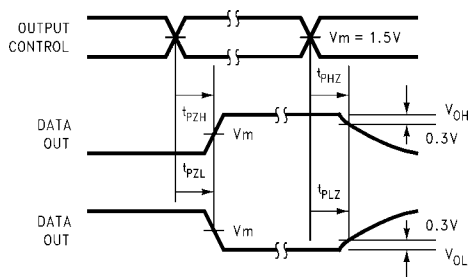


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

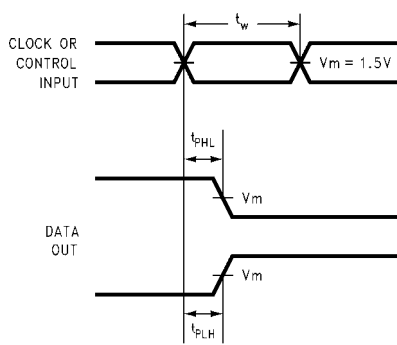


FIGURE 5. Propagation Delay, Pulse Width Waveforms

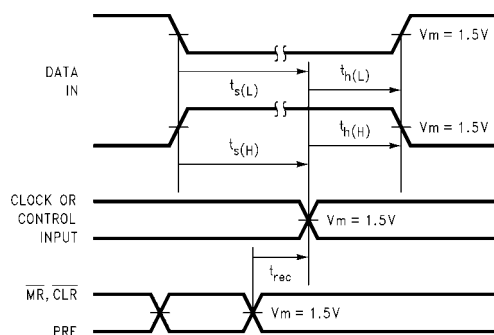
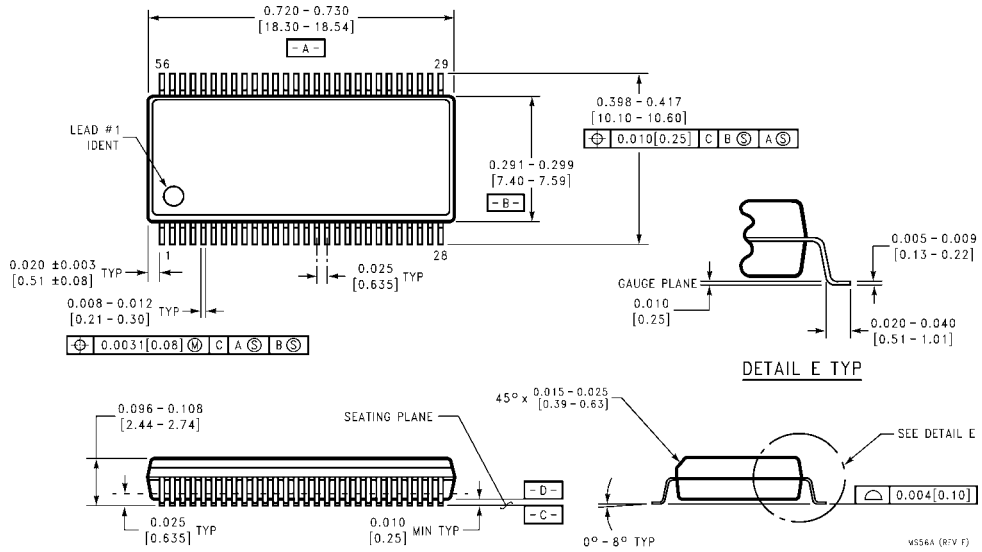


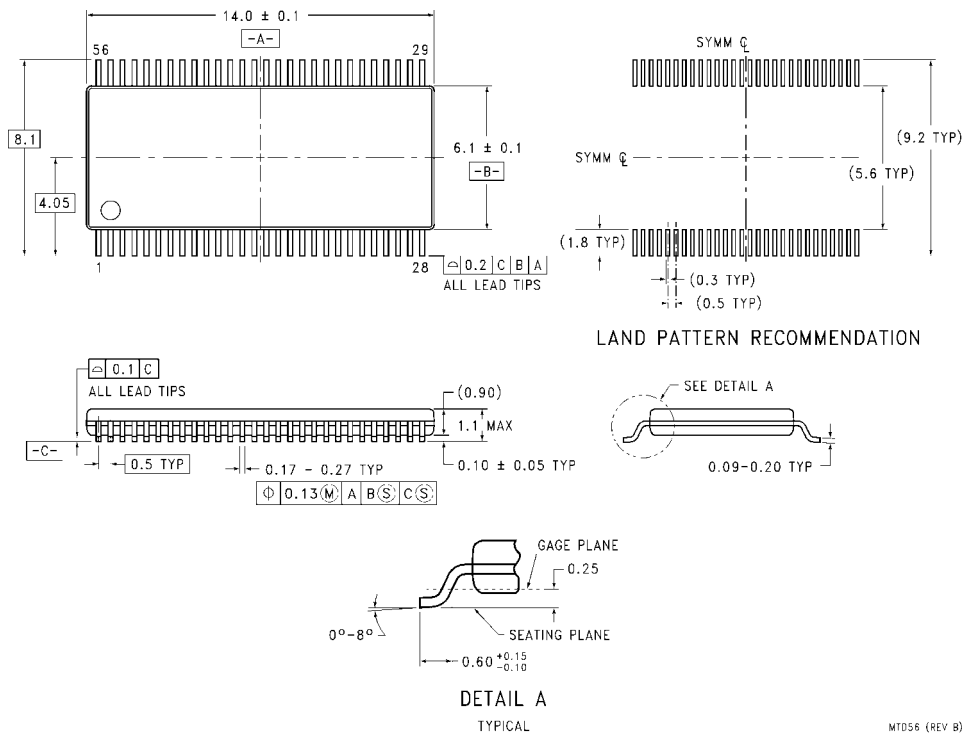
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

MT056 (REV B)

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com