# HS-3374RH

## Radiation Hardened 8-Bit Bidirectional CMOS/TTL Level Converter

March 1996

### Features

- **Devices QML Qualified in Accordance with MIL-PRF-38535**
- **Detailed Electrical and Screening Requirements are Contained in SMD# 5962-9XXXX and Intersil' QM Plan**
- **Radiation Hardened EPI-CMOS**
  - **Total Dose 1 x $10^5$ RAD(Si)**
  - **Latch-Up Immune > 1 x $10^{12}$ RAD (Si)/s (Note 1)**
- **Low Propagation Delay Time**
  - **Typical CMOS to TTL Pre-RAD 40ns**
  - **Typical CMOS to TTL Post 100K RAD 40ns**
  - **Typical TTL to CMOS Pre-RAD 50ns**
  - **Typical TTL to CMOS Post 100K RAD 50ns**
- **Low Standby Power**
- **+10V CMOS and +5V TTL Power Supply Inputs**
- **Eight Non-inverting Three-State Input/Output Channels**
- **No External TTL Input Pull-Up Resistors Required**
- **High TTL Sink Current**
- **Equivalent to Sandia SA2996**
- **Military Temperature Range -55°C to +125°C**

### Description

The Intersil HS-3374RH is a radiation hardened 8-bit bidirectional level converter designed to interface CMOS logic levels with TTL logic levels in radiation hardened bus oriented systems. The HS-3374RH is fabricated using a radiation hardened EPI-CMOS process and features eight parallel bidirectional buffer/level converters.

Two control inputs, ENABLE and DISABLE, are used to determine the direction of data flow, and to set both the in puts and outputs in the high impedance state. The control inputs may be driven by either TTL or CMOS logic drivers capable of sinking one standard TTL load.

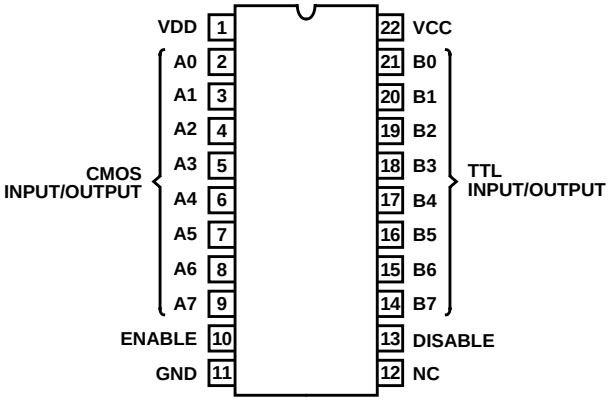
The HS-3374RH is a non-inverting version of the industry standard CD40116. The non-inverting outputs of the HS-3374RH reduce PC board chip count by eliminating the need to restore data back to a non-inverted format.

NOTE:

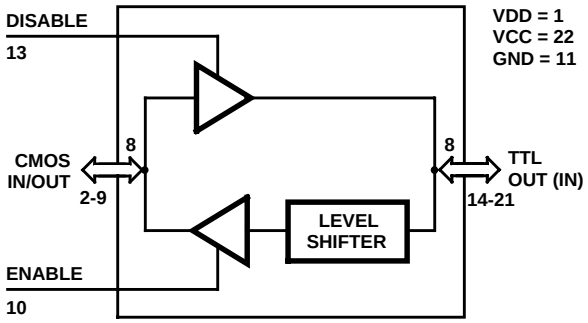
1. For operation at 10V and transient levels above 1 x $10^{10}$ RAD (Si)/s, please refer to Application Note 401.

### Pinout

**HS-3374RH**
**MIL-STD-1835, CDIP2-T22**
**(SBDIP)**
TOP VIEW




### Functional Diagram




### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|---|---|---|---|
| 5962R9XXXX01QRC | -55°C to +125°C | MIL-PRF-38535 Level Q | 22 Lead SBDIP |
| 5962R9XXXX01VRC | -55°C to +125°C | MIL-PRF-38535 Level V | 22 Lead SBDIP |
| HS1-3374 (SAMPLE) | +25°C | Sample | 22 Lead SBDIP |



Spec Number **518052**
File Number **3038.1**

## Absolute Maximum Ratings

Supply Voltage . . . . . +11.0V
I/O Voltage Applied . . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65$^{o}$C to +150$^{o}$C
Junction Temperature . . . . . +175$^{o}$C
Lead Temperature (Soldering 10s) . . . . . +300$^{o}$C
ESD Classification . . . . . Class 1

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ ($^{o}$C/W) | $\theta_{JC}$ ($^{o}$C/W) |
|---|---|---|
| SBDIP Package | 74.8 | 12.3 |

Maximum Package Power Dissipation at +125$^{o}$C
SBDIP Package . . . . . .0.67W
If Device Power Exceeds Package Dissipation Capability, Provide Heat Sinking or Derate Linearly at the Following Rate:
SBDIP Package . . . . . .13.4mW/$^{o}$C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating Voltage Range VDD . . . . . +9.5V to +10.5V
VCC . . . . . +4.75V to +5.25V
Operating Temperature Range . . . . . -55$^{o}$C to +125$^{o}$C
Input Voltage Range
Data Inputs (CMOS) . . . . . .GND-0.3 to VDD+0.3
Data Inputs (TTL) . . . . . .GND-0.3 to VCC+0.3
Enable, Disable Inputs . . . . . .GND-0.3 to VDD+0.3
Input Low Voltage (CMOS) . . . . . GND to 1V
Input High Voltage (CMOS) . . . . . .VDD-1.0V to VDD
Input Low Voltage (TTL) . . . . . 0.8V
Input High Voltage (TTL) . . . . . 2.8V

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| ENABLE AND DISABLE IINPUTS | | | | | | | |
| Input Leakage Current | IIH CMOS | VDD = 10.5V, VCC = 5.25V, VIN = 10.5V, Floating Outputs | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 1 | µA |
| TTL INPUT TO CMOS OUTPUTS | | | | | | | |
| Input Leakage Current | IIL IIH | VDD = 10.5V, VCC = 5.25V, VIN = 0.8V, Other Inputs at 2.8V | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | -1 | - | µA |
| | | VDD = 10.5V, VCC = 5.25V, VIN = 2.8V, other Inputs = 0.8V | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 1 | µA |
| High Level Output Voltage | VOH | VDD = 9.5V, VCC = 4.75V, VIH = 2.8V, VIL = 0.8V, IOH = -2.0mA | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | 9 | - | V |
| Low level output Voltage | VOL | VDD = 10.5V, VCC = 5.25V, VIH = 2.8V, VIL 0.8V, IOL = 2.0mA | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 0.5 | V |
| CMOS to TTL OUTPUTS | | | | | | | |
| High Level Output Voltage | VOH | VDD = 9.5, VCC = 4.75V, VIH = 8.5V, VIL = 1.0V, IOH = -2.0mA | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | 3 | - | V |
| Low Level Output Voltage | VOL | VDD = 10.5V, VCC = 5.25V, VIH = 9.5V, VIL = 1.0V, IOL = 11mA | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 0.4 | V |
| Output Leakage Current | IOZL | VDD = 10.5V, VCC = 5.25V, VIN = 0V, All other pins high | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | -10 | - | µA |
| | IOZH | VDD = 10.5V, VCC = 5.25V, VIN = 2.8V, All other pins at GND | 1, 2, 3 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 10 | µA |

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| Functional Tests | FT | CMOS:<br>1.) VDD = 10.5V, VCC = 5.25V<br>2.) VDD = 9.5V, VCC = 4.75V, VIH = VDD-1V, VIL = 1V<br>TTL:<br>1.) VDD = 10.5V, VCC = 5.25V<br>2.) VDD = 9.5V, VCC = 4.75V, VIH = 2.8V, VIL = 0.8V | 7, 8A, 8B | -55°C, +25°C, +125°C | - | - | - |
| Static Current 1 | SIDD1 | VDD = 10.5V, VCC = 5.25V, EN = 2.8V, DISABLE = 2.8V, Floating Outputs | 1, 2, 3 | -55°C, +25°C, +125°C | - | 300 | µA |
| Static Current 2 | SIDD2 | VDD = 10.5V, VCC = 5.25V, EN = 0V, DISABLE = 2.8V, Floating Outputs | 1, 2, 3 | -55°C, +25°C, +125°C | - | 100 | µA |
| Static Current | SICC | VDD = 10.5, VCC = 5.25V, EN = 0V, DISABLE = 2.8V, Floating Output, Measure VCC pin | 1, 2, 3 | -55°C, +25°C, +125°C | - | 5 | µA |

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | GROUP A SUB-GROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| Propagation Delay Times CMOS/TTL Data In to Data Out | TPHLCT | 9, 10, 11 | -55°C, +25°C, +125°C | - | 40 | ns |
| Propagation Delay Times CMOS Data In to Data Out | TPLHCT | 9, 10, 11 | -55°C, +25°C, +125°C | - | 50 | ns |
| Propagation Delay Times CMOS/TTL Data In to Data Out | TPHLTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 85 | ns |
| Propagation Delay Time TTL/CMOS Data In to Data Out | TPLHTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 70 | ns |
| Transition Time CMOS/TTL Input/Output | TTHLCT | 9, 10, 11 | -55°C, +25°C, +125°C | - | 20 | ns |
| Transition Time CMOS/TTL Input/Output | TTLHCT | 9, 10, 11 | -55°C, +25°C, +125°C | - | 70 | ns |
| Transition Time CMOS/TTL Input/Output | TTHLTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 50 | ns |
| Transition Time CMOS/TTL Input/Output | TTLHTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 50 | ns |
| Propagation Delay Time TTL/CMOS Enable to CMOS Out | TPHZTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 90 | ns |
| Propagation Delay Time TTL/CMOS Enable to CMOS Out | TPZHTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 90 | ns |
| Propagation Delay Time TTL/CMOS Enable to CMOS Out | TPLZTC | 9, 10, 11 | -55°C, +25°C, +125°C | - | 85 | ns |

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

| PARAMETER | SYMBOL | GROUP A SUB-GROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| Propagation Delay Time TTL/CMOS Enable to CMOS Out | TPZLTC | 9, 10, 11 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 90 | ns |
| Propagation Delay Time CMOS/TTL Disable to TTL Out | TPHZCT | 9, 10, 11 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 70 | ns |
| Propagation Delay Time CMOS/TTL Disable to TTL Out | TPZHCT | 9, 10, 11 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 130 | ns |
| Propagation Delay Time CMOS/TTL Disable to TTL Out | TPLZCT | 9, 10, 11 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 120 | ns |
| Propagation Delay Time CMOS/TTL Disable to TTL Out | TPZLCT | 9, 10, 11 | -55$^{o}$C, +25$^{o}$C, +125$^{o}$C | - | 125 | ns |

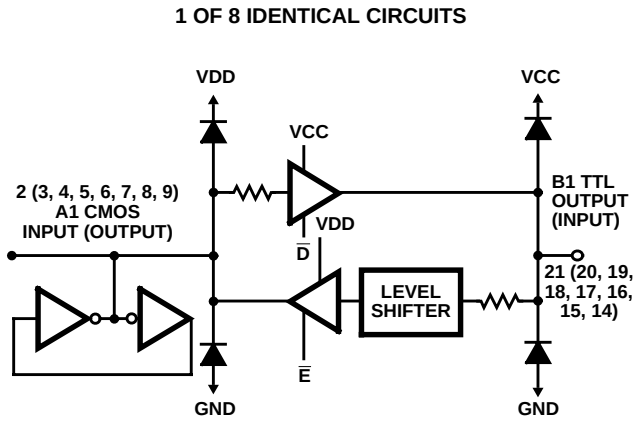
NOTE: Timings are measured with the following conditions: CL = 100pF, VDD = 9.5V, VCC = 4.75V, VIH = 8.5V (2.8V), VIL = 1.0V (0.8V).

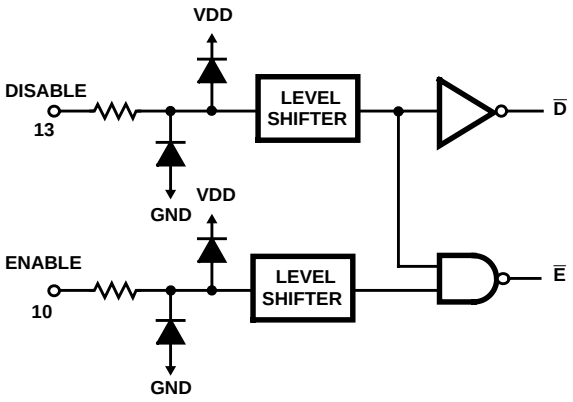
**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| Input, Output Capacitance | CMOS CI/O | VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground | +25$^{o}$C | - | 13 | pF |
| Input Capacitance | CIN | VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground | +25$^{o}$C | - | 15 | pF |
| Input, Output Capcitance | TTL CI/O | VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground | +25$^{o}$C | - | 17 | pF |

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

## Functional Block Diagram




NOTES:

1. Enable and disable are TTL type inputs
2. D and E outputs are common to all 8 channels

| INPUT (OUTPUT) | | OUTPUT (INPUT) | |
|---|---|---|---|
| DATA | TERMINAL NUMBER | DATA | TERMINAL NUMBER |
| A0 | 2 | B0 | 21 |
| A1 | 3 | B1 | 20 |
| A2 | 4 | B2 | 19 |
| A3 | 5 | B3 | 18 |
| A4 | 6 | B4 | 17 |
| A5 | 7 | B5 | 16 |
| A6 | 8 | B6 | 15 |
| A7 | 9 | B7 | 14 |

**TRUTH TABLE**

| ENABLE | DISABLE | FUNCTION |
|---|---|---|
| X | 0 | Convert CMOS Level to TTL Level |
| 1 | 1 | Convert TTL Level to CMOS Level |
| 0 | 1 | High Impedance (Z) |

0 = Low Level 1 = High Level X = Don't Care
Z = High Impedance on Both CMOS and TTL sides.

NOTE: An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-3374RH pins: A0 - 7.

The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.5mA at VDD/2 ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

* WARNING: Do not activate the Disable input by hardwiring to any TTL input pins. This is an incorrect mode of operation.

## Metallization Topology

**DIE DIMENSIONS:**

89.4 mils x 76.0 mils x 14 mils ±1 mil

**METALLIZATION:**

Type: AlSi

Thickness: 8kÅ ±1kÅ

**GLASSIVATION:**

Type: SiO2

Thickness: 11kÅ ±2kÅ

## Metallization Mask Layout

**HS-3374RH**