High Speed CMOS TTL Input – 74HCT163

Programmable 4–bit counter with synchronous reset in bare die form

Rev 1.0
06/06/19

Description

The 74HCT163 programmable synchronous 4-bit decade and binary counter is fabricated using a 2.5μm 5V CMOS process with the same high speed performance of LSTTL combined with CMOS low power consumption. Clock input is active on the rising edge. Both load ($\overline{\text{SPE}}$) and clear ($\overline{\text{MR}}$) inputs are active low. Presetting is synchronous on rising clock edge. Two enable inputs (TE and PE) and ripple carry output (TC) are provided to enable easy cascading of counters, facilitating simple implementation of N-bit counters without use of external gates. Device inputs directly accept LSTTL or CMOS. All inputs are protected against ESD and excess voltage transients.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1μA
- TTL / CMOS compatible Input Levels
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- Function compatible with 74LS163.

Ordering Information

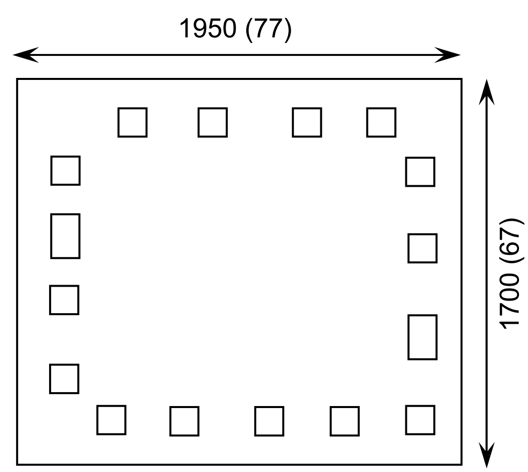
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability version of this product please see

54HCT163

Die Dimensions in μm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350μm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1950 x 1700 78 x 67	μm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	μm mils
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils
Top Metal Composition	Al 1%Si 1.1μm	
Back Metal Composition	N/A – Bare Si	

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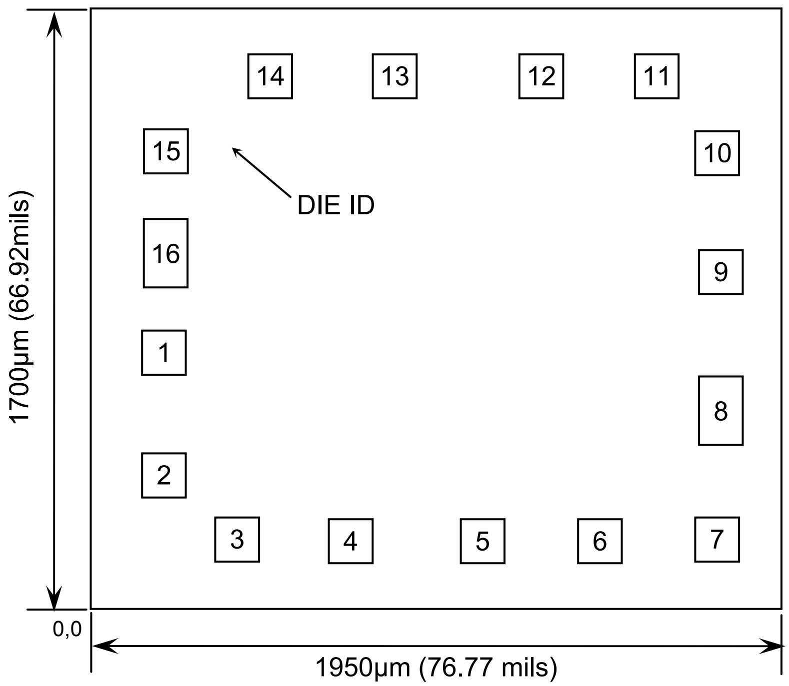
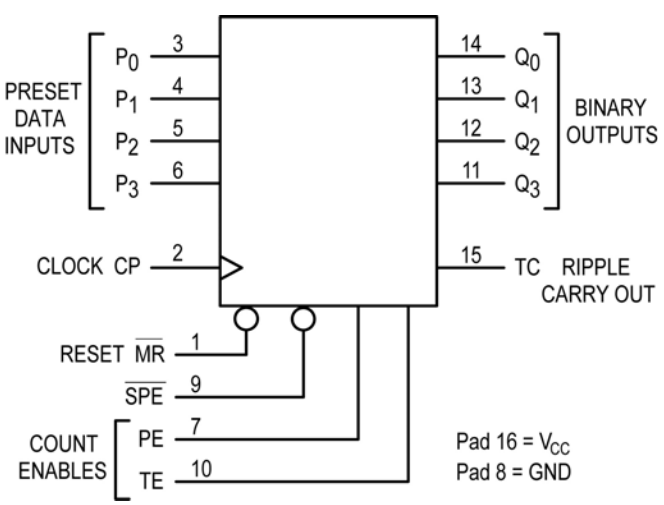
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{MR}$	0.145	0.655
2	CP	0.145	0.315
3	P0	0.350	0.135
4	P1	0.670	0.125
5	P2	1.045	0.125
6	P3	1.375	0.125
7	PE	1.698	0.135
8	GND	1.712	0.465
9	$\overline{SPE}$	1.712	0.885
10	TE	1.698	1.229
11	Q3	1.533	1.441
12	Q2	1.208	1.441
13	Q1	0.795	1.441
14	Q0	0.440	1.441
15	TC	0.155	1.227
16	V_{CC}	0.155	0.910
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Function Table

INPUTS					OUTPUT
CP	$\overline{MR}$	$\overline{SPE}$	PE	TE	Q
↑	L	X	X	X	RESET
↑	H	L	X	X	LOAD DATA
↑	H	H	H	H	COUNT
↑	H	H	L	X	NO COUNT
↑	H	H	X	L	NO COUNT

Function Description

INPUTS

Clock (CP - Pad 2)
The internal flip–flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions such as resetting and loading occur with the rising edge of the Clock Input.

Preset Data Inputs (P0, P1, P2, P3 - Pads 3, 4, 5, 6)
These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip–flops and appear at the counter outputs. P0 (Pad 3) is the least–significant bit and P3 (Pad 6) is the most–significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pads 14, 13, 12, 11)
These are the counter outputs. Q0 (Pad 14) is the least–significant bit and Q3 (Pad 11) is the most–significant bit.

Ripple-Carry Out (TC - Pad 15)
When the counter is in it's maximum state 1111, this output goes high, providing an external look–ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. Logic equation for this output is:

Ripple Carry Out (TC) = T Enable (TE) • Q0 • Q1 • Q2 • Q3

CONTROL FUNCTIONS

Reset (MR – Pad 1)
A low level on Reset resets the internal flip– flops & sets the outputs (Q0 through Q3) to a a low level. Reset is synchronous with the rising edge of the Clock input.

Synchronous Parallel Enable (SPE - Pad 9)
With the rising edge of the Clock, a low level on SPE loads the data from the Preset Data input pads (P0, P1, P2, P3) into the internal flip–flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Count Enable/Disable (PE and TE - Pads 7, 10)
The device has two count–enable control pins: P Enable P (PE) and T Enable (TE). The device counts when these two pads and the Data load pad are high. The logic equation is:

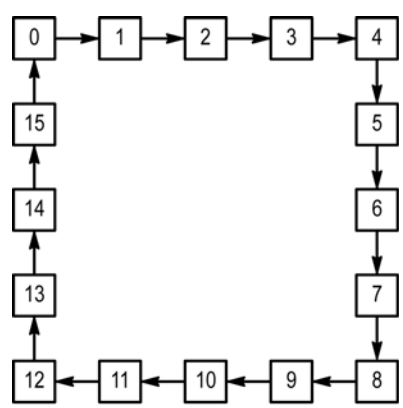
Count Enable = P Enable • T Enable • Data Load

The count is either enabled or disabled by the control inputs according to Figure 1. In general, P Enable (PE) is a count–enable control: T Enable (TE) is both a count–enable and a Ripple–Carry Output control.

Count Enable / Disable truth table

CONTROL INPUTS			RESULT AT OUTPUTS	
SPE	PE	TE	Q0-Q3	TC
H	H	H	COUNT	HIGH WHEN Q0–Q3 ARE MAX
L	H	H	NO COUNT	HIGH WHEN Q0–Q3 ARE MAX
X	L	H	NO COUNT	HIGH WHEN Q0–Q3 ARE MAX
X	X	L	NO COUNT	L
Q0 through Q3 are maximum when Q3 Q2 Q1 Q0 = 1111.				

Output State Diagram



BINARY COUNTERS

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_J	-40	+85	°C
Input Rise or Fall Times	t_r, t_f	-	500	ns

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V |I_{OUT}| ≤ 20µA	2.0	2.0	2.0	V
		5.5V		2.0	2.0	2.0	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V |I_{OUT}| ≤ 20µA	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 20µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 4.0mA	3.98	3.84	3.84	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 20µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 4.0mA	0.26	0.33	0.33	

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current[5]	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \le 0\mu A$	4	40	40	μA
Additional Quiescent Supply Current[5]	ΔI_{CC}	5.5V	V_{IN} = 2.4V, Any One Input. $V_{IN} = V_{CC}$ or GND, Other Inputs $I_{OUT} = 0\mu A$	**≥ -40°C** 2.9	**25°C to 85°C** 2.4		mA

4. $-40^{\circ}C \le T_J \le +85^{\circ}C$ **5.** Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency (50% Duty Cycle) (Figure 1, 3)	f_{MAX}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	30	24	24	MHz
Maximum Propagation Delay, CP to Q (Figure 1, 3)	t_{PLH}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	20	23	23	ns
	t_{PHL}			25	30	30	
Maximum Propagation Delay, TE to TC (Figure 1, 3)	t_{PLH}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	16	18	18	ns
	t_{PHL}			21	24	24	
Maximum Propagation Delay, CP to TC (Figure 1, 3)	t_{PLH}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	22	25	25	ns
	t_{PHL}			28	33	33	
Maximum Output Transition Time, Any Output (Figure 1, 3)	t_{TLH}, t_{THL}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	15	19	19	ns
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[6]	C_{PD}	5V	T_J = 25°C	**TYPICAL** 60			pF

6. Not production tested in die form, characterized by chip design and tested in package.
7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum Setup Time, Pn to CP	t_{SU}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	12	18	18	ns
Minimum Setup Time, $\overline{SPE}$ to CP				12	18	18	ns
Minimum Setup Time, $\overline{MR}$ to CP				12	18	18	ns
Minimum Setup Time, TE or PE to CP				12	18	18	ns
Minimum Hold Time, CP to Pn	t_h	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	3	3	3	ns
Minimum Hold Time, CP to SPE				3	3	3	
Minimum Hold Time, CP to MR				3	3	3	
Minimum Hold Time, CP to TE or PE				3	3	3	
Minimum Recovery Time, SPE Inactive to CP	t_{rec}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	12	17	17	ns
Minimum Pulse Width, CP	t_w	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	12	15	15	ns
Maximum Input Rise and Fall times	t_r, t_f	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	500	500	500	ns

Switching Waveforms

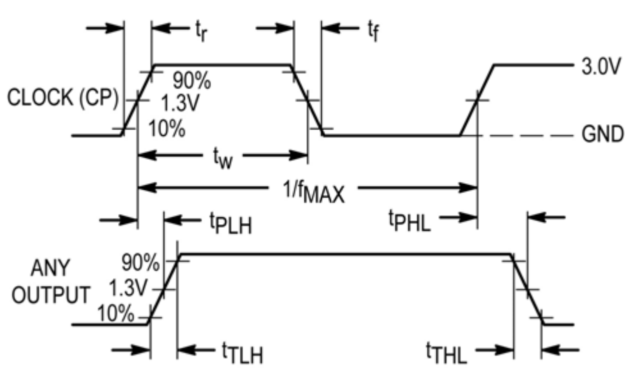


Figure 1 – Propagation Delay & Clock Timing, Clock to Output

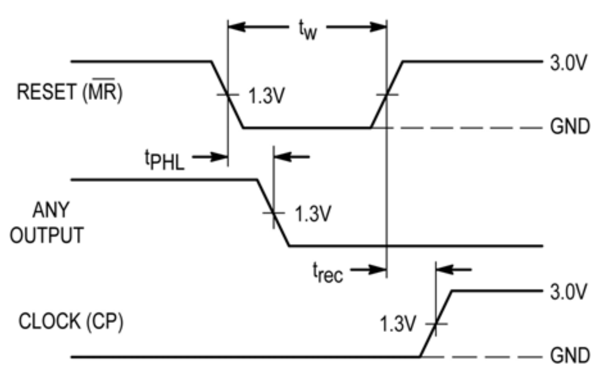


Figure 2 – Propagation Delay & Recovery Time, Reset to Clock

Switching Waveforms continued

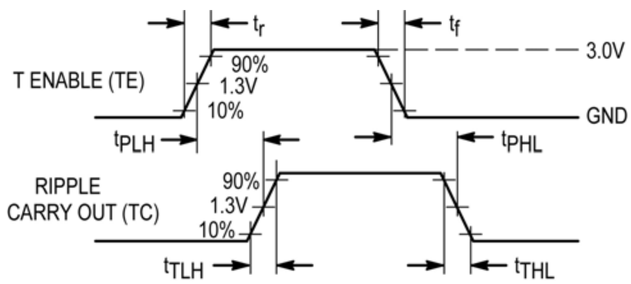


Figure 3 – Propagation Delay & Output Transition Time, Enable to Ripple Carry

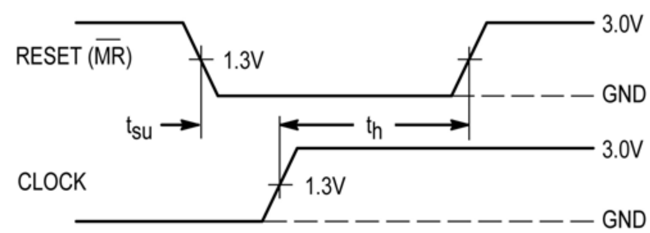


Figure 4 – Setup & Hold Timing, Reset to Clock

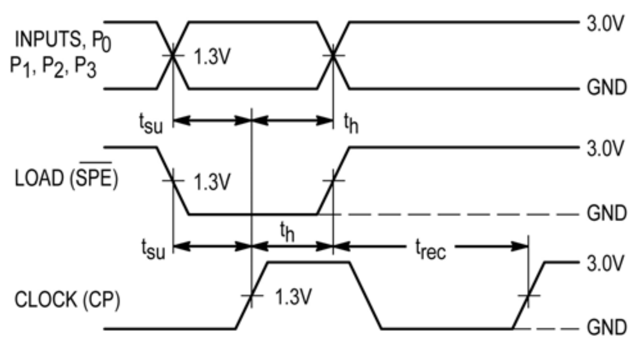


Figure 5 – Setup and Hold Timing, Data to Clock

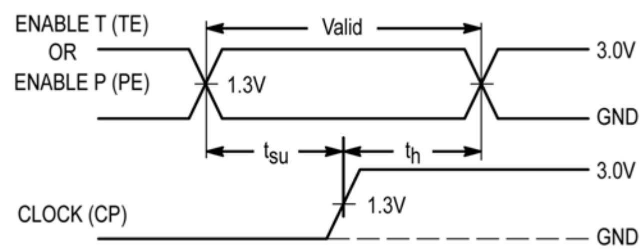
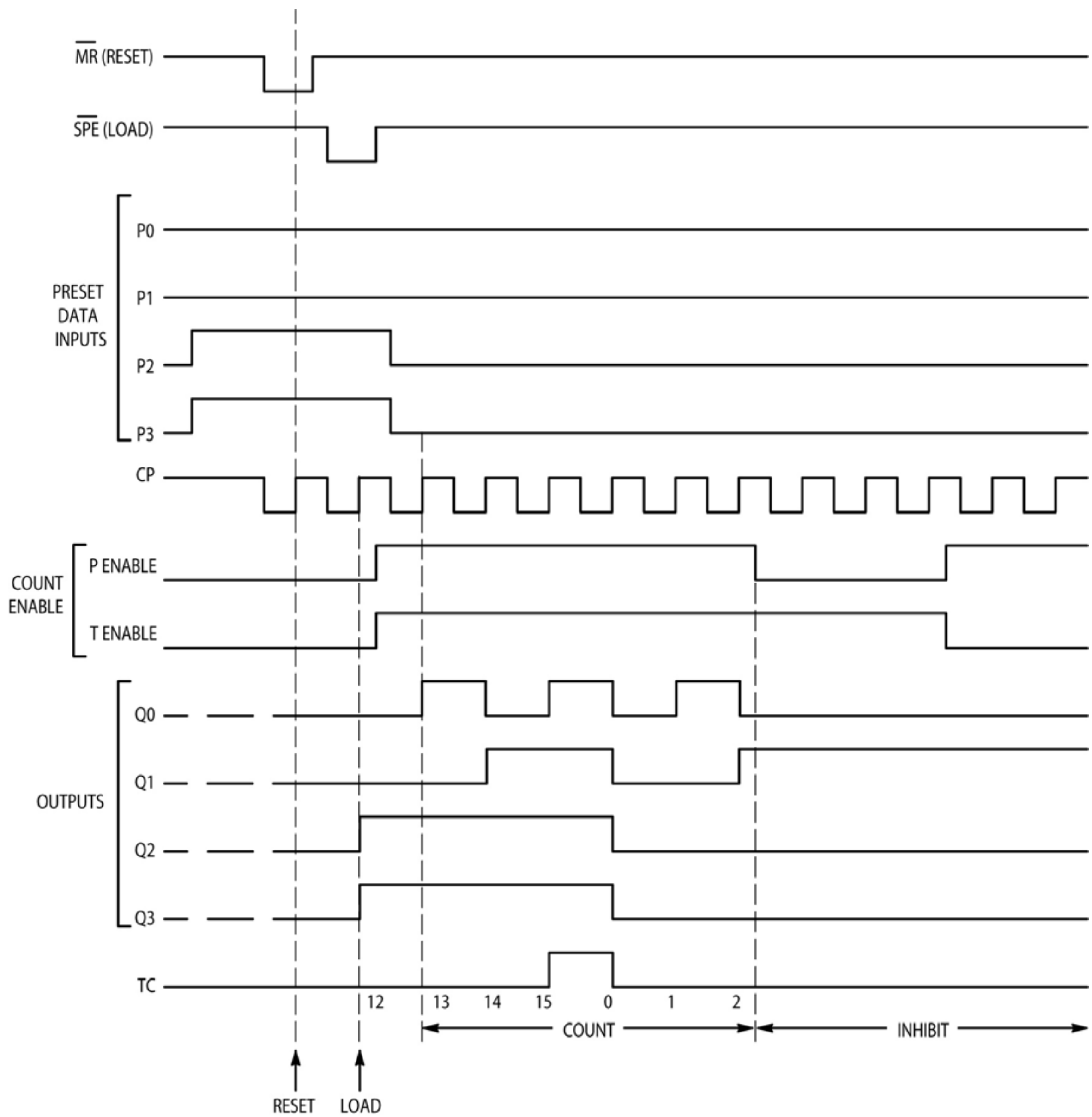
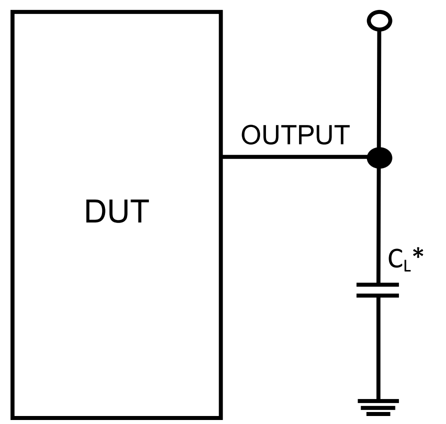


Figure 6 – Minimum Hold Time, Enable to Clock

Timing Diagram



Test Circuit



* Includes all probe and jig capacitance