

# Hex Inverter

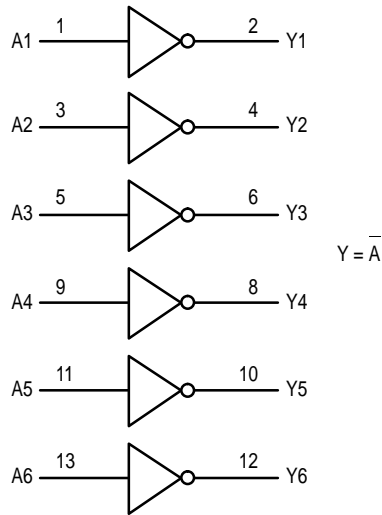
## High-Performance Silicon-Gate CMOS

The MC54/74HC04A is identical in pinout to the LS04 and the MC14069. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

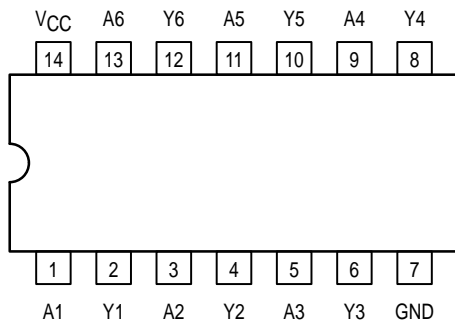
The device consists of six three-stage inverters.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 36 FETs or 9 Equivalent Gates

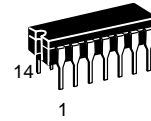
### LOGIC DIAGRAM



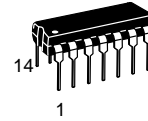
### Pinout: 14-Lead Packages (Top View)



# MC54/74HC04A



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-03



**DT SUFFIX**  
TSSOP PACKAGE  
CASE 948G-01

### ORDERING INFORMATION

|             |         |
|-------------|---------|
| MC54HCXXAJ  | Ceramic |
| MC74HCXXAN  | Plastic |
| MC74HCXXAD  | SOIC    |
| MC74HCXXADT | TSSOP   |

### FUNCTION TABLE

| Inputs | Outputs |
|--------|---------|
| A      | Y       |
| L      | H       |
| H      | L       |



# MC54/74HC04A

## MAXIMUM RATINGS\*

| Symbol    | Parameter  | Value                   | Unit |
|-----------|--|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)  | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins   | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air, Plastic or Ceramic DIP†<br>SOIC Package†<br>TSSOP Package†           | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature  | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>Plastic DIP, SOIC or TSSOP Package<br>Ceramic DIP | 260<br>300              | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max      | Unit |
|-------------------|--|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               |      |          | ns   |
|                   | $V_{CC} = 2.0 \text{ V}$                             | 0    | 1000     |      |
|                   | $V_{CC} = 4.5 \text{ V}$                             | 0    | 500      |      |
|                   | $V_{CC} = 6.0 \text{ V}$                             | 0    | 400      |      |

**DC CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Condition   | V <sub>CC</sub><br>V | Guaranteed Limit |       |        | Unit |
|-----------------|--|---|----------------------|------------------|-------|--------|------|
|                 |  |   |                      | -55 to 25°C      | ≤85°C | ≤125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA   | 2.0                  | 1.50             | 1.50  | 1.50   | V    |
|                 |  |   | 3.0                  | 2.10             | 2.10  | 2.10   |      |
|                 |  |   | 4.5                  | 3.15             | 3.15  | 3.15   |      |
|                 |  |   | 6.0                  | 4.20             | 4.20  | 4.20   |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA   | 2.0                  | 0.50             | 0.50  | 0.50   | V    |
|                 |  |   | 3.0                  | 0.90             | 0.90  | 0.90   |      |
|                 |  |   | 4.5                  | 1.35             | 1.35  | 1.35   |      |
|                 |  |   | 6.0                  | 1.80             | 1.80  | 1.80   |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20μA  | 2.0                  | 1.9              | 1.9   | 1.9    | V    |
|                 |  |   | 4.5                  | 4.4              | 4.4   | 4.4    |      |
|                 |  | 6.0   | 5.9                  | 5.9              | 5.9   |        |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0                  | 2.48             | 2.34  | 2.20   |      |
| 4.5             | 3.98   |   | 3.84                 | 3.70             |       |        |      |
| 6.0             | 5.48   |   | 5.34                 | 5.20             |       |        |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20μA  | 2.0                  | 0.1              | 0.1   | 0.1    | V    |
|                 |  |   | 4.5                  | 0.1              | 0.1   | 0.1    |      |
|                 |  | 6.0   | 0.1                  | 0.1              | 0.1   |        |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0                  | 0.26             | 0.33  | 0.40   |      |
| 4.5             | 0.26   |   | 0.33                 | 0.40             |       |        |      |
| 6.0             | 0.26   |   | 0.33                 | 0.40             |       |        |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 6.0                  | ± 0.1            | ± 1.0 | ± 1.0  | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0μA  | 6.0                  | 1.0              | 10    | 40     | μA   |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC CHARACTERISTICS** (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V | Guaranteed Limit |       |        | Unit |
|--|--|----------------------|------------------|-------|--------|------|
|  |  |                      | -55 to 25°C      | ≤85°C | ≤125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A or B to Output Y<br>(Figures 1 and 2) | 2.0                  | 75               | 95    | 110    | ns   |
|  |  | 3.0                  | 30               | 40    | 55     |      |
|  |  | 4.5                  | 15               | 19    | 22     |      |
|  |  | 6.0                  | 13               | 16    | 19     |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)          | 2.0                  | 75               | 95    | 110    | ns   |
|  |  | 3.0                  | 27               | 32    | 36     |      |
|  |  | 4.5                  | 15               | 19    | 22     |      |
|  |  | 6.0                  | 13               | 16    | 19     |      |
| C <sub>in</sub>                        | Maximum Input Capacitance  |                      | 10               | 10    | 10     | pF   |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Inverter)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |  | pF |
|-----------------|---|---|--|----|
|                 |   | 20                                      |  |    |
|                 |   |   |  |    |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

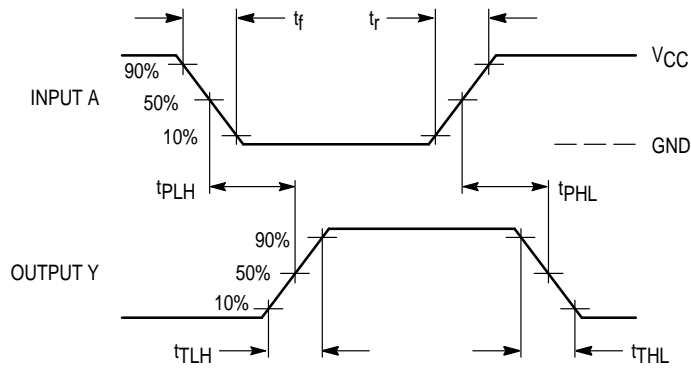
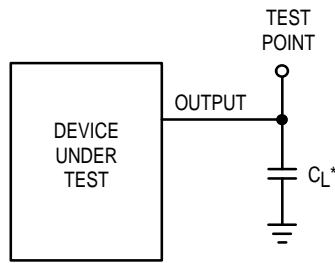


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

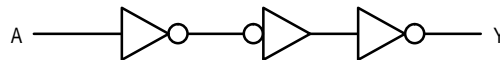
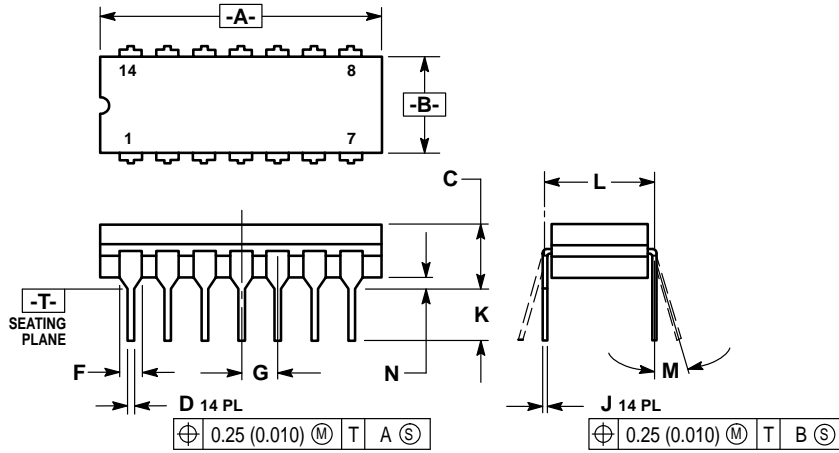


Figure 3. Expanded Logic Diagram  
(1/6 of the Device Shown)

OUTLINE DIMENSIONS

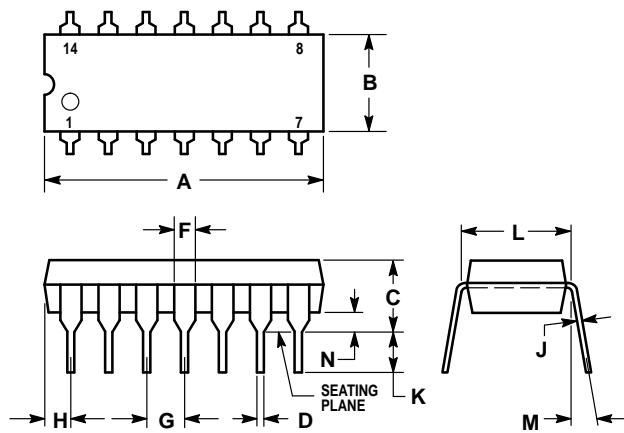
**J SUFFIX**  
 CERAMIC DIP PACKAGE  
 CASE 632-08  
 ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.750     | 0.785 | 19.05       | 19.94 |
| B   | 0.245     | 0.280 | 6.23        | 7.11  |
| C   | 0.155     | 0.200 | 3.94        | 5.08  |
| D   | 0.015     | 0.020 | 0.39        | 0.50  |
| F   | 0.055     | 0.065 | 1.40        | 1.65  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.125     | 0.170 | 3.18        | 4.31  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

**N SUFFIX**  
 PLASTIC DIP PACKAGE  
 CASE 646-06  
 ISSUE L



- NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.715     | 0.770 | 18.16       | 19.56 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.145     | 0.185 | 3.69        | 4.69  |
| D   | 0.015     | 0.021 | 0.38        | 0.53  |
| F   | 0.040     | 0.070 | 1.02        | 1.78  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.052     | 0.095 | 1.32        | 2.41  |
| J   | 0.008     | 0.015 | 0.20        | 0.38  |
| K   | 0.115     | 0.135 | 2.92        | 3.43  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 10°   | 0°          | 10°   |
| N   | 0.015     | 0.039 | 0.39        | 1.01  |



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