

1-70-01-07

# 54/74170 54LS/74LS170

4 X 4 REGISTER FILE  
(With Open-Collector Outputs)

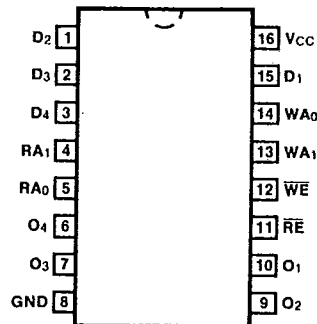
**DESCRIPTION** — The '170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 X 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '670 provides a similar function to this device but it features 3-state outputs.

- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BITS
- TYPICAL ACCESS TIME OF 20 ns
- LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION

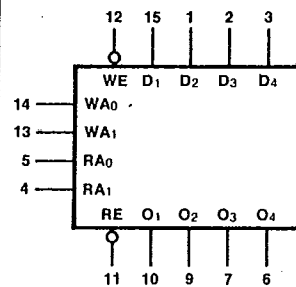
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74170PC, 74LS170PC		9B
Ceramic DIP (D)	A	74170DC, 74LS170DC	54170DM, 54LS170DM	7B
Flatpak (F)	A	74170FC, 74LS170FC	54170FM, 54LS170DM	4L

## CONNECTION DIAGRAM PINOUT A



## LOGIC SYMBOL



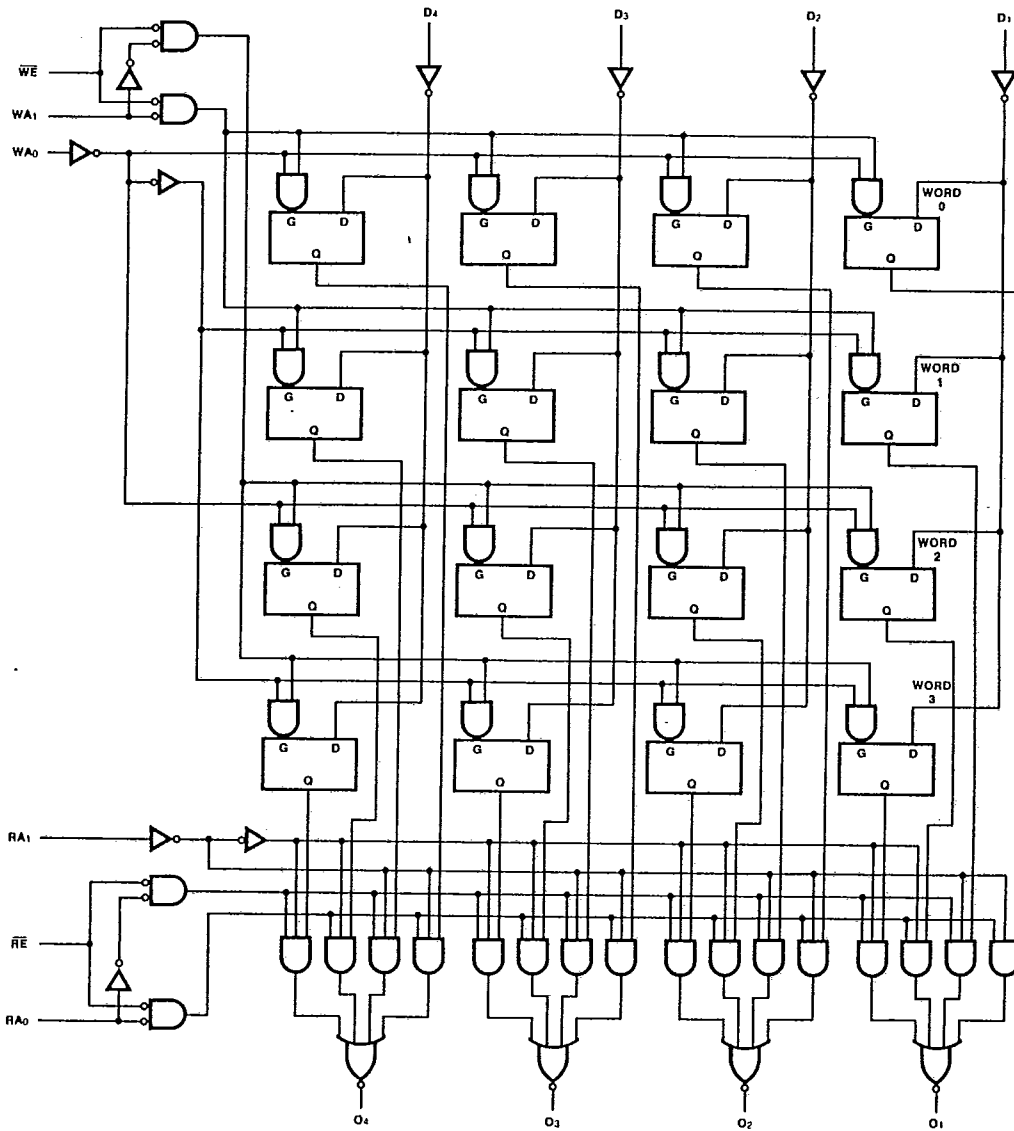
V<sub>CC</sub> = Pin 16  
GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D <sub>1</sub> — D <sub>4</sub>	Data Inputs	1.0/1.0	0.5/0.25
WA <sub>0</sub> , WA <sub>1</sub>	Write Address Inputs	1.0/1.0	0.5/0.25
WE	Write Enable Input (Active LOW)	1.0/1.0	1.0/0.5
RA <sub>0</sub> , RA <sub>1</sub>	Read Address Inputs	1.0/1.0	0.5/0.25
RE	Read Enable Input (Active LOW)	1.0/1.0	1.0/0.5
O <sub>1</sub> — O <sub>4</sub>	Data Outputs	OC*/10	OC*/5.0 (2.5)

\*OC — Open Collector

LOGIC DIAGRAM



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WRITE FUNCTION TABLE

WRITE INPUTS			D INPUTS TO
WE	WA1	WA0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

READ FUNCTION TABLE

READ INPUTS			OUTPUTS FROM
RE	RA1	RA0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = HIGH Voltage Level      L = LOW Voltage Level      X = Immaterial

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>OH</sub>	Output HIGH Current	30		20		μA	V <sub>CC</sub> = Min, V <sub>OH</sub> = 5.5 V
I <sub>CC</sub>	Power Supply Current	XC		40		mA	V <sub>CC</sub> = Max; D <sub>n</sub> , $\overline{WE}$ , $\overline{RE}$ = 4.5 V; W <sub>A<sub>n</sub></sub> , R <sub>A<sub>n</sub></sub> = Gnd
		XM		140			

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω			
		Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay* R <sub>A0</sub> or R <sub>A1</sub> to O <sub>n</sub>	35 40		35 35		ns	Figs. 3-1, 3-20
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{RE}$ to O <sub>n</sub>	15 30		30 30		ns	Figs. 3-1, 3-5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{WE}$ to O <sub>n</sub>	40 45		35 35		ns	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	30 45		35 35		ns	Figs. 3-1, 3-5

\*Measured at least 25 ns after entry of new data at selected location.

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t <sub>s</sub>	Setup Time HIGH or LOW D <sub>n</sub> to rising $\overline{WE}$	10		10		ns	Fig. a
t <sub>h</sub>	Hold Time HIGH or LOW D <sub>n</sub> to rising $\overline{WE}$	15		5.0		ns	
t <sub>s</sub>	Setup Time HIGH or LOW W <sub>A<sub>n</sub></sub> to falling $\overline{WE}$	15		10		ns	
t <sub>h</sub>	Hold Time HIGH or LOW W <sub>A<sub>n</sub></sub> to rising $\overline{WE}$	5.0		5.0		ns	
t <sub>w</sub> (L)	$\overline{WE}$ or $\overline{RE}$ Pulse Width LOW	25		25		ns	

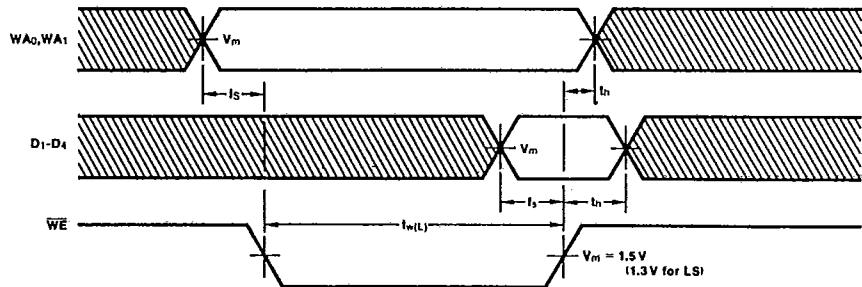


Fig. a