CMOS 8-STAGE SHIFT-AND-STORE BUS REGISTER

FEATURES:

- **3-state parallel outputs for connection to common bus**
- **Separate serial outputs synchronous to both positive and negative clock edges for cascading**
- **Medium speed operation—5 MHz at 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

APPLICATIONS

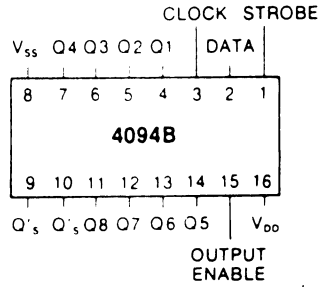
- **Serial-to-parallel data conversion**
- **Remote control holding register**
- **Dual-rank shift, hold, and bus applications**

DESCRIPTION:

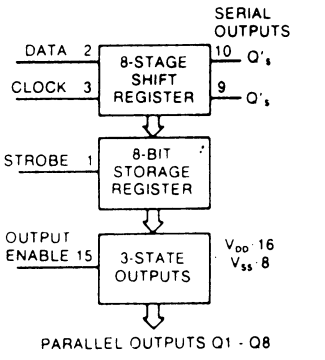
The 4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of 4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading 4094B devices when the clock rise time is slow.

CONNECTION DIAGRAM



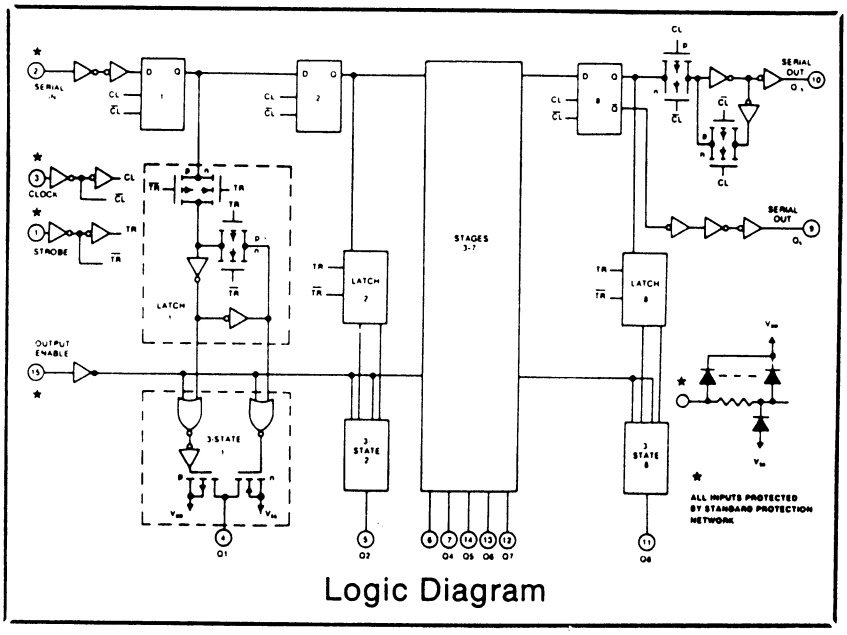
FUNCTIONAL DIAGRAM



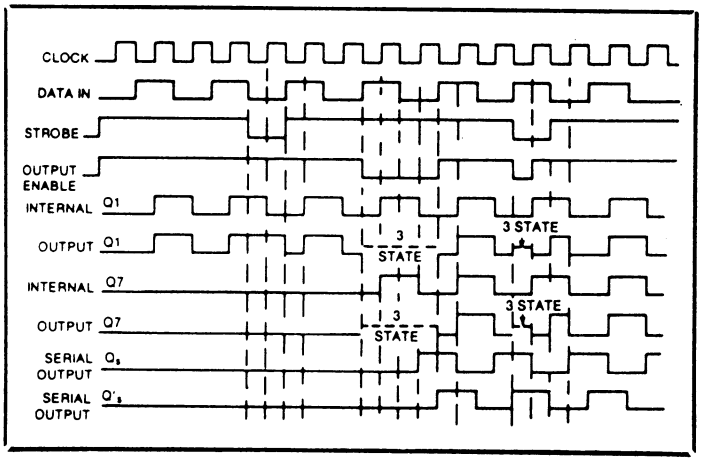
RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_s	5 10 15	125 55 35	— — —	ns
Clock Pulse Width, t_w	5 10 15	200 100 83	— — —	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.25 2.5 3	MHz
Clock Rise & Fall Time, t_rCL, t_fCL*	5, 10, 15	—	15	μs
Strobe Pulse Width, t_w	5 10 15	200 80 70	— — —	ns

*If more than one unit is cascaded t_fCL (for Q_s only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.



Logic Diagram



TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐	0	X	X	OC	OC	Q7	NC
⌐	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐	1	1	1	1	Q_{N-1}	Q7	NC
⌐	1	1	1	NC	NC	NC	Q7

▲ = Level Change Logic 1 ≡ High NC = No Change
X = Don't Care Logic 0 ≡ Low OC = Open Circuit

*At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_s output.

STATIC ELECTRICAL CHARACTERISTICS [1]

PARAMETER	V_{DD}	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT (I_{DD})	5	—	5	—	0.02	5	—	150	μA
	10	—	10	—	0.02	10	—	300	
	15	—	20	—	0.02	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT (I_{ZL})	15	—	±0.1	—	$\pm 10^{-4}$	±0.1	—	±1	μA

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = −55°C for C
= −40°C for E
T_{HIGH} = +125°C for C
= +85°C for E

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL PACKAGES			UNITS
		MIN.	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output (0's)	5	—	300	600	ns
	10	—	125	250	
	15	—	95	190	
Clock to Serial Output (0's)	5	—	230	460	ns
	10	—	110	220	
	15	—	75	150	
Clock to Parallel Output	5	—	420	840	ns
	10	—	195	390	
	15	—	135	270	
Strobe to Parallel Output	5	—	290	580	ns
	10	—	145	290	
	15	—	100	200	
Output Enable to Parallel Output: t_{PHL}	5	—	140	280	ns
	10	—	75	150	
	15	—	55	110	
t_{PLH}	5	—	225	450	ns
	10	—	95	190	
	15	—	70	140	
Minimum Strobe Pulse Width, t_W	5	—	100	200	ns
	10	—	40	80	
	15	—	35	70	
Minimum Clock Pulse Width, t_W	5	—	100	200	ns
	10	—	50	100	
	15	—	40	83	
Minimum Data Setup Time, t_s	5	—	60	125	ns
	10	—	30	55	
	15	—	20	35	
Transition Time; t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Clock Rise and Fall Time; t_r, t_f	5, 10, 15	—	—	15	μs
Max. Clock Input Frequency, f_{CL}	5	1.25	2.5	—	MHz
	10	2.5	5	—	
	15	3	6	—	
Average Input Capacitance, C_I (Any Input)	—	—	5	—	pF