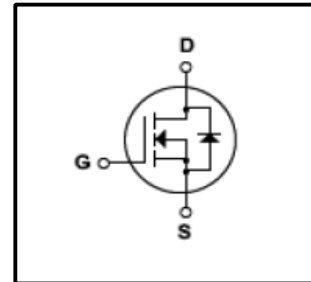


Silicon N-Channel MOSFET

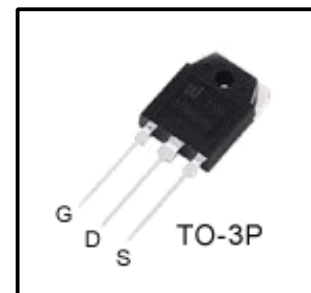
Features

- 18A,500V, $R_{DS(on)}$ (Max0.265 Ω)@ $V_{GS}=10V$
- Ultra-low Gate charge(Typical 42nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150 $^{\circ}C$)



General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, VDMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This device is specially well suited for AC-DC switching power supplies, DC-DC power converters, high voltage H-bridge motor drive PWM.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	500	V
I_D	Continuous Drain Current(@ $T_c=25^{\circ}C$)	18	A
	Continuous Drain Current(@ $T_c=100^{\circ}C$)	12.7	A
I_{DM}	Drain Current Pulsed (Note1)	80	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	330	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	27.7	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	4.5	V/ ns
P_D	Total Power Dissipation(@ $T_c=25^{\circ}C$)	280	W
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^{\circ}C$
T_L	Channel Temperature	300	$^{\circ}C$

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	0.45	$^{\circ}C/W$
R_{QCS}	Thermal Resistance , Case-to-Sink	-	0.24	-	$^{\circ}C/W$
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	40	$^{\circ}C/W$

Electrical Characteristics(Tc=25°C)

Characteristics		Symbol	Test Condition	Min	Type	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 10	nA
Gate-source breakdown voltage		$V_{(BR)GSS}$	$I_G=\pm 10 \mu A, V_{DS}=0V$	± 30	-	-	V
Drain cut-off current		I_{DSS}	$V_{DS}=500V, V_{GS}=0V$	-	-	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D=10 mA, V_{GS}=0V$	500	-	-	V
Breakdown voltage Temperature coefficient		$\Delta BV_{DSS}/\Delta T_J$	$I_D=250 \mu A$, Referenced to 25°C	-	0.5	-	V/°C
Gate threshold voltage		$V_{GS(th)}$	$V_{DS}=10V, I_D=1mA$	2	-	4	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$	-	0.225	0.265	Ω
Forward Transconductance		g_{fs}	$V_{DS}=40V, I_D=10A$	-	16	-	S
Input capacitance		C_{iss}	$V_{DS}=25V,$	-	2530	3290	pF
Reverse transfer capacitance		C_{rss}	$V_{GS}=0V,$	-	11	14.3	
Output capacitance		C_{oss}	$f=1MHz$	-	300	390	
Switching time	Rise time	t_r	$V_{DD}=250V,$	-	40	90	ns
	Turn-on time	t_{on}	$I_D=18A$	-	150	310	
	Fall time	t_f	$R_G=25\Omega$	-	95	200	
	Turn-off time	t_{off}	(Note4,5)	-	110	230	
Total gate charge(gate-source plus gate-drain)		Q_g	$V_{DD}=400V,$ $V_{GS}=10V,$	-	42	55	nC
Gate-source charge		Q_{gs}	$I_D=18A$	-	12	-	
Gate-drain("miller") Charge		Q_{gd}	(Note4,5)	-	14	-	

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I_{DR}	-	-	-	18	A
Pulse drain reverse current	I_{DRP}	-	-	-	27	A
Forward voltage(diode)	V_{DSF}	$I_{DR}=18A, V_{GS}=0V$	-	-	-1.9	V
Reverse recovery time	t_{rr}	$I_{DR}=18A, V_{GS}=0V,$	-	1.6	-	ns
Reverse recovery charge	Q_{rr}	$di_{DR} / dt \leq 100 A / \mu s$	-	20	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=1.83mH $I_{AS}=18A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ C$

3. $I_{SD} \leq 18A, di/dt \leq 200A/\mu s, V_{DD} < BV_{DSS}$, STARTING $T_J=25^\circ C$

4.Pulse Test:Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

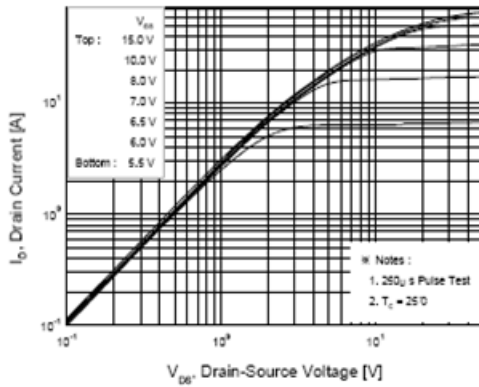


Fig.1 On State Characteristics

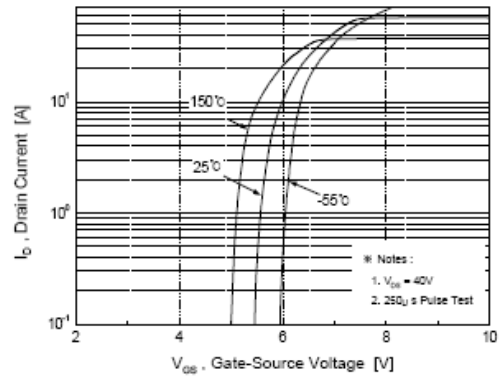


Fig.2 Transfer Current Characteristics

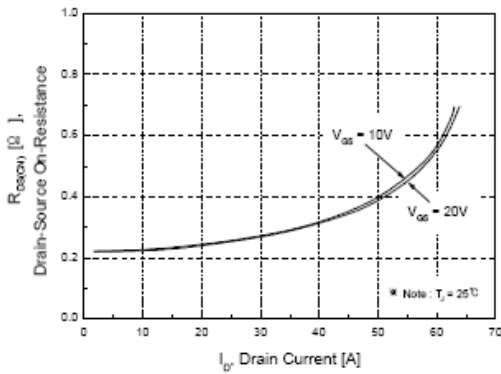


Fig.3 On-Resistance Variation vs Drain Current

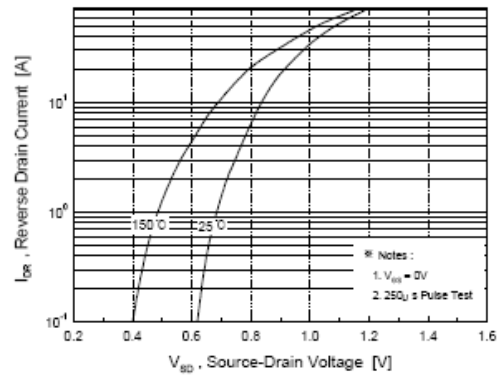


Fig.4 Body Diode Forward Voltage Variation with Source Current and Temperature

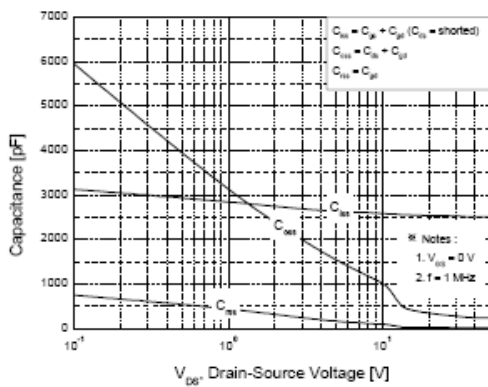


Fig.5 Capacitance Characteristics

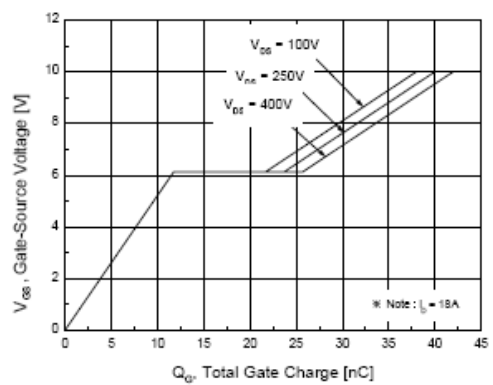


Fig.6 Gate Charge Characteristics

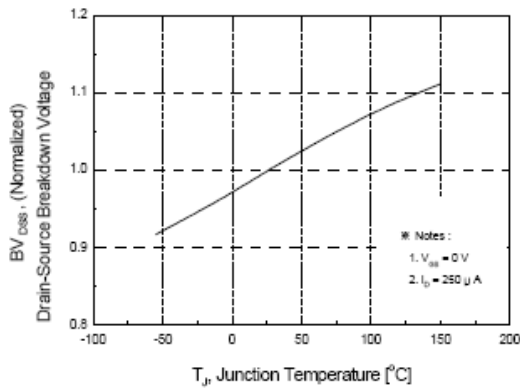


Fig.7 Breakdown Voltage Variation

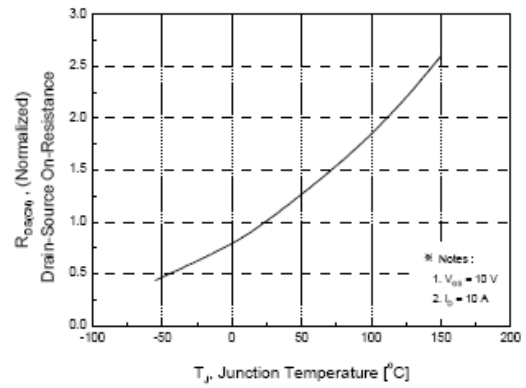


Fig.8 On-Resistance Variation vs. Temperature

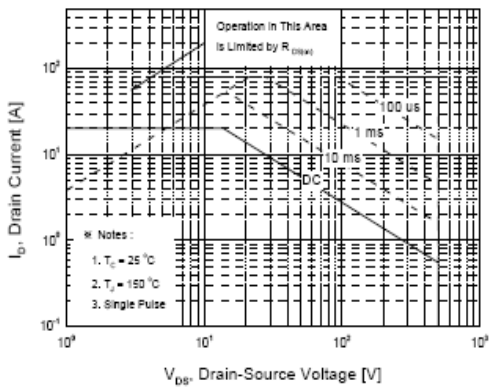


Fig.9 Maximum Safe Operation Area

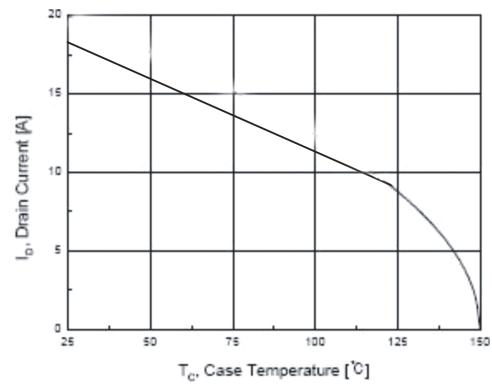


Fig.10 Maximum Drain Current vs Case Temperature

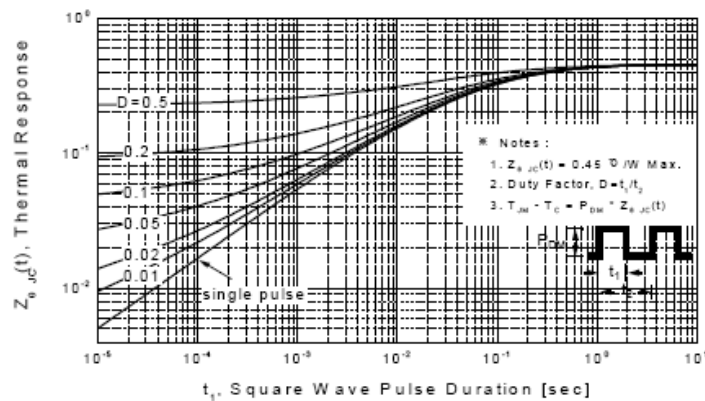


Fig.11 Transient Thermal Response Curve

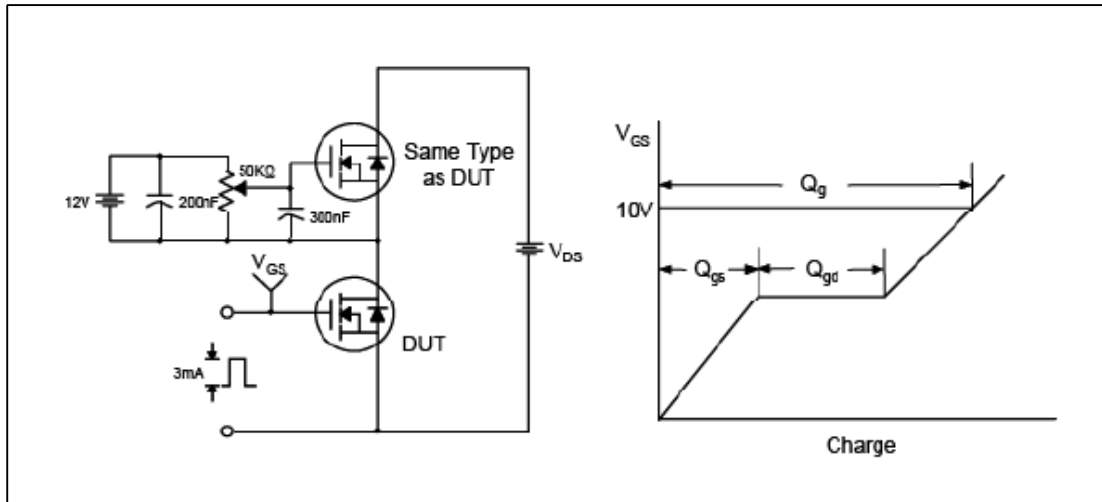


Fig.12 Gate Test Circuit & Waveform

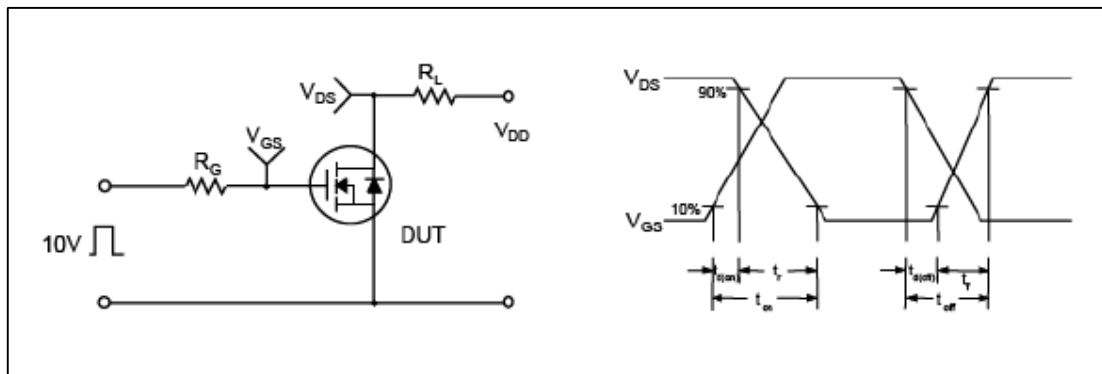


Fig.13 Resistive Switching Test Circuit & Waveform

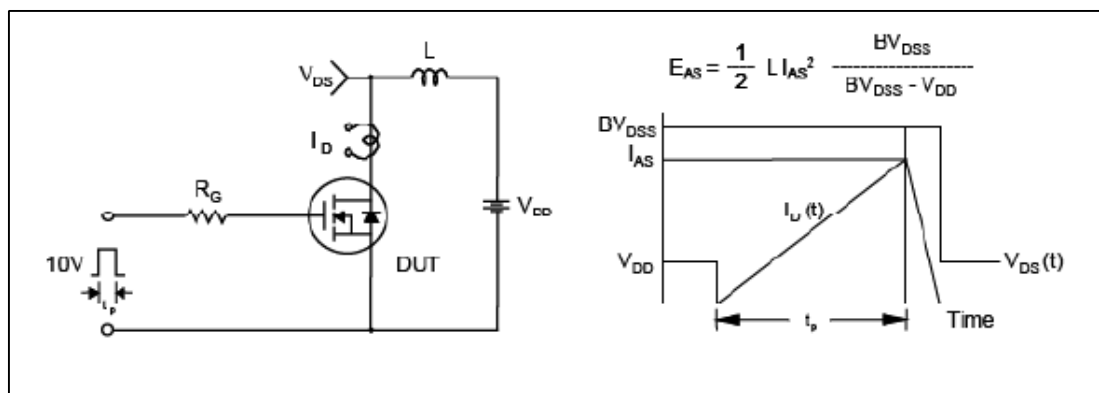


Fig.14 Unclamped Inductive Switching Test Circuit & Waveform

TO-3P Package Dimension

