

## N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

### Description

The 2N6786 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6786 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

### Features

- 1.25A, 400V
- $r_{DS(on)} = 3.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

### Absolute Maximum Ratings ( $T_C = +25^\circ\text{C}$ ) Unless Otherwise Specified

	2N6786	UNITS
Drain-Source Voltage .....	400*	V
Drain-Gate Voltage ( $R_{GS} = 20k\Omega$ ) .....	400*	V
Continuous Drain Current		A
$T_C = +25^\circ\text{C}$ .....	1.25*	A
$T_C = +100^\circ\text{C}$ .....	0.8*	A
Pulsed Drain Current .....	5.5*	A
Gate-Source Voltage .....	$\pm 20^*$	V
Continuous Source Current .....	1.25*	A
Pulse Source Current .....	5.5*	A
Maximum Power Dissipation		W
$T_C = +25^\circ\text{C}$ (See Figure 14) .....	15*	W
Above $T_C = +25^\circ\text{C}$ , Derate Linearly (See Figure 14) .....	0.12*	W/ $^\circ\text{C}$
Inductive Current, Clamped .....	5.5	A
(L = 100 $\mu\text{H}$ )		
Operating and Storage Junction Temperature Range .....	-55 to +150*	$^\circ\text{C}$
Maximum Lead Temperature for Soldering .....	300*	$^\circ\text{C}$
(0.083" (1.8mm) from case for 10s)		



**ELECTRICAL CHARACTERISTICS at  $T_c = 25^\circ\text{C}$  (Unless Otherwise Specified)**

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$BV_{DSS}$ $V_{GS} = 0\text{ V}, I_D = 0.25\text{ mA}$	400*	—	—	V	
Gate Threshold Voltage	$V_{GS(th)}$ $V_{GS} = V_{DS}, I_D = 0.5\text{ mA}$	2.0*	—	4.0*		
Gate-Source Leakage Forward	$I_{GSS}$ $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	100*	nA	
Gate-Source Leakage Reverse	$I_{GSS}$ $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	—	—	100*		
Zero-Gate Voltage Drain Current	$I_{DSS}$ $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	—	—	250*	$\mu\text{A}$	
	$I_{DSS}$ $V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_c = 125^\circ\text{C}$	—	—	1000*		
On-State Voltage <sup>§</sup>	$V_{DS(on)}$ $V_{GS} = 10\text{ V}, I_D = 1.25\text{ A}$	—	—	4.5*	V	
Static Drain-Source On-State Resistance <sup>§</sup>	$r_{DS(on)}$ $V_{GS} = 10\text{ V}, I_D = 0.8\text{ A}, T_A = 25^\circ\text{C}$	—	3.3	3.6*	$\Omega$	
	$r_{DS(on)}$ $V_{GS} = 10\text{ V}, I_D = 0.8\text{ A}, T_A = 125^\circ\text{C}$	—	—	7.92*		
Diode Forward Voltage <sup>§</sup>	$V_{SD}$ $T_c = 25^\circ\text{C}, I_S = 1.25\text{ A}, V_{GS} = 0\text{ V}$	0.6*	—	1.4*	V	
Forward Transconductance <sup>§</sup>	$g_{fs}$ $V_{DS} = 5\text{ V}, I_D = 0.8\text{ A}$	0.7*	1.2	2.1*	S(V)	
Input Capacitance	$C_{iss}$ $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ See Fig. 10	60*	135	200*	pF	
Output Capacitance		15*	35	50*		
Reverse Transfer Capacitance		2*	8	15*		
Turn-On Delay Time		$t_d(on)$ $V_{DD} \cong 170\text{ V}, I_D = 0.8\text{ A}, Z_o = 50\ \Omega$ See Fig. 15. (MOSFET switching times are essentially independent of operating temperature.)	—	—		15*
Rise Time	$t_r$	—	—	20*		
Turn-Of Delay Time	$t_d(off)$	—	—	35*		
Fall Time	$t_f$	—	—	30*		
Safe Operating Area	SOA	$V_{DS} = 200\text{ V}, I_D = 75\text{ mA}$ , See Fig. 16.	15	—	—	W
		$V_{DS} = 12\text{ V}, I_D = 1.25\text{ A}$ , See Fig. 16.	15	—	—	

**THERMAL RESISTANCE**

Junction-to-Case	$R_{\theta jc}$	—	—	8.33*	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta ja}$	Free Air Operation		175	

**SOURCE-DRAIN DIODE SWITCHING CHARACTERISTICS (TYPICAL)**

Reverse Recovery Time	$t_{rr}$	$T_J = 150^\circ\text{C}, I_F = 1.25\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	380	ns
Reverse Recovered Charge	$Q_{RR}$	$T_J = 150^\circ\text{C}, I_F = 1.25\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	2.7	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$ .		

\*JEDEC registered value.

§Pulse Test: Pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .