

# SCRs

## 1.25 Amp, Planar

2N1870A-2N1874A. J

### FEATURES

- Available as Either "JAN" or Standard Types
- Operating D.C. Current Range: 5 to 1250mA
- Pulse Currents: to 30A
- Voltage Ratings: to 200V
- Maximum Trigger Current: 0.2mA
- Maximum Trigger Voltage: 0.8V
- All Leads Isolated from Case
- Maximum  $\theta_{J-C}$ : 20°C/W

### DESCRIPTION

These are premium PNP controlled switches intended for use in applications requiring a high degree of reliability assurance. The JAN types are specified under MIL-S-19500/198, and are included in MIL-STD-701 as recommended types for military usage.

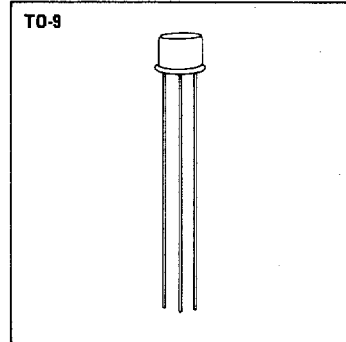
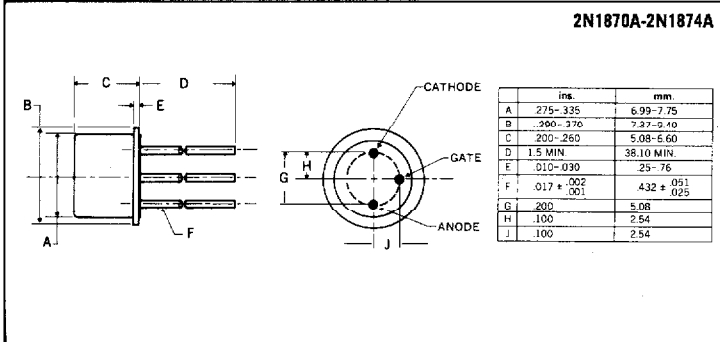
This series is useful in a wide variety of applications including: safety, arming and detonating circuits; timing and programming circuits; protective and warning circuits; driving relays; driving indicator lamps, encoding and decoding circuits; replacing relays, thyatrons, and megamps; servo motor control; pulse generation; plus many others.

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### ABSOLUTE MAXIMUM RATINGS

	2N1870A JAN2N1870A	2N1871A JAN2N1871A	2N1872A JAN2N1872A	2N1873A	2N1874A JAN2N1874A
Repetitive Peak Off-State Voltage, $V_{DRM}$	30V	60V	100V	150V	200V
Repetitive Peak Reverse Voltage, $V_{RRM}$	30V	60V	100V	150V	200V
D.C. On-State Current, $I_T$					
100°C Ambient			250mA		
100°C Case			1.25A		
Repetitive Peak On-State Current, $I_{TRM}$			up to 30A		
Peak One Cycle Surge (Non-Rep.) On-State Current, $I_{TSM}$			15A		
Peak Gate Current, $I_{GM}$			250mA		
Average Gate Current, $I_{C(AV)}$			25mA		
Reverse Gate Voltage, $V_{GR}$			5V		
Thermal Resistance, Junction to Case, $R\theta_{J-C}$			20°C/W		
Operating and Storage Temperature Range			-65°C to +150°C		

### MECHANICAL SPECIFICATIONS



**ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†**

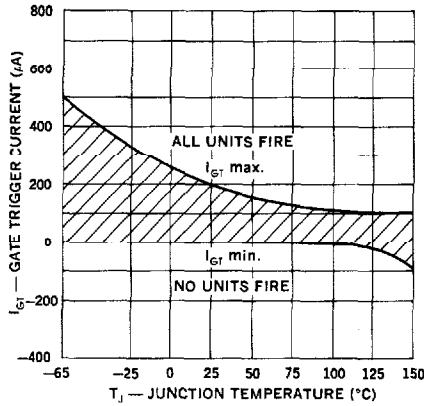
Test	Symbol	Min.	Typical	Max.	Units	Test Conditions
<b>Subgroup 1 (Visual and Mechanical)</b>						
<b>Subgroup 2 (25°C Tests)</b>						
Off-State Current	$I_{DRM}$	—	0.5	10	$\mu A$	$R_{GK} = 1K, V_{DRM} = + \text{Rating}$
Reverse Current	$I_{RRM}$	—	0.5	10	$\mu A$	$R_{GK} = 1K, V_{RRM} = - \text{Rating}$
Gate Trigger Voltage	$V_{GT}$	0.4	0.55	0.8	V	$R_{GS} = 100 \text{ ohms}, V_D = 5V$
Gate Trigger Current	$I_{GT}$	—	30	200	$\mu A$	$R_{GS} > 10K \text{ ohms}, V_D = 5V$
On-State Voltage	$V_{TM}$	—	1.8	2.5	V	$I_{TM} = 2A \text{ (pulse test)}$
Off-State Voltage — Critical of Rise	$dv_c/dt$	100	—	—	V/ $\mu s$	Specified test circuit
Reverse Gate Current	$I_{GR}$	—	0.5	10	$\mu A$	$V_{GRM} = 5V, \text{ anode open}$
Holding Current	$I_H$	0.3	—	5.0	mA	$I_G = -150\mu A, V_D = 5V$
<b>Subgroup 3 (125°C Tests)</b>						
High Temp. Off-State Current	$I_{DRM}$	—	15	100	$\mu A$	$R_{GK} = 1K, V_{DRM} = + \text{Rating}$
High Temp. Reverse Current	$I_{RRM}$	—	15	100	$\mu A$	$R_{GK} = 1K, V_{RRM} = - \text{Rating}$
High Temp. Gate Non-Trigger Voltage	$V_{GD}$	0.2	—	—	V	$R_{GS} = 100 \text{ ohms}, V_D = 5V$
High Temp. Holding Current	$I_H$	0.2	—	—	mA	$I_G = -150\mu A, V_D = 5V$
<b>Subgroup 4 (-65°C Tests)</b>						
Low Temp. Gate Trigger Voltage	$V_{GT}$	—	—	1.0	V	$R_{GK} = 100 \text{ ohms}, V_D = 5V$
Low Temp. Gate Trigger Current	$I_{GT}$	—	—	500	$\mu A$	$R_{GK} > 10K \text{ ohms}, V_D = 5V$
Low Temp. Holding Current	$I_H$	—	—	15	mA	$I_G = -150\mu A, V_D = 5V$

†All values in this table are JEDEC registered.

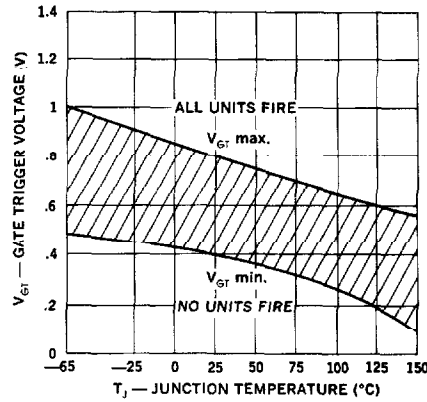
Note: Voltage ratings apply over the full operating temperature range, provided the gate is connected to the cathode through a resistor, 1 K or smaller, or other adequate gate bias is used.

**Triggering and Bias Stabilization**

1. Gate Trigger Current



2. Gate Trigger Voltage



ELECTRICAL SPECIFICATIONS (at 25°C unless noted)†

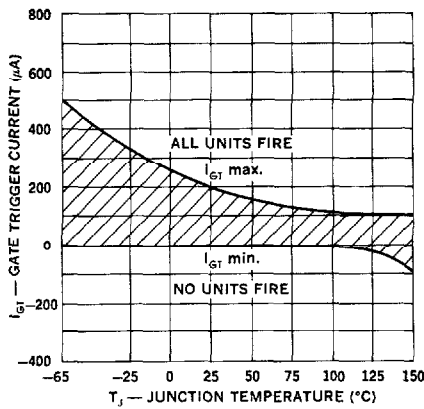
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Gate Trigger Voltage	$V_{GT}$	0.4	0.55	0.8	V	$R_{GK} = 100 \text{ ohms}, V_D = 5V$
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On-State Voltage	$V_{TM}$	—	1.8	2.5	V	$I_{TM} = 2A \text{ (pulse test)}$
Off-State Voltage — Critical of Rise	$dv_V/dt$	100	—	—	V/ $\mu s$	Specified test circuit
Reverse Gate Current	$I_{GR}$	—	0.5	10	$\mu A$	$V_{GRM} = 5V, \text{ anode open}$
Holding Current	$I_H$	0.3	—	5.0	mA	$I_G = -150\mu A, V_D = 5V$
<b>Subgroup 3 (125°C Tests)</b>						
High Temp. Off-State Current	$I_{DRM}$	—	15	100	$\mu A$	$R_{GK} = 1K, V_{DRM} = + \text{Rating}$
High Temp. Reverse Current	$I_{RRM}$	—	15	100	$\mu A$	$R_{GK} = 1K, V_{RRM} = - \text{Rating}$
High Temp. Gate Non-Trigger Voltage	$V_{GD}$	0.2	—	—	V	$R_{GS} = 100 \text{ ohms}, V_D = 5V$
High Temp. Holding Current	$I_H$	0.2	—	—	mA	$I_G = -150\mu A, V_D = 5V$
<b>Subgroup 4 (-65°C Tests)</b>						
Low Temp. Gate Trigger Voltage	$V_{GT}$	—	—	1.0	V	$R_{GK} = 100 \text{ ohms}, V_D = 5V$
Low Temp. Gate Trigger Current	$I_{GT}$	—	—	500	$\mu A$	$R_{GK} > 10K \text{ ohms}, V_D = 5V$
Low Temp. Holding Current	$I_H$	—	—	15	mA	$I_G = -150\mu A, V_{AA} = 5V$

†All values in this table are JEDEC registered.

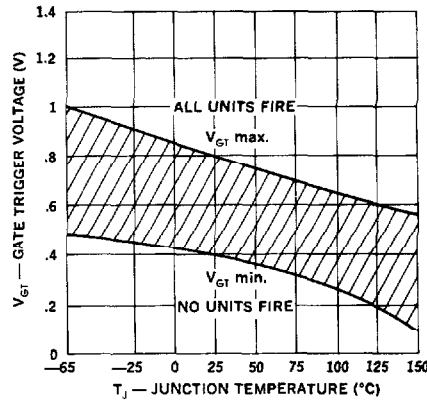
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Triggering and Bias Stabilization

1. Gate Trigger Current

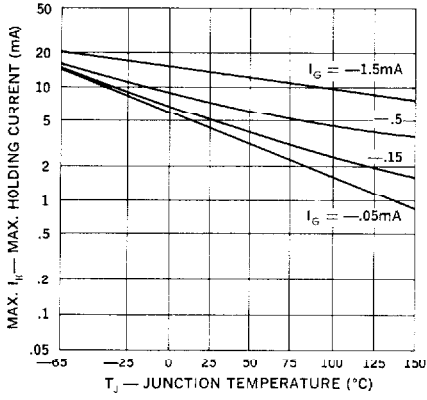


2. Gate Trigger Voltage

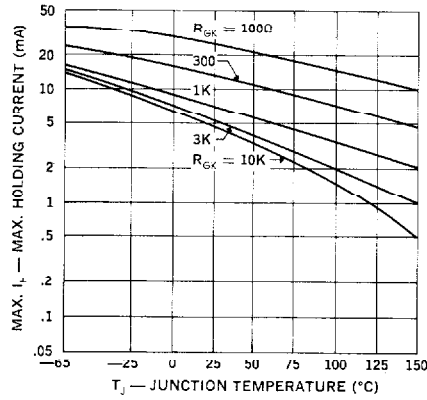


**Holding Current**

**1. Max. Holding Current (Current Bias)**

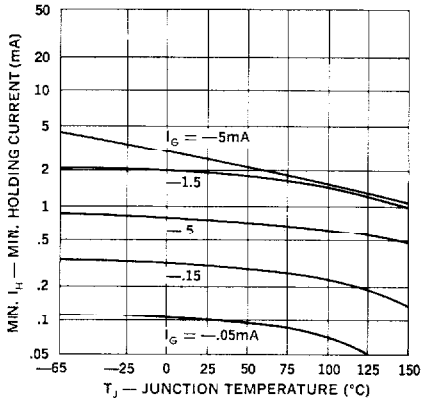


**2. Max. Holding Current (Resistor Bias)**

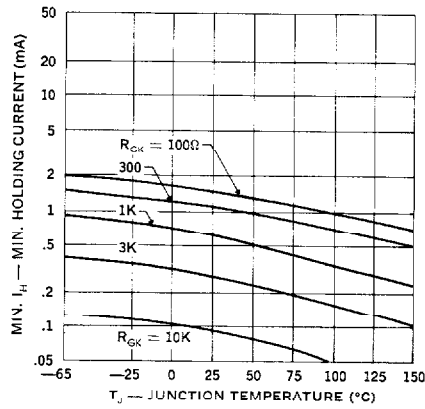


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**3. Min. Holding Current (Current Bias)**

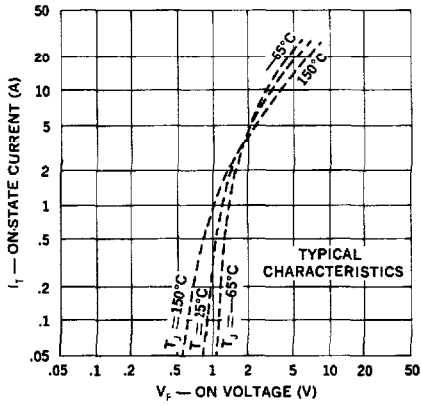


**4. Min. Holding Current (Resistor Bias)**

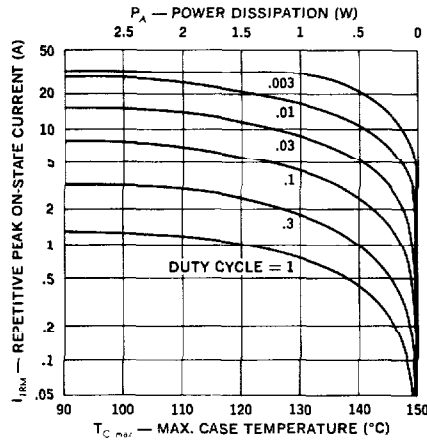


**Current Ratings — Thermal Design**

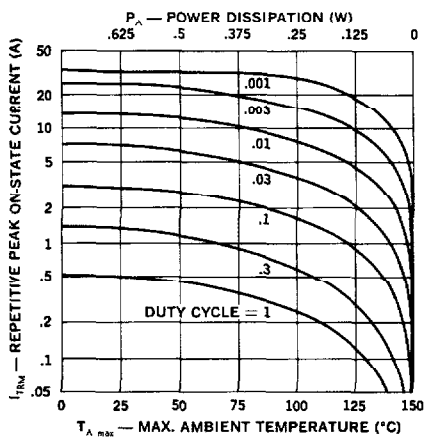
**1. On-State Current vs. Voltage**



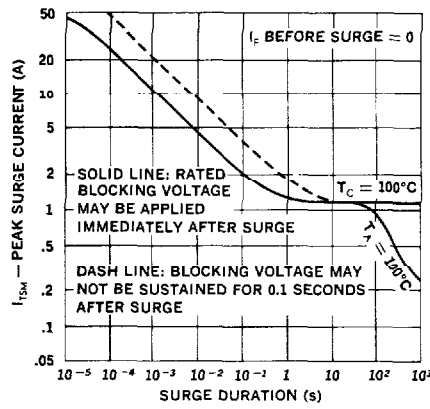
**2. Peak Current vs. Case Temperature**



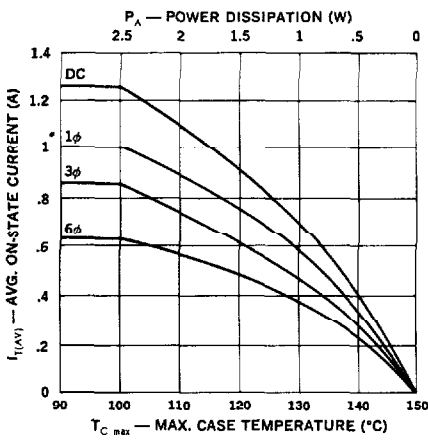
**3. Peak Current vs. Ambient Temperature**



**4. Surge Current vs. Time**



**5. Average Current vs. Case Temperature**



**6. Average Current vs. Ambient Temperature**

