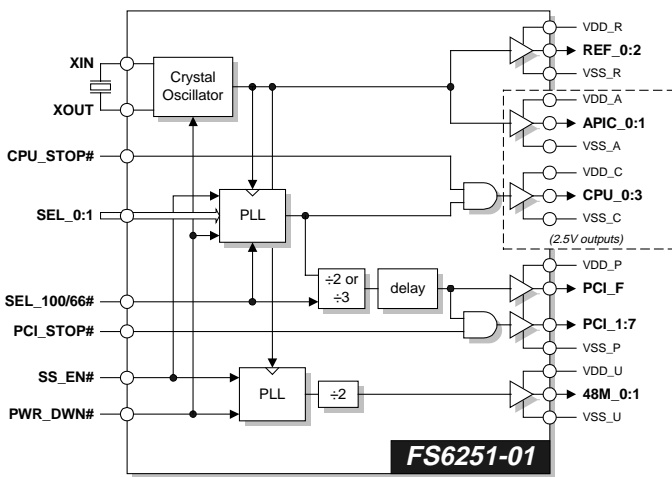


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1.0 Features

- Generates clocks required for Intel Pentium® II based systems, including:
 - Four enabled 2.5V 100MHz or 66MHz CPU system bus clock outputs
 - Seven enabled 3.3V PCI bus clocks and one free-running PCI clock
 - Three 3.3V REF clocks at 14.318MHz
 - Two 2.5V APIC clocks at 14.318MHz for APIC bus timing
 - Two 3.3V 48MHz clocks for 4x Universal Serial Bus (USB) timing
- Non-linear spread spectrum modulation (-0.5% at 31.5kHz)
- Selectable 100MHz or 66MHz system bus clock
- Supports Intel Test Mode and tristate output control to facilitate board testing
- Synchronous clocks skew-matched to <175ps on CPU and APIC buffers and <250ps on PCI buffers
- Separate CPU-enable, PCI-enable and power-down inputs with glitch-free stop clock controls on all clocks for clock control and power management
- All inputs and 3.3V outputs are LVTTL-compatible

Figure 1: Block Diagram (FS6251)



2.0 Description

The FS6251-01 is a CMOS clock generator IC designed for high-speed motherboard applications. Two different frequencies can be selected for the CPU and PCI clocks via two SEL pins. Glitch-free stop clock control of the CPU and PCI clocks is provided. A low current power-down mode is available for mobile applications. Separate clock buffers provide for a 2.5V voltage range on the CPU_0:3 and APIC_0:1 clocks.

Figure 2: Pin Configuration (FS6251)

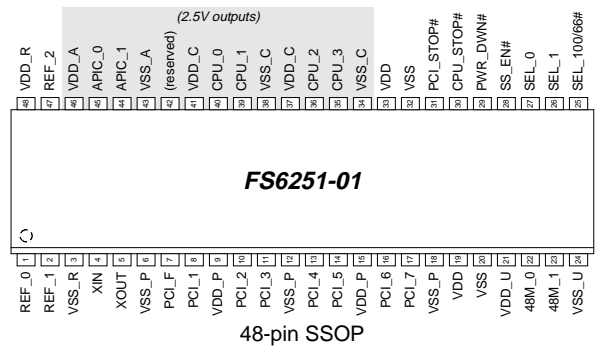


Figure 2: Pin Configuration (FS6252)

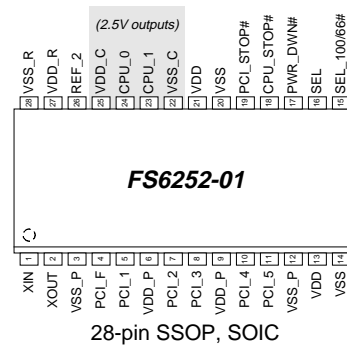


Table 1: CPU/PCI Frequency Selection

SEL_100/66#	SEL_1	SEL_0	CPU (MHz)	PCI (MHz)
0	0	0	tristate	tristate
0	0	1	70	35
0	1	0	73.33	36.67
0	1	1	66.67	33.33
1	0	0	XIN/2	XIN/6
1	0	1	105	35
1	1	0	110	36.67
1	1	1	100	33.33

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Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN (FS6251)	PIN (FS6252)	TYPE	NAME	DESCRIPTION
22, 23	-	DO	48M_0:1	Two 48MHz clock outputs for Universal Serial Bus (USB) timing
35, 36, 39, 40	23, 24	DO	CPU_0:3	Four low-skew (<175ps @ 1.25V) 2.5V to 3.3V CPU clock outputs for host frequencies. (Two copies of the CPU clock are available in FS6252 version)
30	18	DI ^U	CPU_STOP#	CPU_0:3 clock output enable. Asynchronous, active-low disable stops all CPU clocks in the low state.
44, 45	-	DO	APIC_0:1	Two buffered low-skew (<175ps @ 1.25V) 2.5V/3.3V outputs of the 14.318MHz reference clock for APIC bus timing
8, 10, 11, 13, 14, 16, 17	5, 7, 8, 9	DO	PCI_1:7	Seven low-skew (<250ps @ 1.5V) 3.3V PCI clock outputs. PCI clocks are synchronous with CPU clocks but lag the CPU clocks by 1ns to 4ns. (Four copies of the PCI clock are available in FS6252 version)
7	4	DO	PCI_F	One free-running 3.3V PCI clock output.
31	19	DI ^U	PCI_STOP#	PCI_1:7 clock output enable. Asynchronous, active-low disable stops all PCI clocks in the low state.
29	17	DI ^U	PWR_DWN#	Asynchronous active-low power-down signal shuts down oscillator, all PLLs, puts all clocks in low state. Clock re-enable latency of ≤ 3ms.
1, 2, 47	26	DO	REF_0:2	Three buffered outputs of the 14.318MHz reference clock. (One copy of the reference clock is available in FS6252 version)
26, 27	16	DI ^U	SEL_0:1	Two frequency select inputs (Both SEL pins are tied together in FS6252 version)
25	15	DI	SEL_100/66#	Selects 100MHz or 66MHz CPU clock frequency (pull-up/pull-down <i>must</i> be provided externally)
28	-	DI ^U	SS_EN#	Spread spectrum enable. Active-low enable turns on the spread spectrum feature; a logic-high turns off the spread spectrum modulation.
19, 33	13, 21	P	VDD	3.3V ± 10%
46	-	P	VDD_A	Power supply for 2.5V APIC_0:1 clock outputs
37, 41	25	P	VDD_C	Power supply for 2.5V CPU_0:3 clock outputs
9, 15	9, 12	P	VDD_P	Power supply for 3.3V PCI_1:7 and PCI_F clock outputs
48	27	P	VDD_R	Power supply for 3.3V REF_0:2 clock outputs
21	-	P	VDD_U	Power supply for 3.3V 48M_0:1 clock outputs
20, 32	14, 20	P	VSS	Ground
43	-	P	VSS_A	Ground for APIC_0:1 clock outputs
34, 38	22	P	VSS_C	Ground for CPU_0:3 clock outputs
6, 12, 18	3, 12	P	VSS_P	Ground for PCI_1:7 and PCI_F clock outputs
3	28	P	VSS_R	Ground for REF_0:2 clock outputs
24	-	P	VSS_U	Ground for 48M_0:1 clock outputs
4	1	AI	XIN	14.318MHz crystal oscillator feedback
5	2	AO	XOUT	14.318MHz crystal oscillator drive
42	-	-	(reserved)	reserved

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Table 3: Actual Clock Frequencies

Note: Spread spectrum is disabled

CLOCK	TARGET (MHz)	ACTUAL (MHz)	DEVIATION (ppm)
CPU_0:3	100.00	99.9963	-37
	66.67	66.6536	-196
PCI_1:7, PCI_F	33.33 (with CPU = 100)	33.3321	-37
	33.33 (with CPU = 66.67)	33.3268	-196
48M_0:1 ⁽¹⁾	48.00	48.0080	+167

(1) 48MHz USB clock is required to be 167ppm off from 48.000MHz to conform to USB requirements.

3.0 Programming Information

Table 4: Function/Clock Enable Configuration

CONTROL INPUTS						CLOCK OUTPUTS (MHz)					
SEL_100/66#	SEL_1	SEL_0	PWR_DWN#	CPU_STOP#	PCI_STOP#	REF_0:2	CPU_0:3	PCI_F	PCI_1:7	APIC_0:1	48M_0:1
0	0	0	1	X	X	tristate	tristate	tristate	tristate	tristate	tristate
0	0	1	1	1	1	14.318	70	35	35	14.318	48
0	1	0	1	1	1	14.318	73.33	36.67	36.67	14.318	48
0	1	1	1	1	1	14.318	66.67	33.33	33.33	14.318	48
1	0	0	1	1	1	XIN	XIN÷2	XIN÷6	XIN÷6	XIN	XIN÷2
1	0	1	1	1	1	14.318	105	35	35	14.318	48
1	1	0	1	1	1	14.318	110	36.67	36.67	14.318	48
1	1	1	1	1	1	14.318	100	33.33	33.33	14.318	48
X	X	X	0	X	X	low	low	low	low	low	low
SEL_0:1 and SEL_100/66# ≠ 0			1	0	0	14.318	low	running	low	14.318	48
			1	0	1	14.318	low	running	running	14.318	48
			1	1	0	14.318	running	running	low	14.318	48
			1	1	1	14.318	running	running	running	14.318	48

3.1 Frequency Selection

Output frequencies may be selected via three pins: SEL_100/66#, SEL_1 and SEL_0. All three pins should be fixed at a logic state before power-up occurs. Table 4 provides a guide to pin operation.

3.1.1 SEL_1, SEL_0 Pins

These two pins either tristate the output drivers, select the Test Mode frequency, or choose the CPU and PCI frequencies. Both the SEL_1 and SEL_0 pins have pull-ups that default the CPU output frequency to either

66MHz or 100MHz, depending on the state of the SEL_100/66# pin. Both 5% and 10% overclocking frequencies are available for system testing.

Both pins are bonded together on the FS6252 as the SEL pin.

3.1.2 SEL_100/66# Pin

This pin is an active-low LVTTTL input that switches between a 100MHz or a 66MHz system (CPU) clock. A pull-up or pull-down must be provided externally.

3.2 Stop Clock Control

Three pins control the clock outputs: CPU_STOP#, PCI_STOP# and PWR_DWN#.

3.2.1 CPU-Enable, PCI-Enable

The CPU_STOP# pin is an active-low LVTTTL input pin that disables the CPU_0:3 clocks for low power operation. CPU_STOP# can be asserted asynchronously, and the stop clock control is glitch-free, in that the CPU clock must complete a full cycle before the clock is stopped low.

The PCI_STOP# pin is an active-low LVTTTL input pin that disables the PCI_1:7 clocks for low power operation, except for the PCI_F clock. The PCI_F is a free-running clock, and will continue to run even if all other PCI clocks have stopped. PCI_STOP# can be asserted asynchronously, and the stop-clock control is glitch-free, in that the PCI clock must complete a full cycle before the clock is stopped low.

3.2.2 Power Down

The PWR_DWN# signal is an asynchronous, active-low LVTTTL input that puts the device in a low power inactive state without removing power from the device. All internal clocks are turned off, and all clock outputs are held low. Powering down occurs in less than two PCI clocks from the falling edge of PWR_DWN# to when all clock outputs are forced low.

4.0 Clock Latency

All clock outputs are stopped in the low state, and are started so that the first high pulse is a full pulse width. All clocks complete a full period on transitions between running (enabled) and stopped (disabled) to ensure glitch-free stop clock control.

All enabled clocks will continue to run while disabled clocks are stopped. The clock enable signals are assumed to be asynchronous inputs relative to clock outputs. Enable signals are synchronized to their respective clocks by this device. The CPU and PCI clocks will transition between running and stopped according to Table 5.

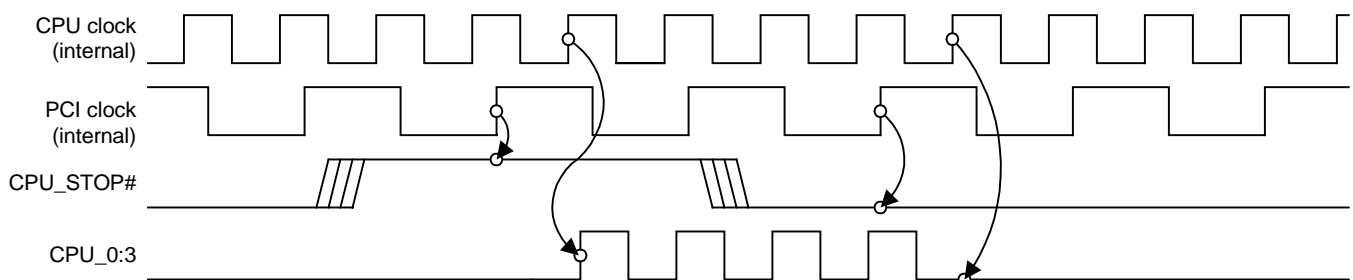
4.1 Power-Up Latency

Power-up latency is defined as the time from the moment when PWR_DWN# goes inactive (a rising edge) to when the first valid clocks are driven from the device. Upon release of PWR_DWN#, external circuitry should allow a minimum of 3ms for the PLLs to lock before enabling any clocks.

4.2 Clock Enable Latency

Clock enable latency is defined in the number of rising edges of free-running CPU clocks between when the enable signal becomes active (a rising edge) to when the first valid clock is driven from the device.

Figure 2: CPU_STOP# Timing



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Figure 3: PCI_STOP# Timing

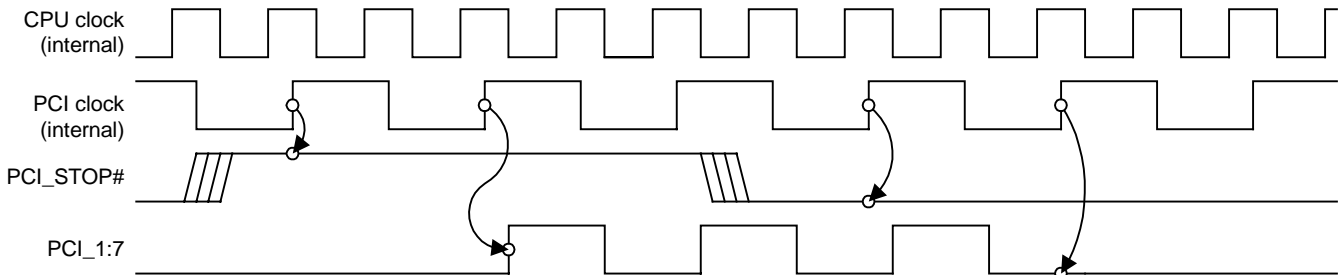
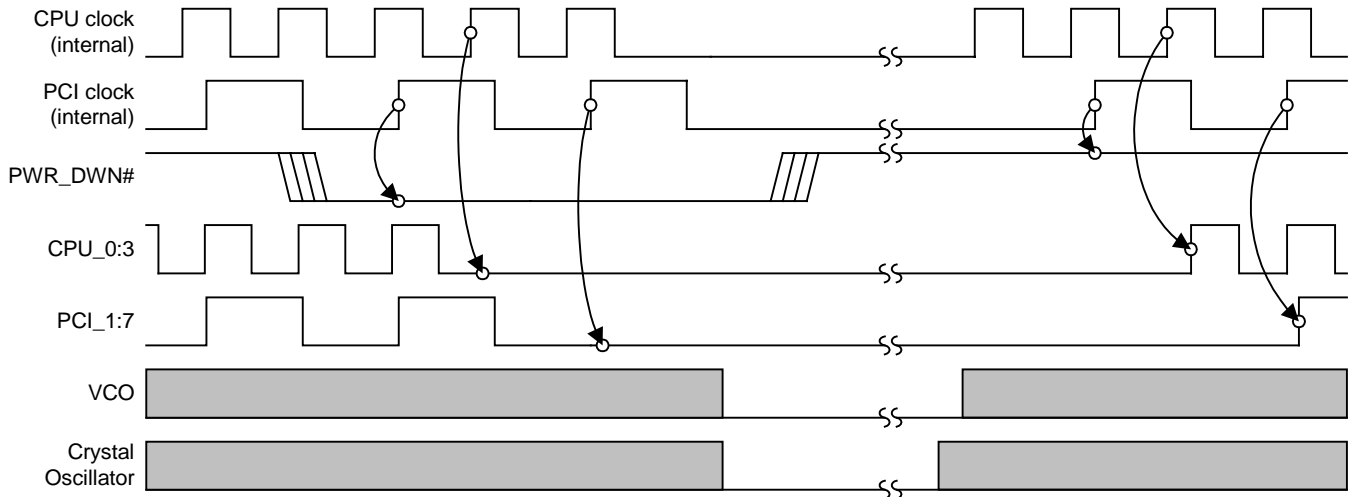


Figure 4: PWR_DWN# Timing



Shaded regions in the Crystal Oscillator and VCO waveforms indicate that the clock is valid and the Crystal Oscillator and VCO are active.

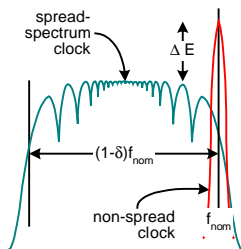
Table 5: Latency Table

SIGNAL	SIGNAL STATE		CPU CLOCK ENABLE LATENCY (Number of rising edges of the CPU clock)		PCI CLOCK ENABLE LATENCY (Number of rising edges of the PCI clock)
			MIN.	MAX.	
CPU_STOP#	0	disabled	2	3	1
	1	enabled	2	3	1
PCI_STOP#	0	disabled	2	3	1
	1	enabled	2	3	1
PWR_DWN#	0	Power OFF	1	4	2 (max.)
	1	Power ON	3ms	3ms	3ms

5.0 Spread Spectrum Modulation

To limit peak EMI emissions, high-speed motherboard designs now require the reduction of the peak harmonic energy contained in the system bus frequencies. A reduction in the peak energy of a specific frequency can be accomplished by spreading the energy over a limited range of frequencies through a technique known as spread spectrum clocking. In this technique, a generated clock frequency is dithered in a tightly controlled sweep near the clock frequency using a predetermined modulation profile and period.

Figure 5: Spectral Energy Distribution



The amount of EMI reduction is directly related to three parameters: the modulation percentage, the frequency of the modulation, and the modulation profile.

5.1 Modulation Percentage

The modulation percentage δ , is typically 0.5% of the center frequency (denoted here as f_{nom}). The modulation percentage determines the range of frequencies the spectral energy is distributed over. For a 100MHz clock frequency, a $\pm 0.5\%$ modulation sweeps the clock frequency between 99.5MHz and 100.5MHz. If the sweep is symmetrical around the center frequency, the technique is known as center-spread modulation. However, a circuit that is designed for a 100MHz reference may not have enough timing margin to support a clock greater than 100MHz. The clock frequency can instead be modulated between f_{nom} , and $(1-\delta) f_{nom}$; the technique is known as down-spread modulation. For a δ of -0.5% , the clock will sweep between 99.5MHz and 100MHz. A small degradation in circuit performance may be noticed, as the clock frequency now averages 99.75MHz.

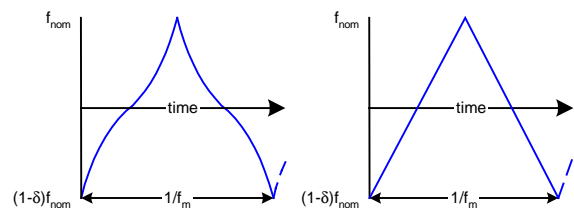
5.2 Modulation Frequency

The frequency of modulation, noted as f_m , describes how fast the center frequency sweeps between f_{nom} , and $(1-\delta) f_{nom}$. Typical modulation frequencies must be greater than 30kHz (above the audio band) but small enough to not upset system timing. Since a tracking PLL cannot instantaneously update the output clock to match a modulated input clock, any accumulation of the difference in phase between the modulated input clock and a tracking PLL output clock is called tracking skew. The resulting phase error will decrease the timing margins in any successive circuitry.

5.3 Modulation Profile

The modulation profile determines the shape of the spectral energy distribution by defining the time that the clock spends at a specific frequency. The longer a clock remains at a specific frequency, the larger the energy concentration at that frequency. A sinusoidal modulation spends a large portion of time between f_{nom} , and $(1-\delta) f_{nom}$, resulting in large energy peaks at the edges of the spectral energy distribution. A linear modulation, such as a triangle profile, improves the spectral distribution but also exhibits energy peaking at the edges. A non-linear modulation profile, known as the "Hershey Kiss" profile and patented by Lexmark International, Inc., offers the best distribution of spectral energy.

Figure 6: Modulation Profiles



The type of modulation profile used will also impact tracking skew. The maximum frequency change occurs at the profile limits where the modulation changes the slew rate polarity. To track the sudden reversal in clock frequency, the downstream PLL must have a large loop bandwidth.

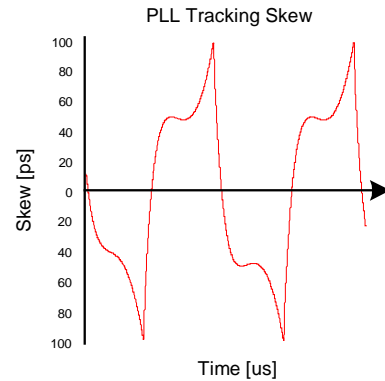
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Compared to the profile limits the modulation slew rate is relatively slow between the limits, allowing the downstream PLL a chance to reduce the tracking skew. The ability of the downstream PLL to catch up is determined by the loop transfer function phase angle.

Spread spectrum clocking can be shown to have a negligible effect on cycle-to-cycle jitter performance. Any increase in jitter is less than 1ps when $\delta < 1\%$ and $f_m < 50\text{kHz}$. Careful design of downstream PLLs can ensure that tracking skew is minimized. To have less than 100ps of tracking skew, a downstream PLL should have a loop bandwidth greater than 1MHz, and a phase angle less than 0.1° .

Figure 7 shows the tracking skew of a downstream PLL with a loop bandwidth of 1.5MHz and a phase angle of 0.26° following a non-linear profile-modulated 100MHz input clock with a $\delta = -0.5\%$ and an $f_m = 31.2\text{kHz}$.

Figure 7: PLL Tracking Skew

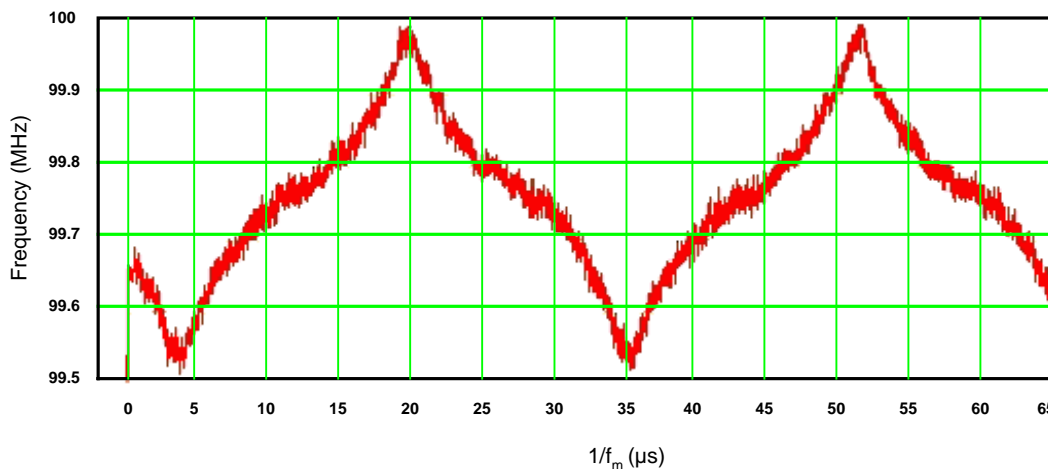


5.4 Spread Spectrum Enable

The active-low LVTTTL SS_EN# input pin enables spread spectrum modulation of the CPU and PCI clocks. When SS_EN# is a logic-high, the spread spectrum modulation of these clocks is disabled. If SS_EN# is a logic-low, spread spectrum modulation is enabled.

A pull-up on this pin disables spread spectrum modulation by default.

Figure 8: Actual Modulation Profile



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6.0 Electrical Specifications

Table 6: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	$V_{SS}-0.5$	7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	-50	50	mA
Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, method 3015.7)			2	kV



CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 7: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	Core (VDD) @ 3.3V ± 5%	3.135	3.3	3.465	V
		Clock Buffers (VDD_P, VDD_R, VDD_U) @ 3.3V ± 5%	3.135	3.3	3.465	
		Clock Buffers (VDD_A, VDD_C) @ 2.5V ± 5%	2.375	2.5	2.625	
Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XTAL}		14.316	14.318	14.32	MHz
Crystal Resonator Load Capacitance	C_{XL}	XIN, XOUT pins	13.5	18	22.5	pF
Load Capacitance	C_L	48M_0:1	10		20	pF
		APIC_0:1	10		20	
		CPU_0:3	10		20	
		PCI_F, PCI_1:7	15		30	
		REF_0:2	10		20	

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Table 8: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V ± 10%, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	$f_{CPU} = 100\text{MHz}; V_{DD_A} = V_{DD_C} = 3.465\text{V}$			170	mA
		$f_{CPU} = 100\text{MHz}; V_{DD_A} = V_{DD_C} = 2.625\text{V}$			100	
		$f_{CPU} = 66.67\text{MHz}; V_{DD_A} = V_{DD_C} = 3.465\text{V}$			170	
		$f_{CPU} = 66.67\text{MHz}; V_{DD_A} = V_{DD_C} = 2.625\text{V}$			72	
Supply Current, Static	I_{DDs}	PWR_DWN# low; $V_{DD_A} = V_{DD_C} = 3.465\text{V}$		48	500	μA
		PWR_DWN# low; $V_{DD_A} = V_{DD_C} = 2.625\text{V}$		45	100	
Digital Inputs (CPU_STOP#, PCI_STOP#, PWR_DWN#, SEL_0:1, SS_EN#)						
High-Level Input Voltage	V_{IH}		2.0		$V_{DD}+0.3$	V
Low-Level Input Voltage	V_{IL}		$V_{SS}-0.3$		0.8	V
High-Level Input Current	I_{IH}		-1		1	μA
Low-Level Input Current (pull-up)	I_{PU}	$V_{IL} = 0.4\text{V}$	15	38	50	μA
Digital Input (SEL_100/66#)						
High-Level Input Voltage	V_{IH}		2.0		$V_{DD}+0.3$	V
Low-Level Input Voltage	V_{IL}		$V_{SS}-0.3$		0.8	V
Input Leakage Current	I_{IL}		-1		1	μA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}		1.0	1.49	2.0	V
High-Level Input Current	I_{IH}	$V_{IH} = 3.3\text{V}$		34		μA
Low-Level Input Current	I_{IL}	$V_{IL} = 0\text{V}$	-50	-34	-15	μA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT	13.5	18	22.5	pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF
Crystal Oscillator Drive (XOUT)						
High Level Output Source Current	I_{OH}	$V_O = 0\text{V}$	-15		-3.0	mA
Low Level Output Sink Current	I_{OL}	$V_O = 3.3\text{V}$	3.0		15	mA
CPU_0:3 Clock Outputs (2.5V Type 1 Clock Buffer)						
High Level Output Source Current	$I_{OH\ min}$	$V_{DD_C} = 2.375\text{V}, V_O = 1.0\text{V}$	-27	-43		mA
	$I_{OH\ max}$	$V_{DD_C} = 2.625\text{V}, V_O = 2.375\text{V}$		-14	-27	
Low Level Output Sink Current	$I_{OL\ min}$	$V_{DD_C} = 2.375\text{V}, V_O = 1.2\text{V}$	27	47		mA
	$I_{OL\ max}$	$V_{DD_C} = 2.625\text{V}, V_O = 0.3\text{V}$		20	30	
Output Impedance	Z_{OL}	Measured at 1.25V, output driving low	13.5	24	45	Ω
	Z_{OH}	Measured at 1.25V, output driving high	13.5	25	45	
Tristate Output Current	I_{OZ}		-10		10	μA
Short Circuit Output Source Current *	I_{SCH}	$V_O = 0\text{V};$ shorted for 30s, max.		-56		mA
Short Circuit Output Sink Current *	I_{SCL}	$V_O = 2.5\text{V};$ shorted for 30s, max.		58		mA

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Table 8: DC Electrical Specifications, continued

Unless otherwise stated, all power supplies = 3.3V ± 10%, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
APIC_0:1 Clock Output (2.5V Type 2 Clock Buffer)						
High-Level Output Source Current	$I_{OH\ min}$	VDD_A = 2.375V, $V_O = 1.4V$	-36	-47		mA
	$I_{OH\ max}$	VDD_A = 2.625V, $V_O = 2.5V$		-10	-21	
Low-Level Output Sink Current	$I_{OL\ min}$	VDD_A = 2.375V, $V_O = 1.0V$	36	85		mA
	$I_{OL\ max}$	VDD_A = 2.625V, $V_O = 0.2V$		21	31	
Output Impedance	Z_{OL}	Measured at 1.25V, output driving low	9	12	30	Ω
	Z_{OH}	Measured at 1.25V, output driving high	9	21	30	
Tristate Output Current	I_{OZ}		-10		10	μA
Short Circuit Output Source Current *	I_{OSH}	$V_O = 0V$; shorted for 30s, max.		-66		mA
Short Circuit Output Sink Current *	I_{OSL}	$V_O = 2.5V$; shorted for 30s, max.		131		mA
REF_0:2, 48M_0:1 Clock Outputs (3.3V Type 3 Clock Buffer)						
High-Level Output Source Current	$I_{OH\ min}$	VDD_R, VDD_U = 3.135V, $V_O = 1.0V$	-29	-34		mA
	$I_{OH\ max}$	VDD_R, VDD_U = 3.465V, $V_O = 3.135V$		-12	-23	
Low-Level Output Sink Current	$I_{OL\ min}$	VDD_R, VDD_U = 3.135V, $V_O = 1.95V$	29	35		mA
	$I_{OL\ max}$	VDD_R, VDD_U = 3.465V, $V_O = 0.4V$		14	27	
Output Impedance	Z_{OL}	Measured at 1.65V, output driving low	20	41	60	Ω
	Z_{OH}	Measured at 1.65V, output driving high	20	42	60	
Tristate Output Current	I_{OZ}		-10		10	μA
Short Circuit Output Source Current *	I_{OSH}	$V_O = 0V$; shorted for 30s, max.		-41		mA
Short Circuit Output Sink Current *	I_{OSL}	$V_O = 3.3V$; shorted for 30s, max.		40		mA
PCI_1:7, PCI_F Clock Outputs (3.3V Type 5 Clock Buffer)						
High Level Output Source Current	$I_{OH\ min}$	VDD_P = 3.135V, $V_O = 1.0V$	-33	-43		mA
	$I_{OH\ max}$	VDD_P = 3.465V, $V_O = 3.135V$		-15	-33	
Low Level Output Sink Current	$I_{OL\ min}$	VDD_P = 3.135V, $V_O = 1.95V$	30	54		mA
	$I_{OL\ max}$	VDD_P = 3.465V, $V_O = 0.4V$		19	38	
Output Impedance	Z_{OL}	Measured at 1.65V, output driving low	12	27	55	Ω
	Z_{OH}	Measured at 1.65V, output driving high	12	33	55	
Tristate Output Current	I_{OZ}		-10		10	μA
Short Circuit Output Source Current *	I_{OSH}	$V_O = 0V$; shorted for 30s, max.		-51		mA
Short Circuit Output Sink Current *	I_{OSL}	$V_O = 3.3V$; shorted for 30s, max.		62		mA

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Table 9: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range $T_A = 0^{\circ}\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	100MHz			66.67MHz			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Overall									
Spread Spectrum Modulation Frequency *	f_m	SS_EN# low			31.5			31.5	kHz
Spread Spectrum Modulation Profile *		SS_EN# low	Lexmark			Lexmark			
Spread Spectrum Modulation Index *	δ_m	SS_EN# low			-0.5			-0.5	%
Clock Skew *	t_{skw}	CPU to CPU @ 1.25V, $C_L=20\text{pF}$		66	175		50	175	ps
		APIC to APIC @ 1.25V, $C_L=20\text{pF}$		32	175		24	175	
		PCI to PCI @ 1.5V, $C_L=30\text{pF}$		48	500		48	500	
Clock Offset *	t_{pd}	CPU @ 1.25V, $C_L = 20\text{pF}$ to PCI @ 1.5V, $C_L = 30\text{pF}$	1.5	1.73	4.0	1.5	1.88	4.0	ns
Tristate Enable Delay *	t_{DZL}, t_{DZH}	SEL_0:1 and SEL_100/66# = 0	1.0		8.0	1.0		8.0	ns
Tristate Disable Delay *	t_{DZL}, t_{DZH}	SEL_0:1 and SEL_100/66# = 0	1.0		8.0	1.0		8.0	ns
Clock Stabilization (on power-up) *	t_{STB}	via PWR_DWN#		1.5	3.0		1.6	3.0	ms
CPU_0:3 Clock Outputs (2.5V Type 1 Clock Buffer)									
Duty Cycle *		Ratio of high pulse width, as measured from rising edge to next falling edge at 1.25V, to one clock period	45		55	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500μs apart at 1.25V relative to an ideal clock, $C_L=20\text{pF}$, all PLLs active		295			296		ps
Jitter, Period (peak-peak) *	$t_{j(AP)}$	From rising edge to next rising edge at 1.25V, $C_L=20\text{pF}$, all PLLs active		145	250		182	250	ps
Rise Time *	$t_{r \min}$	Measured @ 0.4V – 2.0V; $C_L = 10\text{pF}$	0.4	0.8		0.4	0.8		ns
	$t_{r \max}$	Measured @ 0.4V – 2.0V; $C_L = 20\text{pF}$		1.1	1.6		1.1	1.6	
Fall Time *	$t_{f \min}$	Measured @ 2.0V – 0.4V; $C_L = 10\text{pF}$	0.4	1.0		0.4	1.0		ns
	$t_{f \max}$	Measured @ 2.0V – 0.4V; $C_L = 20\text{pF}$		1.1	1.6		1.1	1.6	
Enable Delay *	t_{DLH}	via CPU_STOP#	7		38	11		42	ns
Disable Delay *	t_{DHL}	via CPU_STOP#	2		33	3		34	ns
APIC_0:1 Clock Output (2.5V Type 2 Clock Buffer)									
Duty Cycle *		Ratio of high pulse width, as measured from rising edge to next falling edge at 1.25V, to one clock period	45		55	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500μs apart at 1.25V relative to an ideal clock, $C_L=20\text{pF}$, all PLLs active		50			35		ps
Jitter, Period (peak-peak) *	$t_{j(AP)}$	From rising edge to next rising edge at 1.25V, $C_L=20\text{pF}$, all PLLs active		215			237		ps
Rise Time *	$t_{r \min}$	Measured @ 0.4V – 2.0V; $C_L = 10\text{pF}$	0.4	1.1		0.4	1.1		ns
	$t_{r \max}$	Measured @ 0.4V – 2.0V; $C_L = 20\text{pF}$		1.3	1.6		1.3	1.6	
Fall Time *	$t_{f \min}$	Measured @ 2.0V – 0.4V; $C_L = 10\text{pF}$	0.4	0.6		0.4	0.6		ns
	$t_{f \max}$	Measured @ 2.0V – 0.4V; $C_L = 20\text{pF}$		0.8	1.6		0.8	1.6	

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Table 9: AC Timing Specifications, continued

Unless otherwise stated, all power supplies = 3.3V ± %, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	100MHz			66.67MHz			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
REF_0:2, 48M_0:1 Clock Outputs (3.3V Type 3 Clock Buffer)									
Duty Cycle *		Ratio of high pulse width, as measured from rising edge to next falling edge at 1.5V, to one clock period	45		55	45		55	%
Jitter, Long Term (σ _y (τ)) *	t _{j(LT)}	On rising edges 500μs apart at 1.5V relative to an ideal clock, C _L =20pF, all PLLs active		51			54		ps
Jitter, Period (peak-peak) *	t _{j(ΔP)}	From rising edge to next rising edge at 1.5V, C _L =20pF, all PLLs active		199			252		ps
Rise Time *	t _{r min}	Measured @ 0.4V – 2.4V; C _L = 10pF	1.0	1.3		1.0	1.3		ns
	t _{r max}	Measured @ 0.4V – 2.4V; C _L = 20pF		2.0	4.0		2.0	4.0	
Fall Time *	t _{f min}	Measured @ 2.4V – 0.4V; C _L = 10pF	1.0	1.6		1.0	1.6		ns
	t _{f max}	Measured @ 2.4V – 0.4V; C _L = 20pF		2.0	4.0		2.0	4.0	
PCI_1:7, PCI_F Clock Outputs (3.3V Type 5 Clock Buffer)									
Duty Cycle *		Ratio of high pulse width, as measured from rising edge to next falling edge at 1.5V, to one clock period	45		55	45		55	%
Jitter, Long Term (σ _y (τ)) *	t _{j(LT)}	On rising edges 500μs apart at 1.5V relative to an ideal clock, C _L =30pF, all PLLs active		293			263		ps
Jitter, Period (peak-peak) *	t _{j(ΔP)}	From rising edge to next rising edge at 1.5V, C _L =30pF, all PLLs active		148	500		146	500	ps
Rise Time *	t _{r min}	Measured @ 0.4V – 2.4V; C _L = 15pF	0.5	1.0		0.5	1.0		ns
	t _{r max}	Measured @ 0.4V – 2.4V; C _L = 30pF		1.4	2.0		1.4	2.0	
Fall Time *	t _{f min}	Measured @ 2.4V – 0.4V; C _L = 15pF	0.5	1.1		0.5	1.1		ns
	t _{f max}	Measured @ 2.4V – 0.4V; C _L = 30pF		1.5	2.0		1.5	2.0	
Enable Delay *	t _{DLH}	via PCI_STOP#	30		60	30		60	ns
Disable Delay *	t _{DHL}	via PCI_STOP#	15		45	15		45	ns

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Figure 9: CPU_0:3 Clock Outputs (2.5V Type 1 Clock Buffer)

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-28	-61	-107
0.1	3	7	11	0.4	-28	-61	-107
0.2	6	13	21	0.6	-28	-61	-107
0.3	9	19	30	0.8	-28	-61	-107
0.4	12	24	40	1	-27	-60	-105
0.5	15	30	48	1.2	-26	-58	-101
0.6	17	35	56	1.4	-24	-53	-94
0.7	19	39	63	1.6	-21	-48	-85
0.8	21	43	70	1.8	-17	-40	-73
0.9	23	47	77	1.9	-15	-36	-67
1	24	50	83	2	-12	-31	-59
1.1	25	53	88	2.1	-9	-25	-51
1.2	27	56	93	2.2	-6	-20	-43
1.3	27	58	97	2.3	-3	-14	-34
1.4	28	60	100	2.375	0	-9	-27
1.6	29	62	106	2.5	0	0	-14
1.8	29	63	110	2.625			0
2.2	29	63	111				
2.375	29	63	111				
2.5		63	111				
2.625			111				

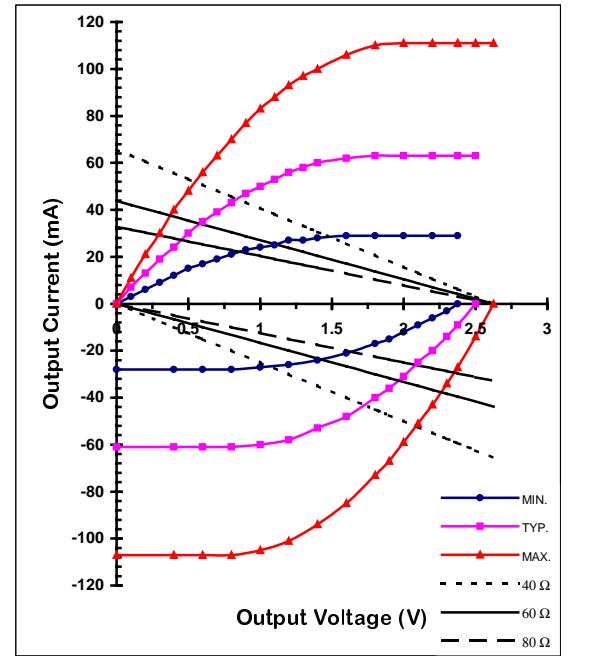
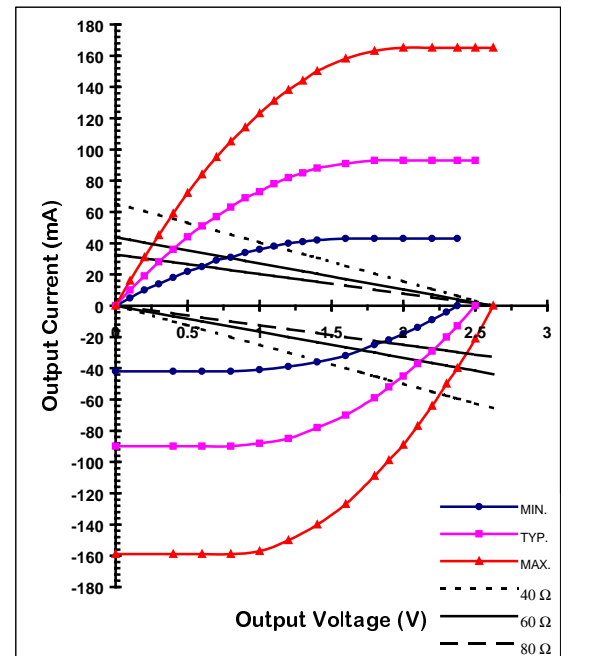


Figure 10: APIC_0:1 Clock Output (2.5V Type 2 Clock Buffer)

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-42	-90	-159
0.1	5	10	16	0.4	-42	-90	-159
0.2	10	19	31	0.6	-42	-90	-159
0.3	14	28	45	0.8	-42	-90	-159
0.4	18	36	59	1	-41	-88	-157
0.5	22	44	72	1.2	-39	-85	-150
0.6	25	51	84	1.4	-36	-78	-140
0.7	29	57	95	1.6	-32	-70	-127
0.8	31	63	105	1.8	-25	-59	-109
0.9	34	69	114	1.9	-22	-52	-99
1	36	73	123	2	-18	-45	-89
1.1	38	78	131	2.1	-14	-37	-77
1.2	40	82	138	2.2	-9	-29	-64
1.3	41	85	144	2.3	-4	-20	-50
1.4	42	88	150	2.375	0	-13	-40
1.6	43	91	158	2.5	0	0	-21
1.8	43	93	163	2.625			0
2.2	43	93	165				
2.375	43	93	165				
2.5		93	165				
2.625			165				



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Figure 11: REF_0:2, 48M_0:1 Clock Outputs (3.3V Type 3 Clock Buffer)

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-29	-46	-99
0.4	9	13	27	1	-29	-46	-99
0.65	14	21	41	1.4	-27	-44	-94
0.85	17	26	52	1.5	-27	-43	-92
1	20	29	59	1.65	-25	-41	-89
1.4	25	37	76	1.8	-24	-39	-85
1.5	26	39	79	2	-22	-36	-79
1.65	27	41	84	2.4	-16	-28	-63
1.8	28	43	88	2.6	-12	-22	-53
1.95	29	45	92	3.135	0	-6	-23
3.135	29	45	102	3.3	0	0	-12
3.6		45	102	3.465			0

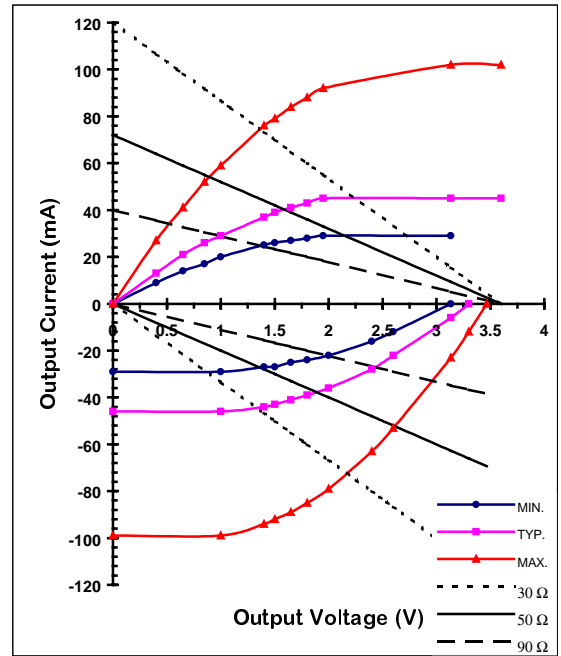
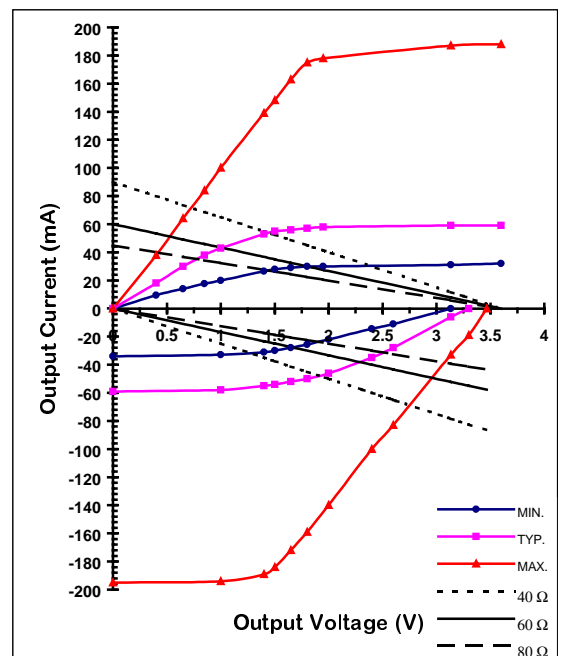


Figure 12: PCI_1:7, PCI_F Clock Outputs (3.3V Type 5 Clock Buffer)

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-34	-59	-195
0.4	9.4	18	38	1	-33	-58	-194
0.65	14	30	64	1.4	-31	-55	-189
0.85	17.7	38	84	1.5	-30	-54	-184
1	20	43	100	1.65	-28	-52	-172
1.4	26.5	53	139	1.8	-25.5	-50	-159
1.5	28	55	148	2	-22	-46	-140
1.65	29	56	163	2.4	-14.5	-35	-100
1.8	30	57	175	2.6	-11	-28	-83
1.95	30	58	178	3.135	0	-6	-33
3.135	31	59	187	3.3	0	0	-19
3.6	32	59	188	3.465			0



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Figure 13: DC Measurement Points

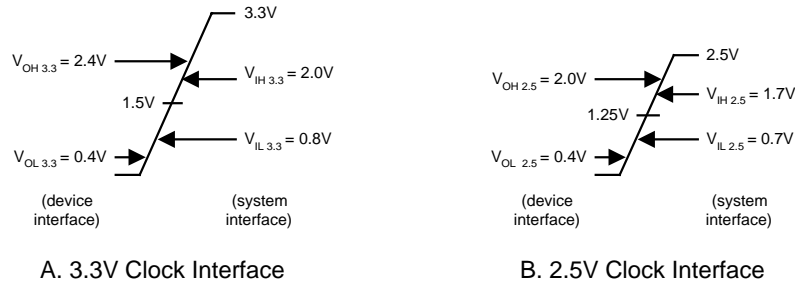


Figure 14: Clock Skew Diagrams

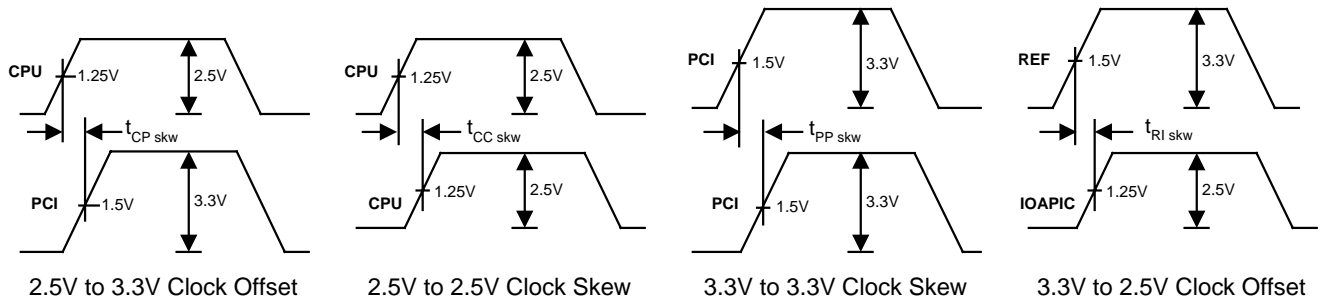
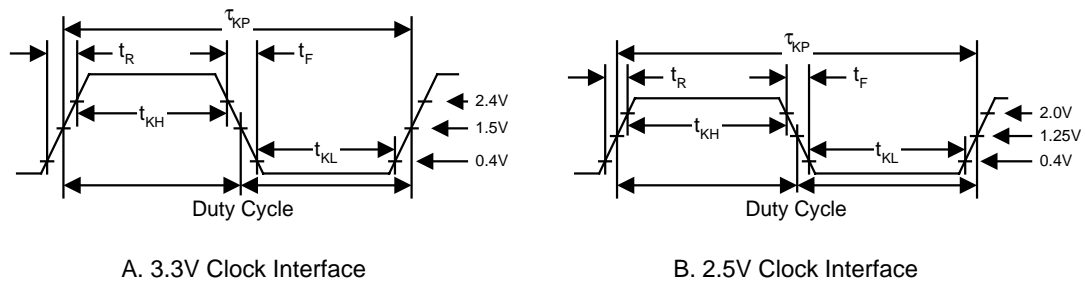


Figure 15: Timing Diagrams



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7.0 Package Information

Table 10: 48-pin SSOP (7.5mm/0.300") Package Dimensions

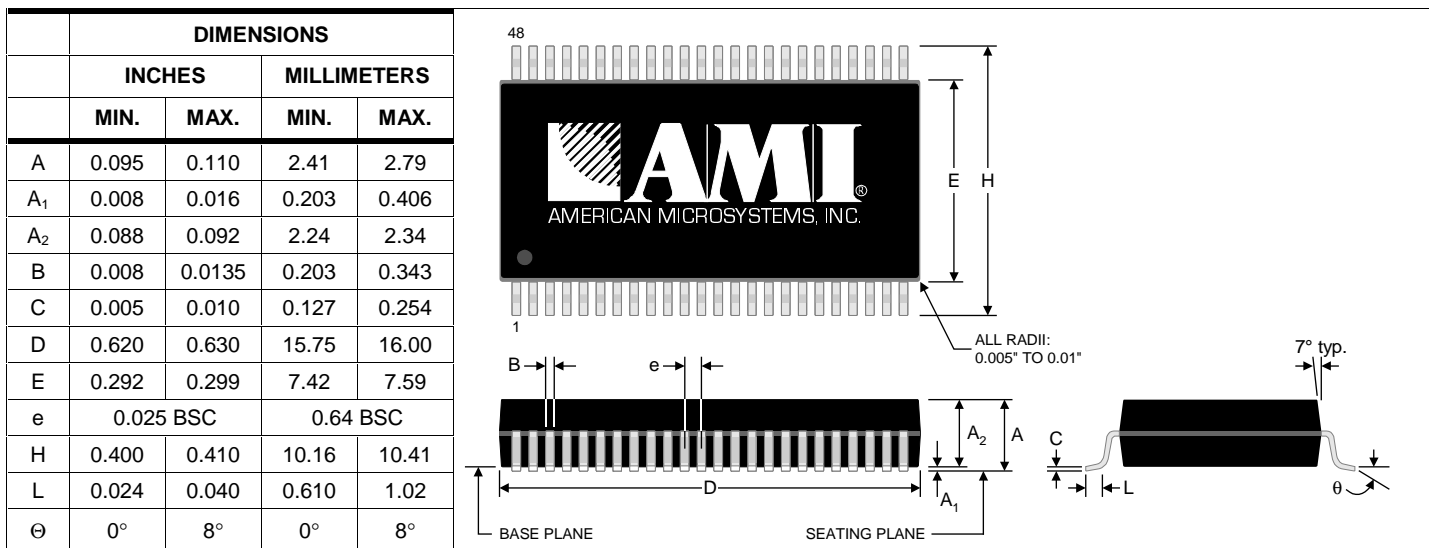


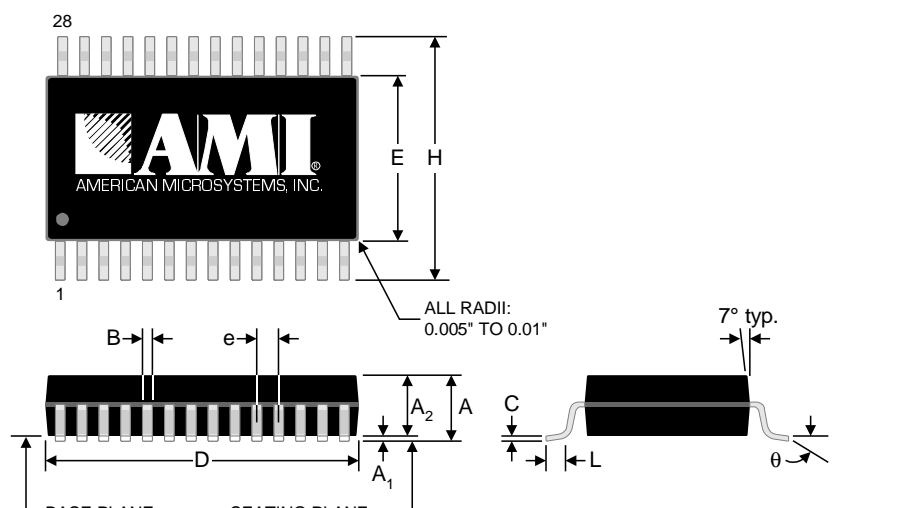
Table 11: 48-pin SSOP (7.5mm/0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	93	°C/W
Lead Inductance, Self	L ₁₁	Center lead	3.3	nH
Lead Inductance, Mutual	L ₁₂	Center lead to any adjacent lead	1.6	nH
Lead Capacitance, Bulk	C ₁₁	Center lead to V _{SS}	0.6	pF
Lead Capacitance, Mutual	C ₁₂	Center lead to any adjacent lead	0.2	pF

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Table 12: 28-pin SSOP Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.068	0.078	1.73	2.00
A ₁	0.002	0.008	0.05	0.21
A ₂	0.066	0.07	1.68	1.78
B	0.01	0.015	0.25	0.38
C	0.005	0.008	0.13	0.20
D	0.396	0.407	10.07	10.33
E	0.205	0.212	5.20	5.38
e	0.028 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95
Θ	0°	8°	0°	8°



28
1
ALL RADII: 0.005" TO 0.01"
7° typ.
BASE PLANE
SEATING PLANE

Table 13: 28-pin SSOP Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	97	°C/W
Lead Inductance, Self	L ₁₁	Center lead	2.24	nH
Lead Inductance, Mutual	L ₁₂	Center lead to any adjacent lead	0.95	nH
Lead Capacitance, Bulk	C ₁₁	Center lead to V _{SS}	0.25	pF
Lead Capacitance, Mutual	C ₁₂	Center lead to any adjacent lead	0.07	pF

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Table 14: 28-pin SOIC (0.300") Package Dimensions

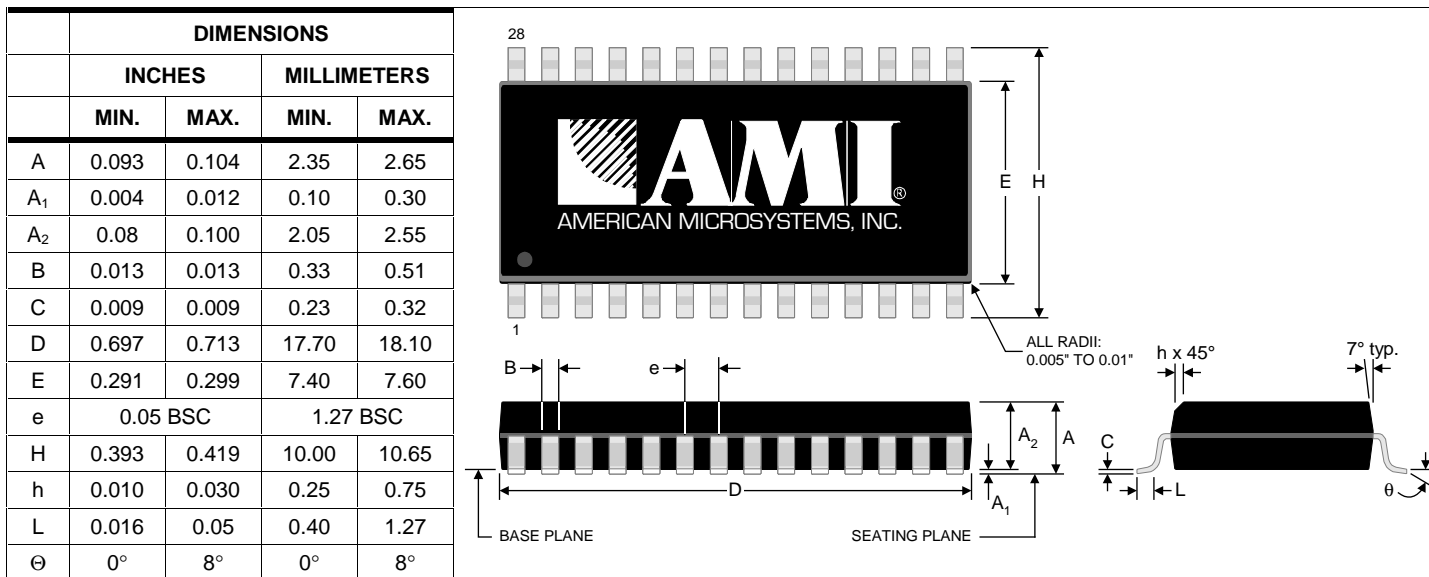


Table 15: 28-pin SOIC (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	80	°C/W
Lead Inductance, Self	L_{11}	Center lead	2.53	nH
Lead Inductance, Mutual	L_{12}	Center lead to any adjacent lead	0.85	nH
Lead Capacitance, Bulk	C_{11}	Center lead to V_{SS}	0.42	pF
Lead Capacitance, Mutual	C_{12}	Center lead to any adjacent lead	0.08	pF

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8.0 Ordering Information

DEVICE NUMBER	FONT	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6251	-01	11525-801	48-pin (7.5mm/0.300") SSOP (Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
FS6252	-01	11525-802	28-pin (7.5mm/0.300") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
		11525-803	28-pin (5.3mm/0.209") SSOP (Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel

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8.1 PLL Tracking Skew



Time-Domain PLL Simulator for SSC Tracking

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This application note is a Mathcad simulation of downstream PLL tracking skew on a spread spectrum clock with a Lexmark profile.

The Mathcad 7.0 document, along with three different modulation profiles, may be obtained from Intel's web site at <http://www.intel.com> or from AMI's web site at <http://www.amis.com>. If either document is unavailable, contact your local AMI sales representative to obtain a copy.

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Note: inputs are needed for highlighted equations (with yellow background color).

Read in the modulation profile:

(Use the .prn file name as the argument of the READPRN function. The file names of the three example modulation profiles are: lexmark.prn, triangle.prn, and sin.prn)

$f := \text{READPRN}(\text{"lexmark.prn"}) \cdot \text{Hz}$

wavepoints := rows(f) $i := 0.. \text{wavepoints} - 1$

$F_{\text{carrier}} := \text{mean}(f)$ $F_{\text{carrier}} = 99.75 \text{ MHz}$ <--the center frequency of the clock

$\delta := \frac{\max(f) - \min(f)}{\max(f)}$ $\delta = 0.5\%$ <--the spread amount

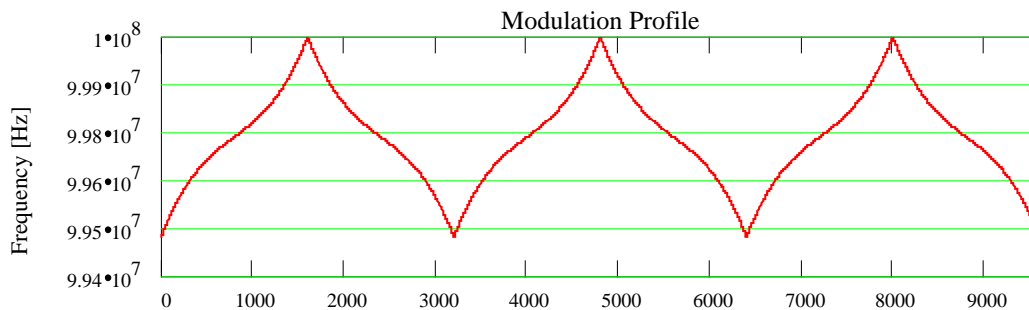
$n_1 := \text{if}(f_1 = \min(f), i, -1)$ $n_1 := \text{if}(f_1 = \max(f), i, -1)$

$f_m := \frac{F_{\text{carrier}}}{|\max(m) - \max(n)| \cdot 2}$ $f_m = 31.17 \text{ KHz}$ <--the modulation frequency

Input modulation amount (peak to peak in percentage, δ_{mod})

$\delta_{\text{mod}} := 0.5\%$ $f_{\text{mod}} := F_{\text{carrier}} + \max(f) \cdot \frac{\delta - \delta_{\text{mod}}}{2} + (f - F_{\text{carrier}}) \cdot \frac{\delta_{\text{mod}}}{\delta}$

Display the profiles



Build up a simulation. The general methodology that we will use here is:

Compute the phase of the source waveform (the one that is applied to the tracking PLL) at a series of points in time.

Iteratively compute the phase of the tracking PLL clock at successive points in the series, take the error between the two clocks and adjust the frequency of the tracking PLL to suit. Note that the spacing of the points is regular. In an actual PLL, the corrections to the loop are applied only on zero crossings of the signals. This deviation from actual practice can be demonstrated to have a very small effect on the resulting performance of the loop (assuming that no cycle slips are occurring).

The simulation time step will be set to the average clock period: $t_{\text{step}} := \frac{1}{F_{\text{carrier}}}$

Set up the range variables for simulation: $i := 0..(\text{wavepoints} - 1)$ $i1 := 1..(\text{wavepoints} - 1)$

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Compute the accumulated phase of each source clock at each point in the simulation:

$$\phi_0 := 0$$

$$\phi_{i1} := \phi_{i1-1} + 2 \cdot \pi \cdot f_{\text{mod}_{i1}} \cdot t_{\text{step}}$$

Define the parameters of the tracking PLL:

$$G_{\text{VCO}} := 400 \frac{\text{MHz}}{\text{volt}}$$

<--the vco gain (not including any feedback divider)

$$N_{\text{FB}} := 2$$

<--the modulus of the feedback divider

$$R := 9750 \text{ ohm}$$

<--the loop filter resistor

$$C_1 := 11 \cdot 10^{-12} \text{ farad}$$

<--the loop filter capacitors

$$C_2 := 356 \cdot 10^{-12} \text{ farad}$$

$$I_{\text{CP}} := 7 \cdot 10^{-6} \text{ amp}$$

<--the charge pump current

Calculate the effective series capacitance (used later):

$$C_s := \frac{C_1 \cdot C_2}{C_1 + C_2} \quad C_s = 10.67 \text{ pF}$$

Find out the loop bandwidth and the phase angle of the transfer function:

$$H_o(s) := \frac{G_{\text{VCO}} \cdot I_{\text{CP}}}{N_{\text{FB}} \cdot C_1} \cdot \frac{1}{s^2} \cdot \frac{s + \frac{1}{R \cdot C_2}}{s + \frac{1}{R \cdot C_s}}$$

$$H(s) := \frac{H_o(s)}{1 + H_o(s)}$$

$$x := 10^5 \cdot \text{Hz} \quad f_B := \frac{\text{root}\left(\left|H_o(x \cdot i)\right| - 1, x\right)}{2 \cdot \pi}$$

$$f_B = 1.504 \cdot 10^6 \text{ } ^\circ\text{Hz}$$

$$\theta := \arg\left(H\left(2 \cdot \pi \cdot f_m \cdot i\right)\right)$$

$$\theta = -0.262 \text{ } ^\circ\text{deg}$$

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Display a Bode plot of tracking PLL closed loop response:

$$\omega_{\min} := 2 \cdot \pi \cdot 1000 \cdot \text{Hz}$$

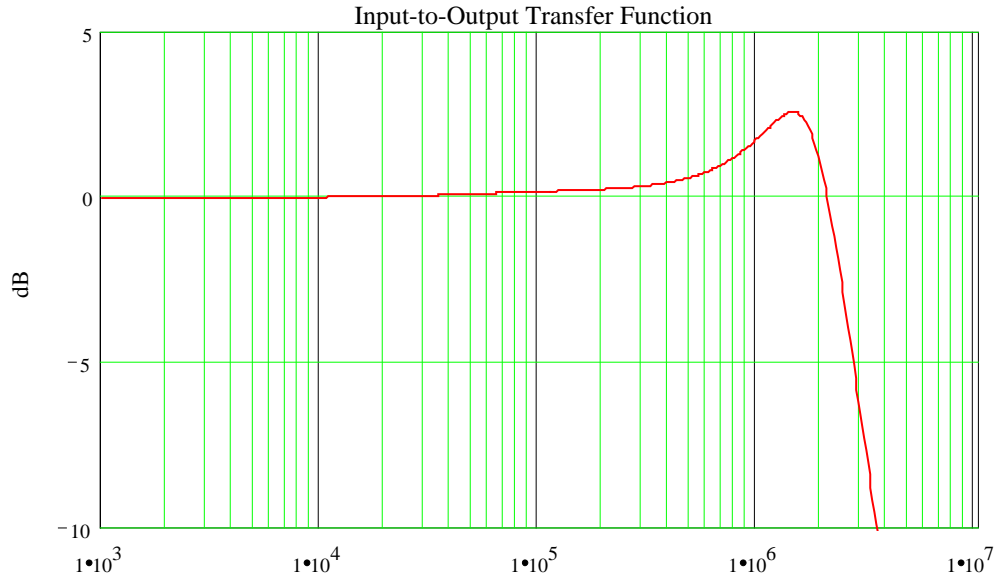
$$\omega_{\max} := 2 \cdot \pi \cdot 10 \cdot \text{MHz}$$

$$r := \ln \left(\frac{\omega_{\max}}{\omega_{\min}} \right)$$

$$\text{bpts} := 500$$

$$j := 1.. \text{bpts}$$

$$\omega_j := \omega_{\min} \cdot e^{\frac{j}{\text{bpts}} \cdot r}$$



Remove dimensions to speed iterative calculations:

$$C_1 := \frac{C_1}{\text{farad}}$$

$$C_2 := \frac{C_2}{\text{farad}}$$

$$R := \frac{R}{\text{ohm}}$$

$$G_{\text{VCO}} := G_{\text{VCO}} \cdot \text{sec} \cdot \text{volt}$$

$$t_{\text{step}} := \frac{t_{\text{step}}}{\text{sec}}$$

$$F_{\text{carrier}} := F_{\text{carrier}} \cdot \text{sec}$$

$$I_{\text{CP}} := \frac{I_{\text{CP}}}{\text{amp}}$$

$$C_s := \frac{C_s}{\text{farad}}$$

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The functions to calculate the voltage on C1 and C2 after some time (t), with an applied current (I), with initial voltages on the capacitors (V1₀ and V2₀, respectively):

$$v_1(t, V1_0, V2_0, I) := C_1 \cdot \left[\frac{(V1_0 - V2_0)}{(C_1 + C_2)} + \frac{I \cdot R \cdot C_2}{(C_1 + C_2)^2} \right] \cdot e^{\left(\frac{-t}{R \cdot C_s} \right)} \dots$$
$$+ \frac{\left[(C_1 \cdot C_2) \cdot (V1_0 + V2_0 - I \cdot R) + (C_1 + C_2) \cdot I \cdot t + C_2^2 \cdot V1_0 + C_1^2 \cdot V2_0 \right]}{(C_1 + C_2)^2}$$

$$v_2(t, V1_0, V2_0, I) := C_2 \cdot \left[\frac{(V2_0 - V1_0)}{(C_1 + C_2)} - \frac{I \cdot R \cdot C_2}{(C_1 + C_2)^2} \right] \cdot e^{\left[\frac{-t}{(R \cdot C_s)} \right]} \dots$$
$$+ \frac{\left[C_1 \cdot C_2 \cdot (V1_0 + V2_0) + (C_1 + C_2) \cdot I \cdot t + C_2^2 \cdot V1_0 + C_1^2 \cdot V2_0 + I \cdot C_2^2 \cdot R \right]}{(C_1 + C_2)^2}$$

The function used to compute the area under the loop filter voltage curve (this will be used twice: once for the time the charge pump is on and a second time when it is off):

$$a(t, V1_0, V2_0, I) := \frac{1}{2} \cdot \frac{\left[2 \cdot C_s \cdot R \cdot C_2 \cdot \left[(V1_0 - V2_0) \cdot (C_1 + C_2) + I \cdot R \cdot C_2 \right] \right]}{(C_1 + C_2)^2} \cdot e^{\left[\frac{-t}{(R \cdot C_s)} \right]} \dots$$
$$+ \frac{1}{2} \cdot \frac{\left[t \cdot \left[t \cdot I \cdot (C_1 + C_2) + 2 \cdot C_1 \cdot C_2 \cdot (V1_0 + V2_0) + 2 \cdot C_2^2 \cdot (V1_0 + I \cdot R) + 2 \cdot C_1^2 \cdot V2_0 \right] \right]}{(C_1 + C_2)^2} \dots$$
$$+ R \cdot C_s \cdot C_2 \cdot \frac{\left[(V2_0 - V1_0) \cdot (C_1 + C_2) - I \cdot R \cdot C_2 \right]}{(C_1 + C_2)^2}$$

sgn(x) := if(x < 0, -1, 1)

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Define a function to accept an array of incoming phase vs. time data and simulate the response of the PLL:

$\text{trackPLL}(\phi_src) := \left\{ \begin{array}{l} \phi_trk_0 \leftarrow 0 \\ v1_0 \leftarrow \frac{F_{carrier} \cdot N_{FB}}{G_{VCO}} \\ v2_0 \leftarrow \frac{F_{carrier} \cdot N_{FB}}{G_{VCO}} \\ \text{for } k \in 1..(\text{wavepoints} - 1) \\ \left\{ \begin{array}{l} \phi_err \leftarrow \phi_src_{k-1} - \phi_trk_{k-1} \\ \tau \leftarrow \left \frac{\phi_err}{2 \cdot \pi \cdot F_{carrier}} \right \\ \tau \leftarrow \text{if}(\tau > t_step, t_step, \tau) \\ I \leftarrow I_{CP} \cdot \text{sgn}(\phi_err) \\ v1_{\tau} \leftarrow v1(\tau, v1_{k-1}, v2_{k-1}, I) \\ v2_{\tau} \leftarrow v2(\tau, v1_{k-1}, v2_{k-1}, I) \\ v1_k \leftarrow v1[(t_step - \tau), v1_{\tau}, v2_{\tau}, 0] \\ v2_k \leftarrow v2[(t_step - \tau), v1_{\tau}, v2_{\tau}, 0] \\ A1 \leftarrow a(\tau, v1_{k-1}, v2_{k-1}, I) \\ A2 \leftarrow a[(t_step - \tau), v1_{\tau}, v2_{\tau}, 0] \\ A \leftarrow A1 + A2 \\ \phi_incr \leftarrow 2 \cdot \pi \cdot A \cdot \frac{G_{VCO}}{N_{FB}} \\ \phi_trk_k \leftarrow \phi_trk_{k-1} + \phi_incr \end{array} \right. \\ \phi_trk \end{array} \right.$	<p>initialize tracking PLL phase</p> <p>initialize C1 voltage</p> <p>initialize C2 voltage</p> <p>sample the phase error</p> <p>calculate the pulse width</p> <p>make the correct polarity of charge pump current</p> <p>compute the voltage on C1 and C2 at the end of the current pulse</p> <p>compute the voltage on C1 and C2 at the end of the sampling period</p> <p>compute the total volt-seconds under the loop filter voltage curve (in two parts)</p> <p>total phase accumulated in this step</p> <p>running total phase accumulated by VCO</p> <p>return saved data</p>
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Use the function above to compute the response of the PLL to the pre-calculated source phase sequences:

$i := 300.. \text{wavepoints} - 1$

$\text{simdata} := \text{trackPLL}(\phi)$

$$\text{skew}_i := \left(\frac{\text{simdata}_i - \phi_i}{2 \cdot \pi} \right) \cdot \frac{1}{F_{carrier} \cdot \text{Hz}}$$

translate to time-domain

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Display the resulting skew vs. time plots:

$\max(\text{skew}) = 99 \text{ ps}$

$\min(\text{skew}) = -99 \text{ ps}$

