SINGLE CHANNEL DS1/CEPT LINE INTERFACE UNIT

JULY 2004 REV. 1.0.3

GENERAL DESCRIPTION

The XRT83D10 is a fully integrated, single channel, Line Interface Unit (Transceiver) for 75 Ω or 120 Ω E1 (2.048 Mbps) and 100Ω DS1 (1.544 Mbps) applications. The LIU consists of a receiver with adaptive data slicer for accurate data and clock recovery and a transmitter which accepts dual-rail digital inputs for signal transmission to the line using a low- impedance differential line driver. The LIU also includes a crystal-less jitter attenuator for clock and data smoothing which, depending on system requirements, can be selected in either the transmit or receive path.

The XRT83D10 uses the transformer coupling on both the Receiver and Transmitter sides, and supports both 120Ω balanced,75Ω unbalanced and 100Ω interfaces.

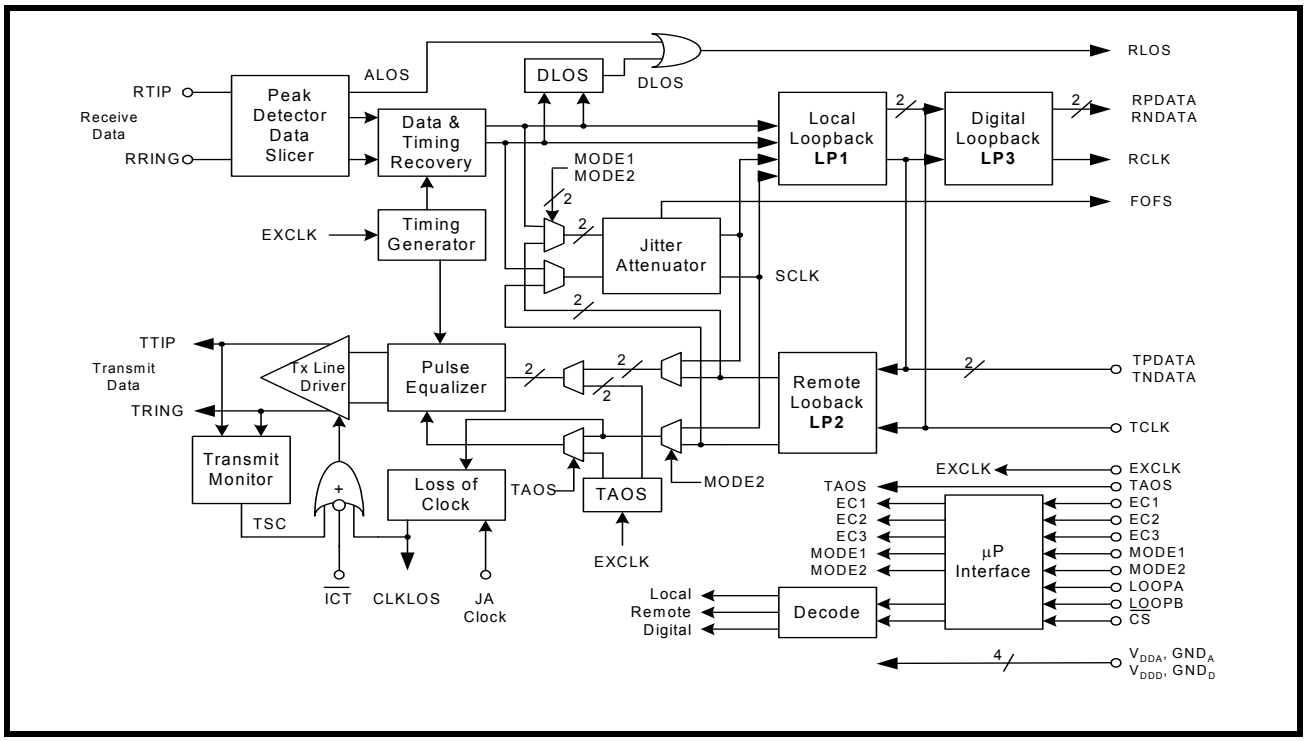
FEATURES

- Complete E1 (CEPT) and DS1 Line Interface Unit
- Generates transmit output pulses that are compliant with the ITU-T G.703 Pulse Template for 2.048Mbps (E1) rates
- On-Chip Pulse Shaping for both 75 Ω ,120 Ω and 100 Ω Line Drivers
- Clock Recovery and Selectable Crystal-less Jitter attenuator
- Compliant with ETS300166 Return Loss
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements
- Remote, Local and Digital Loop backs
- Declares and Clears LOS per ITU-T G.775
- -40°C to 85°C Temperature Range
- Low Power Dissipation
- +5V or +3.3V Supply Operation
- Pin Compatible with AGERE T7290A and T5290A

APPLICATIONS

- PDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment

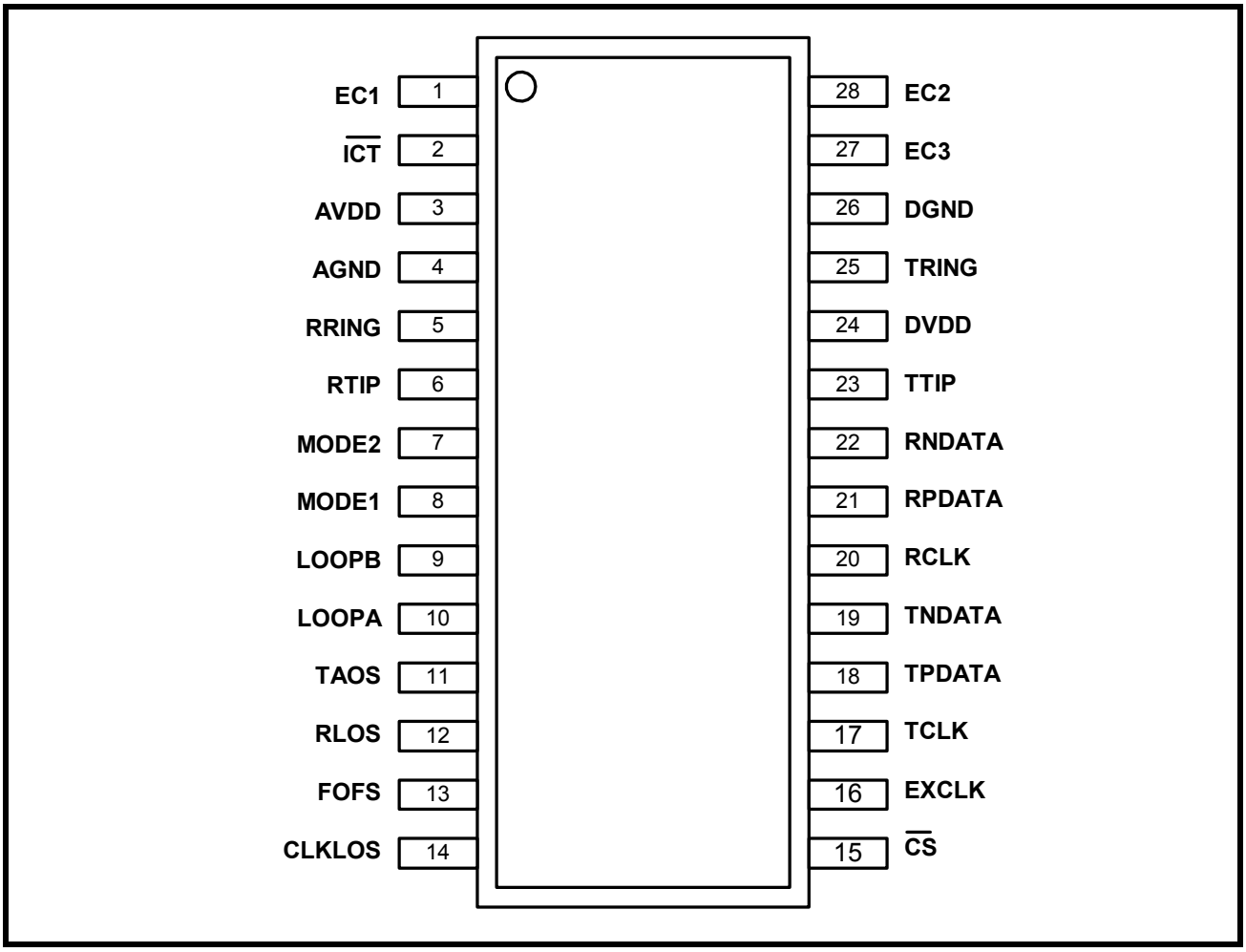
FIGURE 1. BLOCK DIAGRAM OF THE XRT83D10



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83D10IW	28 Lead 300 Mil Jedec SOJ	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT83D10



PIN DESCRIPTIONS

MICROPROCESSOR

PIN #	NAME	TYPE	DESCRIPTION
15	$\overline{CS}$	I	**Microprocessor Interface Select (Active Low)** $\overline{CS}$ loads the data into the device on its falling edge and latches the data on its rising edge. For Hardware mode, $\overline{CS}$ is left open or connected to GND. ***NOTE:*** *Internally pulled down*
1	EC1	I	**Transmit Equalization Control.** The three inputs, EC1,EC2 and EC3 are used for selecting transmit equalization. ***NOTE:*** *Internally Pulled down.*
27	EC3	I	**Transmit Equalization Control** ***NOTE:*** *Internally Pulled down.*
28	EC2	I	**Transmit Equalization Control** ***NOTE:*** *Internally Pulled down.*
7	MODE2	I	**Mode Select** Mode 1 and Mode 2 select the clock and data paths through the jitter attenuator. ***NOTE:*** *Internally Pulled down.*
8	MODE1	I	**Mode Select** ***NOTE:*** *Internally Pulled down.*
9	LOOPB	I	**Loopback control.** LOOPB along with LOOPA are used for selecting different loopbacks. **LOOPA / LOOPB / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Digital** **1 / 0 / Remote** **1 / 1 / Local** ***NOTE:*** *Internally Pulled down.*
10	LOOPA	I	**Loopback control.** LOOPB along with LOOPA are used for selecting different loopbacks. ***NOTE:*** *Internally Pulled down.*

RECEIVER SECTION

PIN #	NAME	TYPE	DESCRIPTION
6	RTIP	I	**Receive positive bipolar data Input**
5	RRING	I	**Receive negative bipolar data Input**
20	RCLK	O	**Receive Clock Output** Recovered receive clock for the terminal equipment.
21	RPDATA	O	**Receive positive NRZ data:** Recovered positive data DS1 (1.544Mbits/s) or CEPT (2.048 Mbits/s)
22	RNDATA	O	**Receive negative data** Recovered negative NRZ data DS1 (1.544Mbits/s) or CEPT (2.048 Mbits/s)
12	RLOS	O	**Receive Loss of Signal:** This pin is set "High" if analog loss-of-signal at the receiver input is detected or if digital loss-of-signal of the recovered data is detected.RLOS will remain "High" until the loss of signal condition clears.

TRANSMITTER SECTION

PIN #	NAME	TYPE	DESCRIPTION
17	TCLK	I	**Transmit Clock** DS1 Clock Signal. (1.544 MHz ± 130 ppm) or CEPT clock signal (2.048 MHz ± 80 ppm).
18	TPDATA	I	**Transmit Positive Data** DS1 (1.544 Mbits/s) or CEPT (2.048 Mbits/s) positive bipolar data
19	TNDATA	I	**Transmit Negative Data** DS1 (1.544 Mbits/s) or CEPT (2.048 Mbits/s) negative bipolar data
23	TTIP	O	**Transmit Tip Output** Positive bipolar transmit data
25	TRING	O	**Transmit Differential Ring Output** Negative bipolar transmit data
14	CLKLOS	O	**Loss of Clock Signal:** This pin is set "High" when either the transmit clock (TCLK) or the clock output from the jitter attenuator is absent.

CONTROL FUNCTION

PIN #	NAME	TYPE	DESCRIPTION
2	$\overline{\text{ICT}}$	I	**In Circuit Testing** When this pin is tied "Low" all output pins are forced to high-impedance state for in-circuit testing. ***NOTE:*** *Internally pulled up.*
16	ExCLK	I	**External Clock Input:** DS1 (1.544 MHz ± 130 ppm) or CEPT E1 (2.048 MHz ± 80 ppm) clock signal is provided. ExCLK must be an independent clock to guarantee device performance for all specifications. This clock must be continuously active (ungapped or unswitched) and void of jitter for the device to operate properly.
11	TAOS	I	**Transmit All Ones:** With this pin tied "High", an AMI encoded all "1's" signal sent to the transmit output using ExCLK as the timing reference. A remote loop back has higher priority over TAOS request. ***NOTE:*** *Internally pulled down.*
9	LOOPB	I	**Loopback control.** LOOPB along with LOOPA is used for selecting different loopbacks. **LOOPA / LOOPB / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Digital** **1 / 0 / Remote** **1 / 1 / Local** ***NOTE:*** *Internally Pulled down.*
10	LOOPA	I	**Loopback control.** LOOPB along with LOOPA is used for selecting different loopbacks. ***NOTE:*** *Internally Pulled down.*
13	FOFS	O	**FIFO Overflow Signal:** This pin is set "High" if the phase jitter of the incoming signal exceeds the tolerance of the jitter attenuator's buffer. This may result in loss of data and Jitter Attenuator is no longer attenuating jitter.

POWER AND GROUND

PIN #	NAME	TYPE	DESCRIPTION
3	AVDD	****	Analog Supply: 5V ± 5% or 3.3V ± 5%
4	AGND	****	Analog GND.
24	DVDD	****	Digital Supply: 5V ± 5% or 3.3V ± 5%
26	DGND	****	Digital GND

TABLE 1: DC ELECTRICAL CHARACTERISTICS

Ta = -40°C to 85°C, Vdd = 5V ± 5% or 3.3V ± 5% unless otherwise specified					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Input High Voltage	V_{IH}	2.0	5.0	5.5	V
Input Low Voltage	V_{IL}	0.5	0	0.8	V
Output High Voltage @IOH=5mA (See Note) VDD=5.0v VDD=3.3v	V_{OH}	2.4	-	VDD	V
Output Low Voltage @ IOL=5mA (See Note) VDD=5.0v VDD=3.3v	V_{OL}	0	-	0.4	V
Input Leakage Current (except input pins with pull-up resistors)	I_L	-	0	10	uA
Input Capacitance	C_I	-	5	20	pF
Output Load Capacitance	C_O	-	-	20	pF

ELECTRICAL CHARACTERISTICS- POWER SPECIFICATIONS

PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Power Dissipation:	PD				
With Jitter Attenuator					
DS1 (EC1=0,EC2=1,EC3=1)			275	350	mW
CEPT (75 Ω)			275	350	mW
CEPT (120 Ω)			275	350	mW

NOTE: *Power consumption measurement conditions with 50% 1s on the Transmit and Receive, TA = 25^0 C, VDD = 5V*

TABLE 2: RECEIVER CHARACTERISTICS

TA = -40°C to 85°C, VDD = 5V± 5% or 3.3V ± 5% Unless otherwise specified				
PARAMETER	**MIN.**	**TYP.**	**MAX**	**UNIT**
Receiver Sensitivity DS1[1] CEPT[2]	 10 9			dB
Recovered Clock Jitter Transfer Corner Frequency	-	20		kHz
Jitter Attenuator Corner Frequency (-3dB curve)	-	3		Hz
Return Loss in E1 (CEPT) Mode 51kHz-102kHz 102kHz-2048kHz 2048kHz-3072kHz	 12 18 14			 dB dB dB

NOTES:

1. *Measured at 772 KHz. 0dB is the Reference to 3.0Vp.*
2. *Measured at 1024 KHz (both for 75Ω and 120Ω). 0dB is the Reference to 2.37Vp (75Ω) and 3.0Vp (120Ω)*

TABLE 3: TRANSMITTER CHARACTERISTICS

TA = -40°C to 85°C, VDD = 5V± 5% or 3.3V ± 5% Unless otherwise specified				
PARAMETER	**MIN.**	**TYP.**	**MAX**	**UNIT**
AMI Output Pulse Amplitude DS1 (at DSX) 75 Ω Application 120 Ω Application	 2.4 2.13 2.70	 3.0 2.37 3.00	 3.6 2.60 3.30	 V V V
Output Pulse Width DS1 CEPT	 330 224	 350 244	 370 264	 ns ns
Output Power Levels: DS1 (2kHz band at 772 kHz) DS1 (2 kHz band at 1544 kHz)	 12 -29	 16.7 -35	 17.9 -	 dBm dB
Output Return Loss:(CEPT only) 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 8 8 8	 - - -	 	 dB dB dB

TABLE 4: INTERFACE DATA TIMING (SEE FIGURES 3 AND 4)

TA = -40° to +85 °C, VDD = 5V ± 5% or 3.3V ± 5% Unless otherwise specified					
PARAMETER	**SYMBOL**	**MIN.**	**TYP**	**MAX**	**UNITS**
Transmit Clock Period DS1[1] CEPT[2]	TClk	-	 647.7 488	-	 ns ns
TClk Duty Cycle	T_{CLK}	40	50	60	%
Transmit Data Setup Time	t_{TSU}	50	-	-	ns
Transmit Data Hold Time	t_{THO}	40	-	-	ns
TClk Rise Time (10% /90%)	t_r	-	-	40	ns
TClk Fall Time (90% / 10%)	t_f	-	-	40	ns
Receive Data Setup Time	t_{RSU}	140		-	ns
Receive Data Hold Time	t_{RHO}	180		-	ns
Receive Propagation Delay	t_{PD}			40	ns

NOTE: *1. Tolerance of ± 130 ppm 2. Tolerance of ± 80 ppm.*

FIGURE 3. INTERFACE TIMING DIAGRAM - TRANSMIT

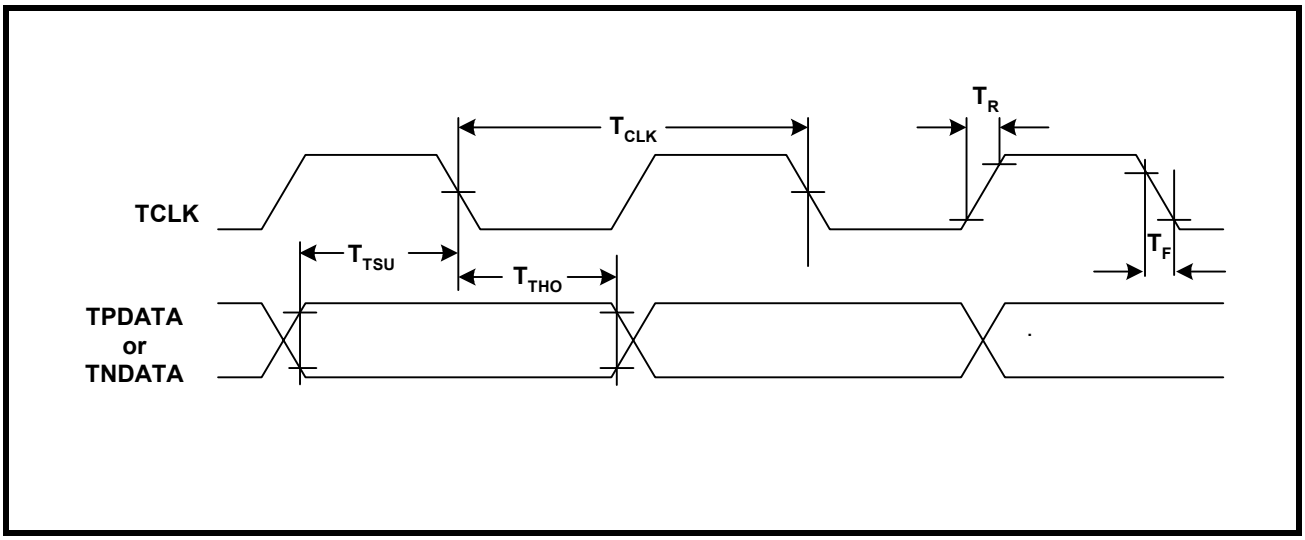


FIGURE 4. INTERFACE TIMING DIAGRAM - RECEIVE

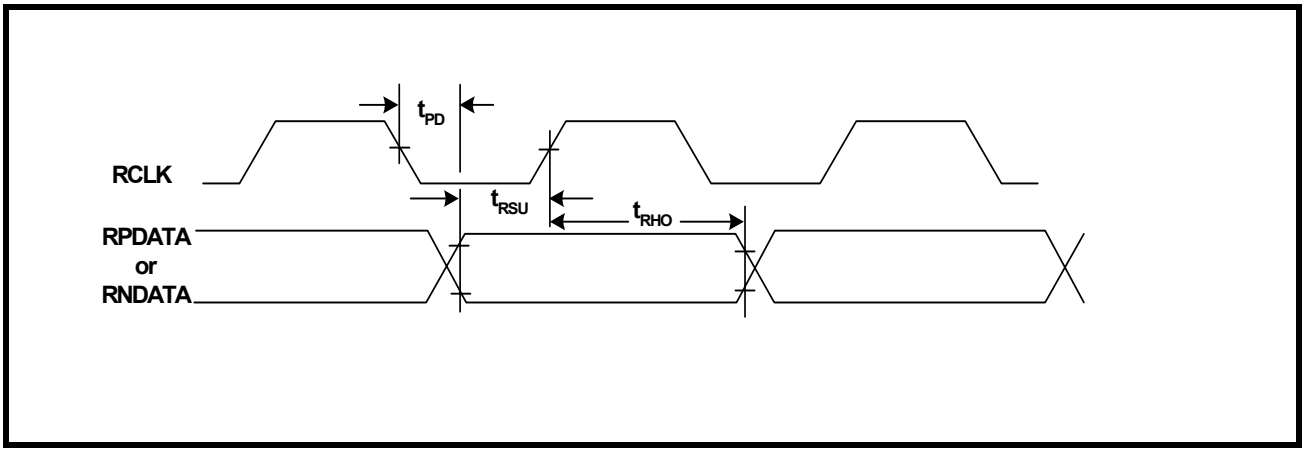


FIGURE 5. MICROPROCESSOR INTERFACE TIMING

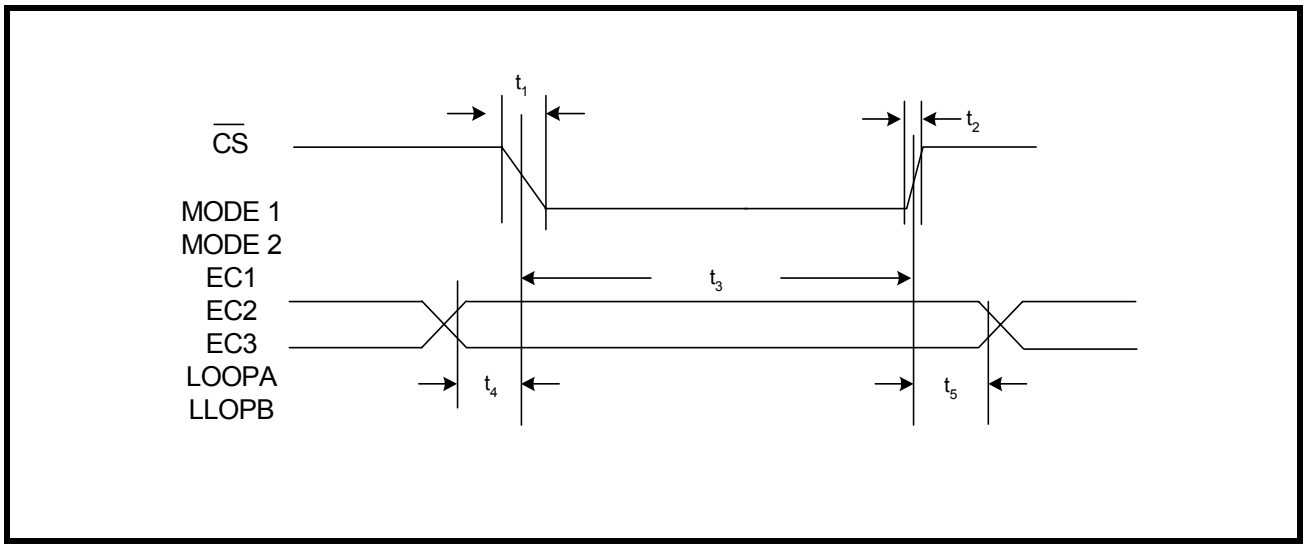


TABLE 5: MICROPROCESSOR INTERFACE TIMING

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_1	Control Signal Rise Time (10% - 90%)		40	ns
t_2	Control Signal Rise Time (10% - 90%)		40	ns
t_3	Control Signal Pulse Width Time	40		ns
t_4	Control SIgnal Setup Time	50		ns
t_5	Control Signal Hold Time	40		ns

1.0 SYSTEM DESCRIPTION:

1.1 RECEIVER:

The XRT83D10, a single channel DS1/CEPT Line Interface Unit is a fully integrated transceiver that provides an electrical interface for DS1 carrier rate (1.544 Mbits/s) or CEPT rate (2.048 Mbits/s) applications.The bipolar input signals at RTIP and RRING are applied to the peak detector and slicer.Timing recovery is performed by the Clock and Data Recovery block. EC1,EC2 and EC3 rate control inputs must be set appropriately for DS1 or CEPT operation. The digital representation of the AMI signals goes to the clock recovery circuit for timing recovery before being output to the RPDATA and RNDATA pins. Clock timing recovery of the line interface is accomplished by means of a digital PLL scheme which has high input jitter tolerance.

A continuously active (ungapped or unswitched) reference clock must be present at ExCLK to enable the Timing Generator block. ExCLK must be an independent reference such as an oscillator or system clock for proper operation. The ExCLK frequency must be 1.544 MHz ± 130 ppm for DS1 operation or 2.048 MHz ± 80 ppm for CEPT operation.

Any data pattern with a minimum long-term 1s density of 12.5% with 15 or fewer consecutive 0s is allowed.

1.1.1 Loss of Signal:

Both digital (DLOS) and analog (ALOS) loss-of-signal detection are used. The analog signal detector uses the output of the peak detector to determine if a signal is present at RTIP and RRING. If the input amplitude drops below approximately 0.4 Vp, the analog detector becomes active.Hysteresis is provided in the analog detector to eliminate ALOS chattering. Either the analog or digital detector sets RLOS "High".

1.2 TRANSMITTER:

The transmitter accepts a clock with positive and negative data (dual-rail NRZ format) and converts the signal to a balanced bipolar data signal (AMI format). Positive 1s are produced by a positive pulse on device pin TTIP and negative 1s are produced by a positive pulse on device pin TRING. Binary 0s are converted to null pulses. All pulse shapes are controlled on-chip according to equalizer control inputs as defined in Table 6 below.

TABLE 6: EQUALIZER/RATE CONTROL

OPERATION	CLOCK RATE	TRANSMITTER EQUALIZATION*	MAXIMUM CABLE LOSS**	EC1	EC2	EC3
DS1	1.544 MHz	0 ft -131 ft	0.6	0	0	1
		131 ft - 262 ft	1.2	0	1	0
		262 ft - 393 ft	1.8	0	1	1
		393 ft - 524 ft	2.4	1	0	0
		524 ft - 655 ft	3.0	1	0	1
CEPT	2.048 MHz	75 Ω	-	1	1	0
		120 Ω	-	1	1	1

NOTES:

1. ** Distance to DSX in feet for 22-Ga. Use maximum loss figures for other cable types.*
2. *** dB at 772 kHz.*

Transmitter specifications are shown in Figure 6. The DS1 pulse shape template is specified at the DSX and is illustrated in Figure 6.CEPT transmit waveforms at the device output conform to the template shown in Figure 7.

FIGURE 6. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

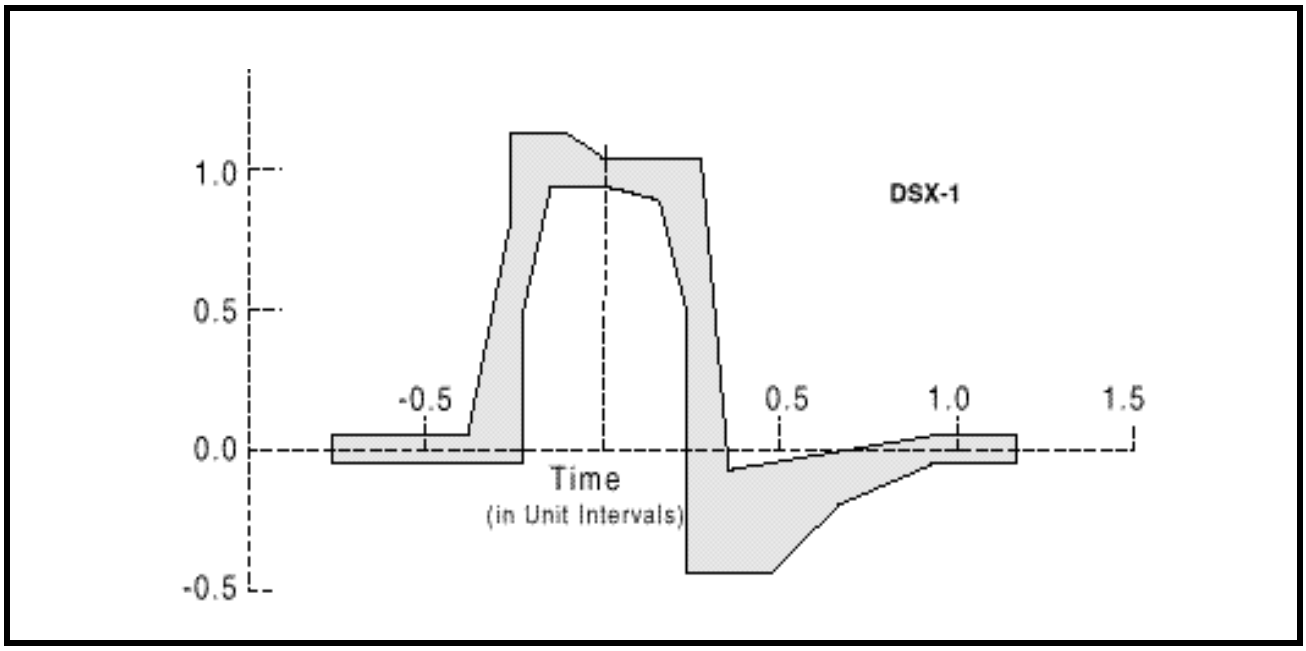
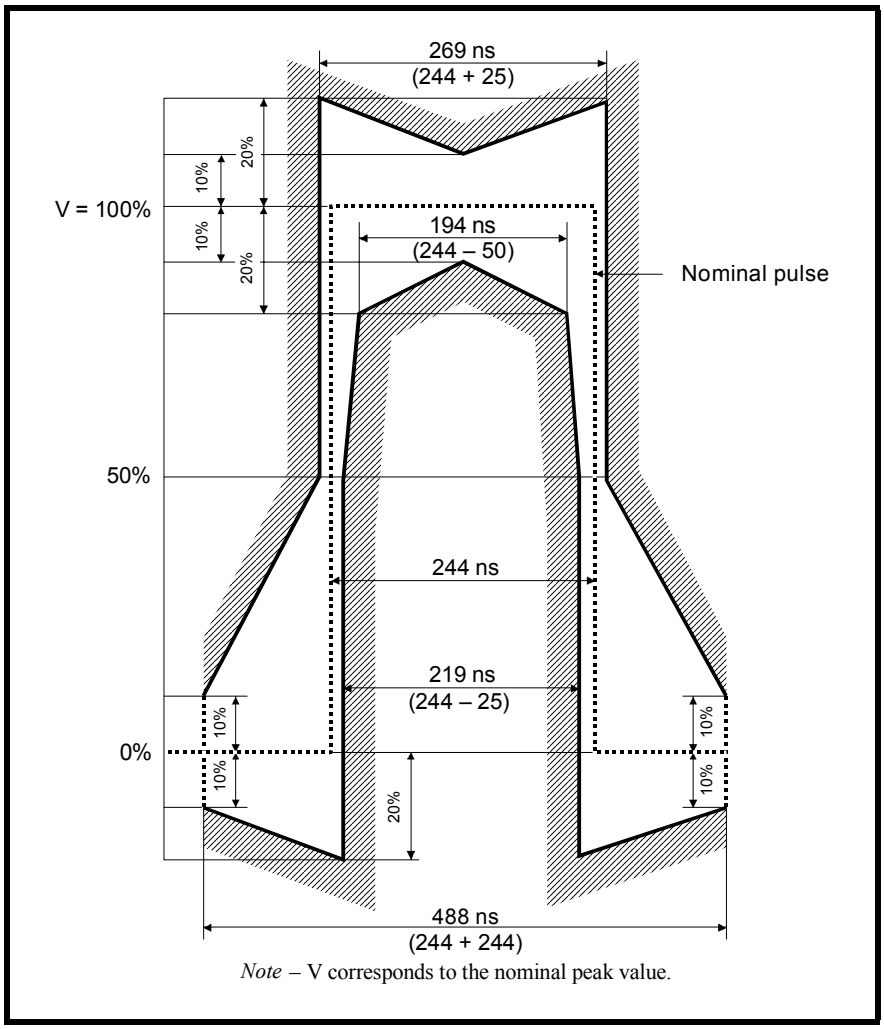


TABLE 7: DSX1 INTERFACE ISOLATED PULSE MASK PER ANSI T1.102-1993 AND CORNER POINT SPECIFICATIONS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE (V)	TIME (UI)	NORMALIZED AMPLITUDE (V)
-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05
-0.23	0.5	-0.27	0.8
-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.15
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	-0.45	0.35	-0.07
0.46	-0.45	0.93	0.05
0.66	-0.2	1.16	0.05
0.93	-0.05		
1.16	-0.05		

FIGURE 7. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

1.3 JITTER ATTENUATOR

To reduce frequency jitter in the transmit clock or receive clock, a crystal-less jitter attenuator is provided. The jitter attenuator can be selected either in the transmit or receive path or it can be disabled as shown in Table 8.

TABLE 8: JITTER ATTENUATOR SELECTION

JITTER ATTENUATOR CONNECTIVITY	MODE 1	MODE 2
Bypass (Disabled)	0	0
Transmit Path	0	1
Receive Path	1	0
Test Mode	1	1

1.3.1 FIFO Overflow Signal (FOFS):

A FIFO overflow Signal (FOFS = 1) is indicated if the phase jitter exceeds the tolerance of the jitter attenuator. When FOFS is "High", jitter attenuator bandwidth is increased to track the short term jitter and no data error will

occur.Jitter attenuator is no longer attenuating input jitter.(This signal is asserted until normal operation resumes.)

1.4 ALARMS AND MAINTENANCE:

1.4.1 Loss of Signal:

A digital loss of signal (DLOS =1) is indicated if 175±75 or more consecutive 0s occur in the receive data stream during DS1 operation.During CEPT operation, a DLOS is indicated when 32 or more consecutive 0s occur in the receive data stream.DLOS is the deactivated when the ones density exceeds 12.5% and there are no more than 100 consecutive 0s for DS1 and 16 consecutive 0s for CEPT, signifying the return of good signal.DLOS deactivation monitors the data in a fixed 32-bit window.Each window must have at least four 1s with no more than 15 consecutive 0s. Upon DLOS detection, RCLK is phase-locked to the external clock (ExCLK) so that other system devices slaved to the line clock continue to operate without instantaneous phase hits or discontinuities. Either an analog loss of signal (ALOS) or a digital loss of signal (DLOS) activates the RLOS output pin.

1.4.2 Loss of Clock Signal (CLKLOS):

A loss of clock signal (CLKLOS =1) is indicated if either the transmit clock (TCLK) or the smoothing clock (SCLK) output of the jitter attenuator is absent.If the jitter attenuator is placed in the transmit path, the SCLK is monitored.If the jitter attenuator is not placed in the transmit path, TCLK or Remote Loopback Clock is monitored.For every ten clock periods of the ExCLK oscillator clock, a strobe is generated.If a single transmit clock period occurs between strobes, then CLKLOS = 0. If no transmit clock period occurs between strobes, then CLKLOS = 1 and the output drivers ((TTIP and TRING) are placed into a high-impedance state and no data is transmitted.

1.4.3 AIS (TAOS) Generator:

When the transmit all ones (TAOS = 1) signal is set, a continuous stream of bipolar 1s is transmitted onto the line synchronous with ExCLK. The TPDATA and TNDATA inputs are ignored during this mode. If the RLOS output is externally connected to the TAOS input, an RLOS error initiates a transmit all 1s signal as long as RLOS = 1.Also, TAOS input is ignored when a remote loopback is selected. There is no microprocessor input for the TAOS input, i.e., any change on the TAOS pin is fed directly into the device and is not impeded by the $\overline{CS}$ function.

1.5 LOOPBACKS:

The XRT83D10 has three independent loopback paths, which are activated as shown in Figure 9.

TABLE 9: LOOPBACK CONTROL

OPERATION	SYMBOL	LOOPA	LOOPB
Normal	-	0	0
Digital Local loopback	LP3	0	1
Remote Loopback	LP2*	1	0
Local Loopback	LP1	1	1

NOTE: *During Remote Loopback, TAOS is ignored.*

A local loopback (LP1) connects the jitter attenuator's output clock and data to the receive clock and data output pins. MODE1:2 = 01 must be selected for this loopback to operate (jitter attenuator in the transmit path). Valid transmit output data continues to be sent to the network. However, if the transmit all 1s (TAOS =1) is

initiated, an all 1s signal is sent to the network and does not corrupt the looped data. The RLOS alarm still monitors the entire receive function.

A remote loopback (LP2) loops the recovered clock and re-timed data into the transmitter and back onto the line. The receive front end, receive PLL, jitter attenuator (if enabled), and transmit driver circuitry are all exercised. The transmit clock, transmit data, and TAOS inputs are ignored. Valid receive output data continues to be sent to RPDATA and RNDATA. This loop can be used to isolate failures between systems.

A digital local loopback (LP3) directly loops the transmit clock and data to the receive clock and data output pins. The transmit all 1s signal can be transmitted when in this loopback. LP3 (rather than LP1) must be selected if MODE2 = 0.

1.6 MICROPROCESSOR INTERFACE:

A chip select input ($\overline{CS}$) configures the device in either hardware mode or microprocessor mode. The chip-select function, applies to the following inputs: MODE1, MODE2,EC1,EC2,EC3,LOOPA and LOOPB. In the hardware mode, any change on these asynchronous input pins fed directly into the device.To maintain hardware mode, set $\overline{CS}$ = 0. In the microprocessor mode, new digital control inputs are loaded into the XRT83D10 on the falling edge of $\overline{CS}$ and are latched on the rising edge of $\overline{CS}$.

1.7 IN-CIRCUIT TESTING:

The XRT83D10 has the ability to allow for in-circuit testing by activating the high-impedance mode ($\overline{ICT}$ = 0).During this mode, all output buffers (TTIP,TRING,RCLK,RPDATA,RNDATA,RLOS,FOFS and CLKLOS) are 3-stated. During the 3-stated condition, the absolute maximum voltage ratings must not be exceeded on any pin.

1.8 ABSOLUTE MAXIMUM RATINGS:

Stresses in excess of absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only.Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet.

ELECTRICAL CHARACTERISTICS - ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Supply Voltage Range	VDD	-0.5	6.5	V
Storage Temperature	STO	-65	125	degC
Maximum Voltage (any pin) with respect to VDD			0.5	V
Minimum Voltage (any pin) with respect to GND		-0.5		V
Maximum voltage allowed (RTIP,RRING) with respect to GND		-5.0	5.0	V
ESD (Human-body model)		2000		V

NOTE: *Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device.The above values are absolute stress ratings only. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.*

2.0 APPLICATIONS:

2.1 Line Termination:

For the following applications, the tolerance of all transformer turns ratios is a maximum of ± 2%. The tolerance of all resistors in the transmit path is a maximum of ± 1%.

FIGURE 8. CEPT APPLICATION FOR TWISTED-PAIR INTERFACE - 5V OR 3.3V OPERATION.

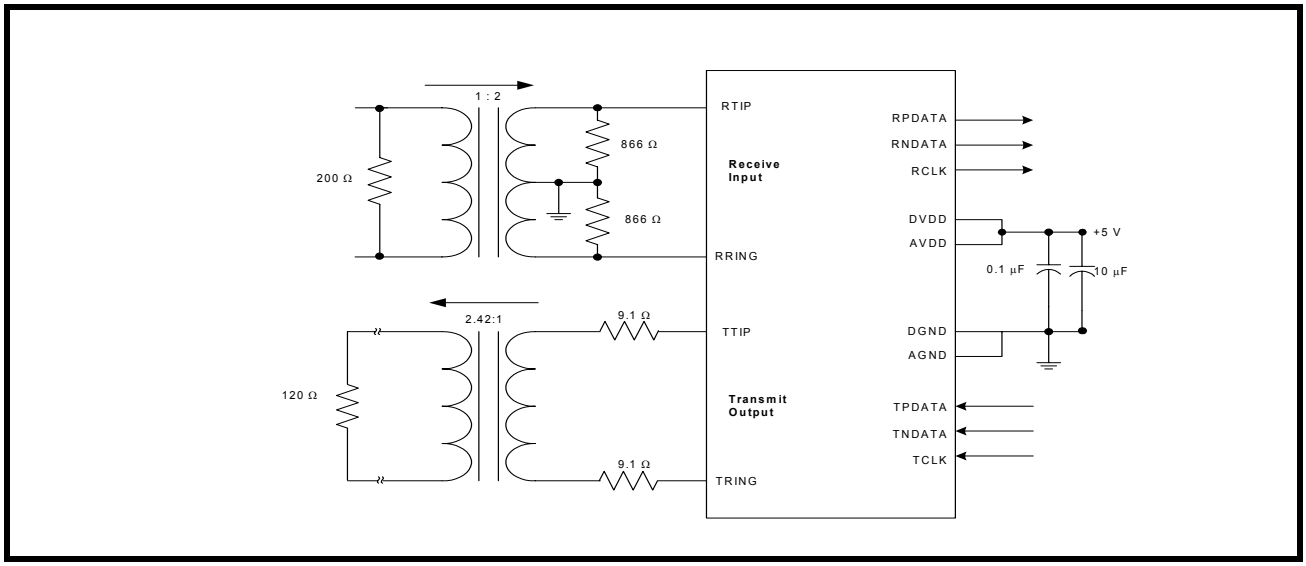


FIGURE 9. DS1 APPLICATION FOR TWISTED-PAIR INTERFACE - 5V OR 3.3V OPERATION.

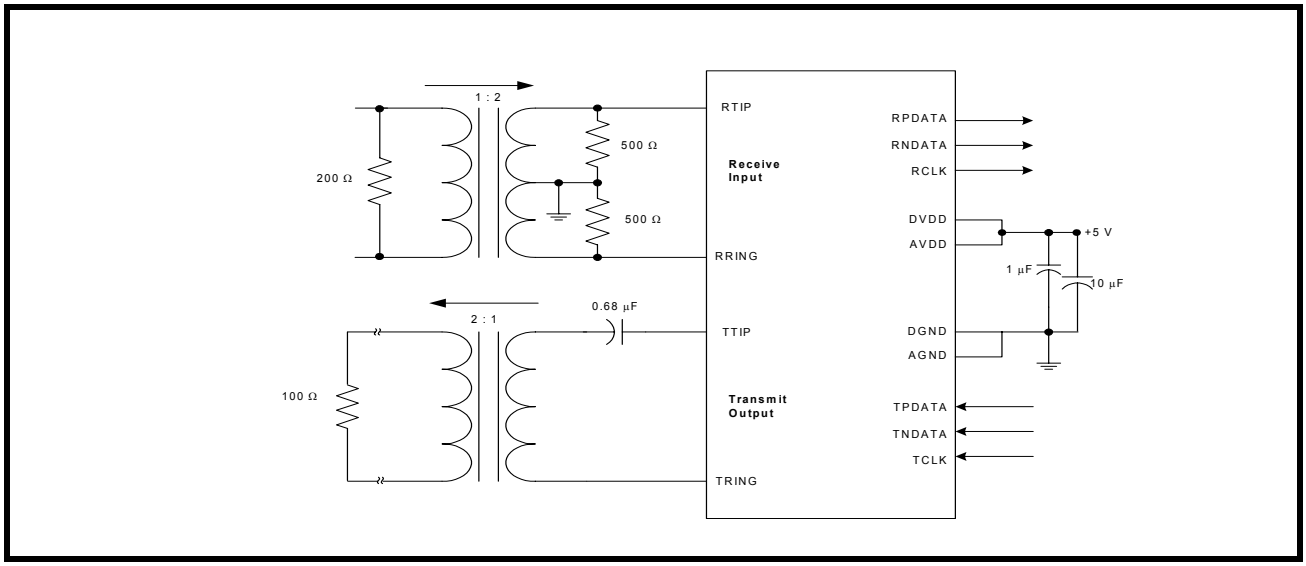


FIGURE 10. CEPT APPLICATION FOR COAXIAL INTERFACE - 5V OR 3.3V OPERATION.

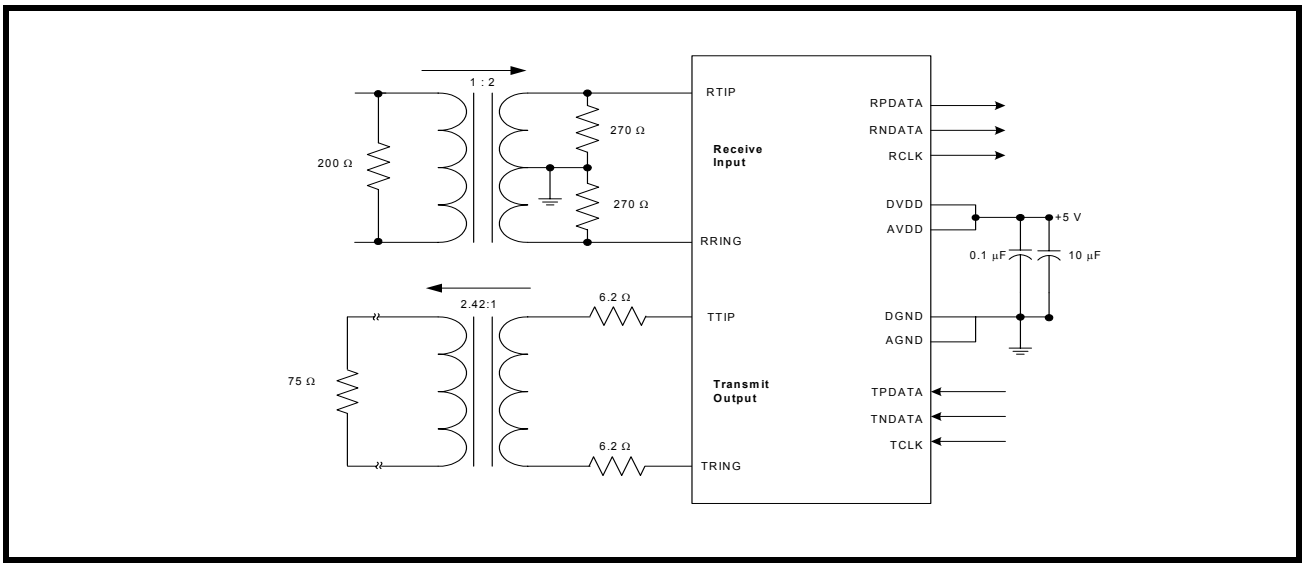
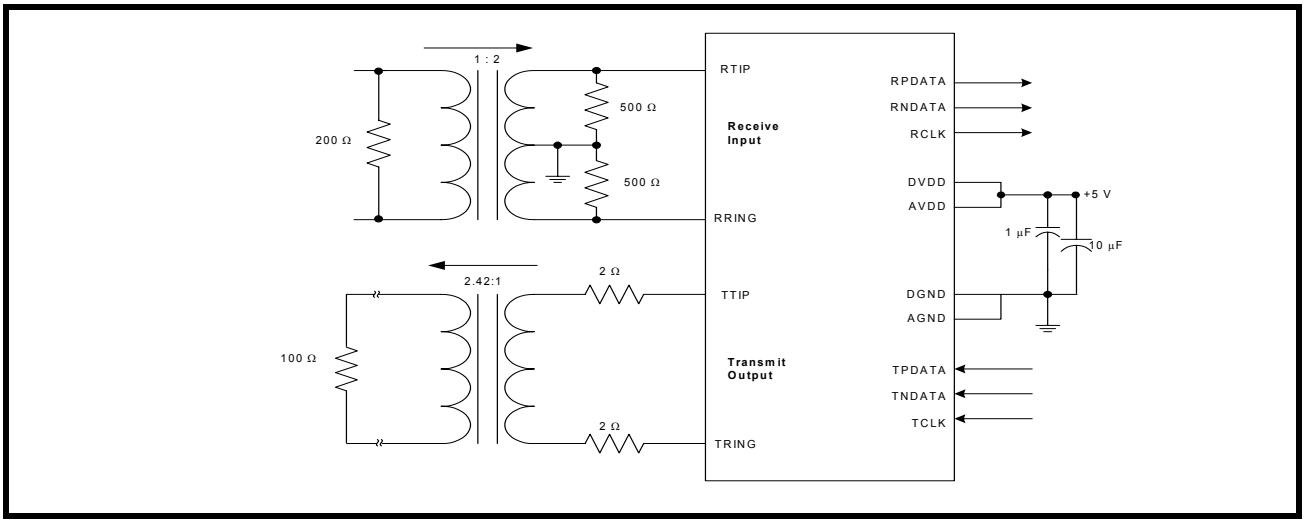


FIGURE 11. DS1 APPLICATION FOR TWISTED-PAIR INTERFACE 5V OR 3.3V OPERATION



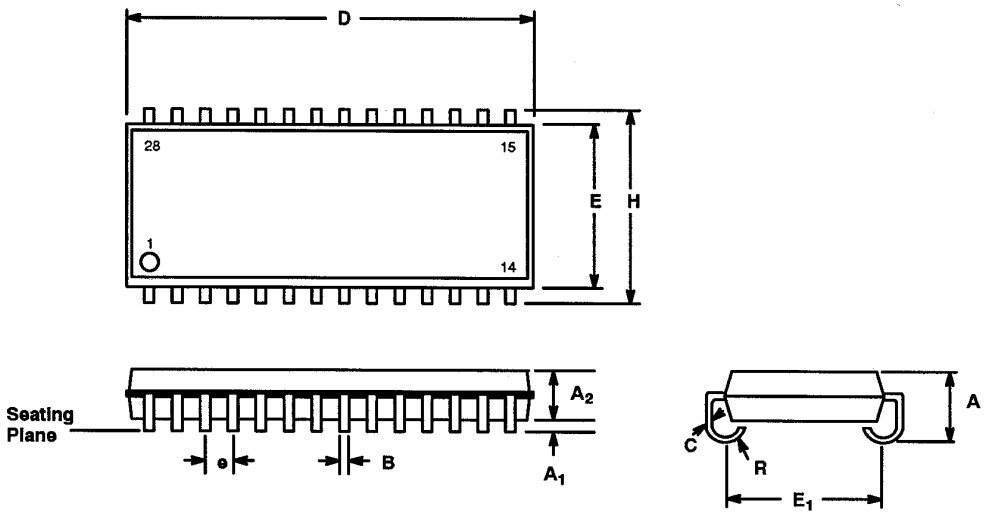
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83D10IW	28 Lead 300 Mil Jedec SOJ	-40^0C to $+85^0$C

PACKAGE DIMENSIONS

28 LEAD SMALL OUTLINE J LEAD (300 MIL JEDEC SOJ)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.120	0.140	3.05	3.56
A_1	0.025	---	0.64	---
A_2	0.090	0.094	2.29	2.39
B	0.014	0.020	0.36	0.51
C	0.008	0.013	0.20	0.30
D	0.697	0.712	17.70	18.08
E	0.292	0.300	7.42	7.62
E_1	0.262	0.272	6.65	6.91
e	0.050 BSC		1.27 BSC	
H	0.335	0.347	8.51	8.81
R	0.030	0.040	0.76	1.02

Note: The control dimension is the inch column

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	06/17/03	1st release of the XRT83D10 mkll.0 preliminary data sheet.
P1.0.1	7/28/2003	Modified the block diagram. Added application circuits.Corrected the timinga dn electrical characteristics.
P1.0.2	8/11/2003	For Receiver Sensitivity, added a note stating that DS1 measured at 772 KHz and CEPT measured at 1024 KHz.
P1.0.3	8/29/2003	Cleaned up the description for the LOS condition.
P1.0.4	12/16/2003	Transformer information and resistor values included.Rearranged and added information in the tables.
1.0.0	2/16/2004	The TBD numbers filled in. "Preliminary" removed.
1.0.1	3/12/2004	Included Table 7
1.0.2	5/3/2004	Included the Power Levels for DS1
1.0.3	7/23/2004	Included the Max Power numbers.Included Figure 11 for DS1 interface